Study of Wallace Tree Multiplier using Reversible Logic Gate

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Abstract- The objective of this project is to design high performance arithmetic circuits which are faster and have low power consumption using a new adiabatic logic family of CMOS and to analyze its performance for sequential circuits and effects upon cascading. Reversible logic generally used in low power VLSI. This adiabatic logic family is best for arithmetic circuits because the critical path is made of a long chain of cascaded reversing gates. The more advantage of this logic which is speed is high and low power consumption is observed upon cascading which is more precise, it's more suitable for arithmetic circuits. The proposed multiplier is better and provides better result in terms of the number of gates, garbage outputs and constant inputs hardware complexity, and number of transistors required as comparison with the existing circuit. The data is related to the primitive reversible gates which are available in literature and helps researches in designing higher complex computing circuits using reversible gates are represented by this paper.

Keywords—Reversible logic gate, Wallace multiplier, Reversible circuit, low power.

I. INTRODUCTION

The reversible logic operations do not erase (lose) information and dissipate very less heat. Demand of reversible logic is high in high speed power aware circuits. Interest of reversible circuit is generally high in nanotechnology, quantum computing optical computing and low power CMOS design. Application of reversible logic is high in quantum computers. Quantum network (or a family of quantum networks) can be viewed as a quantum computer. Quantum network can be consists of logic gates; each. A unitary operation on one or more two–state quantum systems called qubits is performed by each gate.

An elementary unit of information corresponding to the classical bit values 0 and 1 is represented by each qubit is reversible, Quantum networks effecting elementary arithmetic operations such as addition, multiplication as well as exponentiation cannot be directly deduced from their classical Boolean counter parts (classical logic gates such as AND or OR are clearly irreversible) because any unitary operation is reversible. Thus, reversible logic components can be made from quantum arithmetic. Serious problems for today's computer chips are heat generation and power dissipation.

The 30-year-long trend in microelectronics has been to increase both speed and density by scaling of device components. In the last the heat generation is reduced by higher level of integration and new fabrication processes during this trend. Quantum gates which are represented by unitary matrices have potentials to implement reversible logic circuits. A valid quantum operation is represented by each quantum gate. Each quantum gate must be unitary and hence must be reversible. Many classical logic gates are irreversible but quantum gates are reversible.

II. REVERSIBLE LOGIC GATE

1) If n is input and m output is logic gate and there is a one-to-one correspondence between its inputs and outputs, and then this type of logic gate is called to be reversible.

2) If and only if the (Boolean) function is objective then the gate is said to be reversible. In other words, a gate is reversible if each of its input vector maps into a unique output vector and vice versa.

Following are basic reversible gates:

FEYNMAN GATE:

The Feynman gate is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out

Purposes. The inputs (A, B) and outputs P=A, Q=A XOR

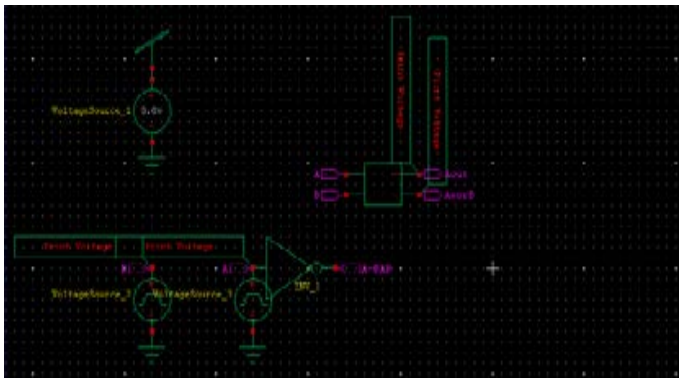


Fig:2.1 Design Of Feynman Gate

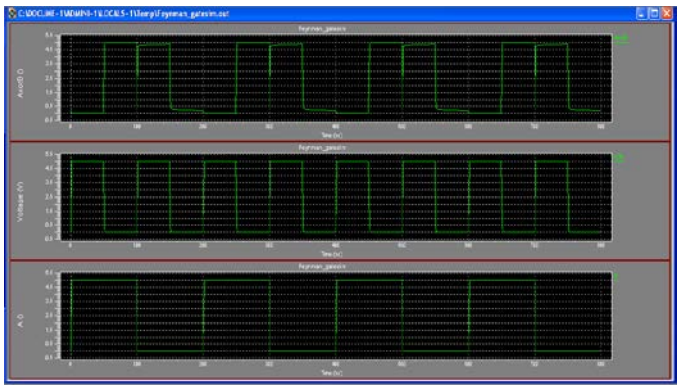


Fig 2.2 Output Simulation Of Feynman Gate

TOFFOLI GATE:

Toffoli gate which is a 3*3 gate with inputs (A, B, C) and outputs P=A, R=AB XOR C, Q=B.

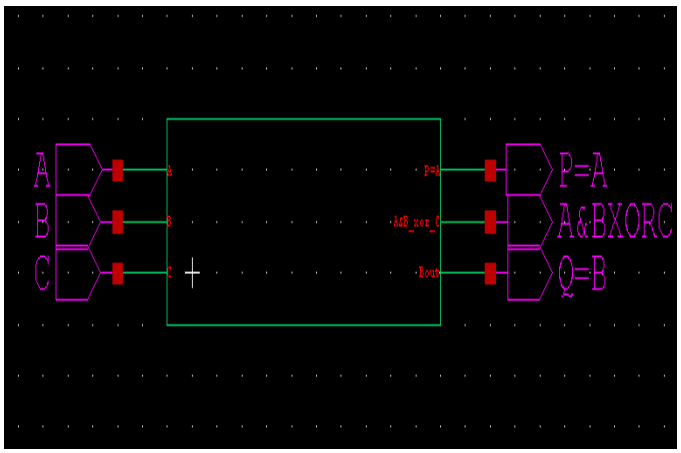


Fig2.3 Design Of Toffoli Gate

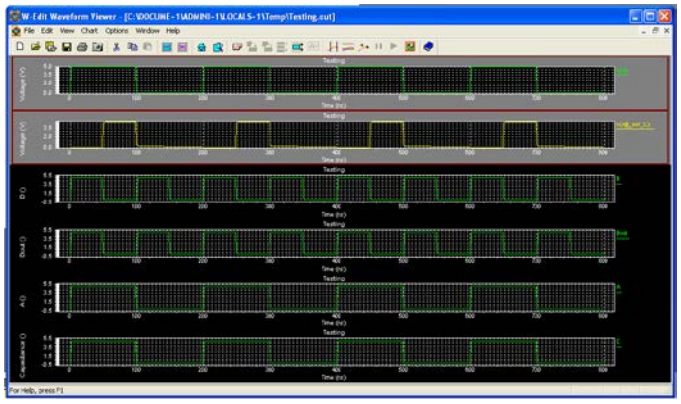
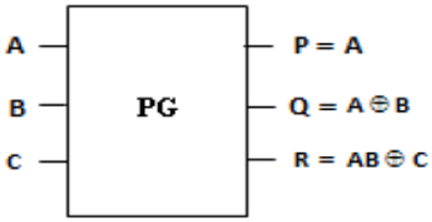


Fig2.4 Simulation Of Toffoligate

PERES GATE:

Peres gate which is a 3*3 gate having inputs (A, B, C) and outputs

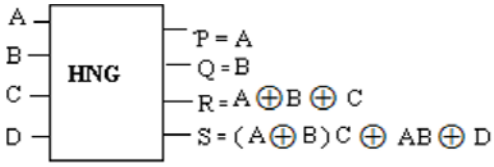
P = A; Q = A XOR B; R = AB XOR C.



HAGHPARAST NAVI GATE:

Each output is annotated with the corresponding logic expression. It is 4*4 gate having some inputs are (A, B, C, D) and output P=A, Q=B,

R=AB XORC, S= (A XOR B) C XOR AB XOR D.



This document proved that the proposed Wallace multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required.

By using full adders and half adders in their reduction phase. This paper presented that Wallace high-speed multipliers half adders do not reduce the number of partial product bits. Hence, in hardware reduction complexity can be achieved by the number of half adders used in a multiplier reduction. This document proposed a novel reversible multiplier and the aim of this paper is to decrease the depth of the circuit. In this paper the depth of novel reversible multiplier is less without increasing the quantum cost or the number of garbage outputs with respect to previous counterparts. In proposed design, using Peres gates partial products are generated.

This study provided the initial threshold for building more complex system which can execute more complicated operations using reversible logic. It is proved that the proposed multiplier architecture using the proposed TSG gate is better than the existing counterpart in literature in terms of reversible gates and garbage output.

III. PREVIOUS WORK

[1] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, “Low-power digital signal processing using approximate adders,” Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on,vol. 32, no. 1, pp. 124–137, jan. 2013. IEEE Transactions on, vol. 18, no. 8, pp. 1225–1229, aug. 2010.

- This paper targeted low power and propose five different versions of mirror adders.

- Complexity level of the circuitry is quite high.
- Very few researches have reported work on approximate multipliers.

[2] M. B. Sullivan and E. E. Swartzlander, "Truncated error correction for flexible approximate multiplication," in Signals, Systems and Computers (ASILOMAR), 2012 Conference Record of the Forty Sixth Asilomar Conference on, 2012, pp. 355–359.

- This paper proposed the iterative approximate multiplier in which some amount of error correcting circuitry is added for each iteration.
- As the no. of iterations performed are more it added a significant delay.

[3] Ron S. Waters, Member, IEEE, and Earl E. Swartzlander, Jr., Fellow, IEEE 2010 propose A Reduced Complexity Wallace Multiplier Reduction saying that Wallace high-speed multipliers use full adders and half adders in their reduction phase. Half adders do not reduce the number of partial product bits. Therefore, minimizing the number of half adders used in a multiplier reduction will reduce the complexity.

[4] Power- and Area-Efficient Approximate Wallace Tree Multiplier for Error-Resilient Systems KartikeyaBhardwaj, Pravin S. Mane 15th Int'l Symposium on Quality Electronic Design 2014 IEEE

- This paper proposes a power and area-efficient Approximate Wallace Tree Multiplier (AWTM) for error-resilient systems.
- The simulation results shown in this paper.
- Shown scope for reduction in area

[5] Synthesis of Dual-Rail Adiabatic Logic for Low Power Security Applications Matthew Morrison, Member, IEEE and NagarajanRanganathan, Fellow, *IEEE*

IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 33, No. 7, July 2014

- This paper gives an idea about the adiabatic logic and the reduction of power dissipation.
- This paper proposes the adiabatic logic for the various circuits

[6] "CMOS Full-Adders for Energy-Efficient CMOS Full-Adders for Energy- Efficient Arithmetic Applications

Mariano Aguirre-Hernandez and Monico Linares-Aranda718 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 19, NO. 4, APRIL 2011

The paper describes An alternative internal logic structure for designing full-adder cellswas introduced. In order to demonstrate its advantages, two full-adders were built in combination with pass-transistor powerless/groundless logic styles.

IV. WALLACE TREE MULTIPLIER

Multipliers do not have the same number of bits in every column. In 1964, Wallace proposed a method for a carry save adder like reduction scheme which is valid for columns of any length Wallace multiplier assumes adders which take multiple inputs of the same weight and produce sum outputs of the

Same weight and carry outputs with higher weights.

These are combined in stages to reduce the number of terms at each weight to 2 or less. These two terms are then added by a conventional adder to produce the final result.

1. In parallel partial products generate all bits.

2. Collect partial products bits with the same place value in Bunches of wires and reduce these in several layers of Adders till each weight has no more than two wires.

3. For all bit positions which have two wires, take one wire at corresponding place values to form one number, and the other wire to form another number. Add these two numbers using a fast adder of appropriate size.

V. REDUCTION PHASE OF WALLACE MULTIPLIER

We assume that Full adders as well as half adders will be used. A full adder takes 3 inputs and produces one output of the Same weight (sum) and another of higher weight (carry). This is called a (3, 2) adder. It reduces the number of wires At its own weight by 2 and adds one wire at the higher Weight.

A half adder takes 2 inputs and produces one output of the Same weight (sum) and another of higher weight (carry).

This is a (2, 2) adder. It reduces the number of wires at its Own weight by 1 and adds one wire at the higher weight.

The reduction algorithm is general and can be used with Any adders of type (n,m). For example, a carry save adder of type (4, 2).

Each reduction stage looks at the number of wires for each Weight and if any weight has more than 2 wires, it adds a Layer of adders.

When the numbers of wires for every weight have been Reduced to 2 or less, we form one number with one of the Wires at corresponding place values and another with the Other wire (if present).

These two numbers are added using a fast adder of Appropriate size to generate the final product.

At any l for any weight, we place a Full Adder, which generates 1 wire of the same weight and1 wire with the next higher weight. We place enough full adders in this layer such that the remaining wires for any weight are less than Ayer, if we find 3 wires If only one wire is left, it is carried through to the next layer. If there are two wires left after using Full Adders for all groups of 3, we have the option of either passing them both through to the same weight or to pass 1 wire to the same weight and the other to the next higher weight (using a Half Adder).Different rules apply for the last reduction step and the earlier ones.

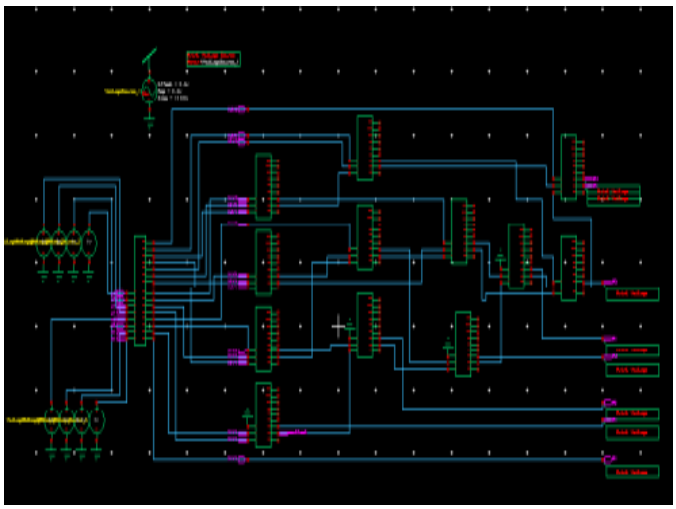


Fig-3.1: Design Of Wallace Multiplier.

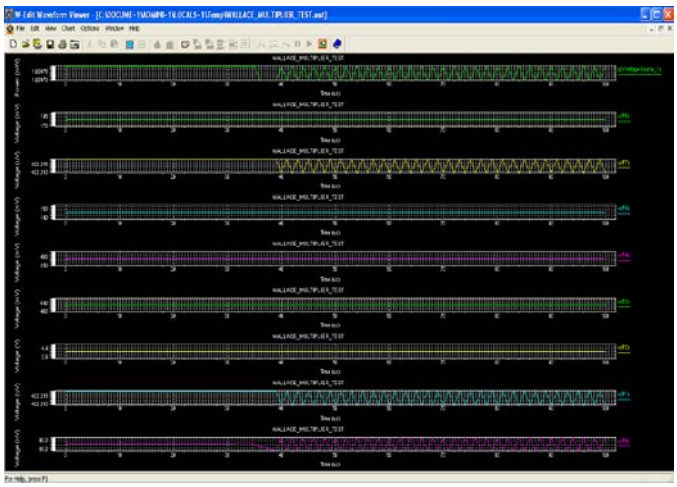


Fig-.3.2 Output Simulation Waveform Of Wallace Multiplier

VI. CONCLUSIONS

Wallace tree multiplier method reduces partial product array and it can be used for implementation of reversible multiplier with the use of reversible logic gate using pass transistor logic. By using reversible logic gate number of transistor is reduced and hence hardware complexity is less. Due to these reasons, Reversible multiplier is better and most favorable method than other methods.

There are many uses of reversible logics such as low power CMOS, nanotechnology, quantum computing and optical computing.

VII. FUTURE SCOPE

The objective of this project is to design high performance low power multiplier circuits using this new CMOS adiabatic logic. Second is to analysis the performance of this logic when applied to sequential circuits and also the effects upon cascading. Main objective is to design a tree multiplier by using CMOS power efficient adder to reduce no of gates using adiabatic logic architecture.

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