To Reduce The Number of Flip-Flops By Using State Look-Ahead Logic Based on Parallel Counter Architecture

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Abstract *- The microcomputer and its peripherals are operated at different frequencies. The Input frequencies can be divided using frequency dividers and connected to each module. This can be done by using flip-flop circuit, since each flip-flop can divide the input frequency by 2. Thus the required frequencies can be drawn from the output of series connected flip-flops. This requires large number of flip-flops. In our design we will reduce the number of flip-flops by using State Look-Ahead Logic Based on A Digital CMOS Parallel Counter Architecture‖. We design a scalable high-speed divide-by-N frequency divider using only basic digital CMOS circuits. The divider achieves high-speed operation using a novel parallel counter and a pipelined architecture. The structure is scalable to arbitrary bit counter widths (2-to- range) using only the three module types and no fan- in or fan-out increase.*

Keywords*- Architecture design, high-performance counter design, parallel counter design, pipeline counter design.*

I. INTRODUCTION

A counter is a sequential logic circuit which are capable of counting numbers of clock pulses. These are the special case of registers hear each counter may contain multiple numbers of J-K flip-flops or T flip-flops. Output of flip-flop constitute the state of the counter. A counter is nothing but change of state after the arrival of each clock pulse. Each count, a binary number is called the state of the counter. Hence a counter counting in term of n bits has 2n different states. The number of different states of the counter is known as modulus of the counter. Thus, an n bit counter is a module 2n counter.

Problem formulation:

In this thesis, we presented a scalable high-speed parallel counter using digital CMOS gate logic components using CMOS layout design. We design a gigahertz, wide range, cost- effective technology scaling programmable divide-by-N frequency divider implemented in 0.12μm CMOS technology. The key novelty of our frequency divider is its architectural improvements. Since we implement all circuit blocks as digital logic CMOS structures, these circuit blocks can easily be replaced with alternative optimized dividers in order to maximize the operating speed and further reduce the power consumption. The parallel operation of our frequency divider makes the architecture amenable to arbitrary width scaling, resulting in both high-speed and predictable operation. Our divider provides a low-cost implementation for continued technology scaling, which is attractive for both SOC and VLSI implementation.

This thesis is structured as follows. Our counter design logic is comprised of only 8-bit counting CMOS layout modules and three-input AND gates. The counter structure's main features are a pipelined paradigm and state look-ahead path logic whose interoperation activates all modules concurrently at the system's clock edge, thus providing all counter state values at the exact same time without rippling affects. In addition, this structure avoids using a long chain detector circuit typically required for large counter widths. An initial m-bit counting module pre- scales the counter size and this initial module is responsible for generating all early overflow states for modules of higher significance. In addition, this structure uses a regular VLSI topology, which is attractive for continued technology scaling due to two repeated module types (module-2s and module-3s) forming a pattern paradigm and no increase in fan-in or fan-out as the counter width increases, resulting in a uniform frequency delay that is attractive for parallel designs. Consequently, the counter frequency is greatly improved by reducing the gate count on all timing paths to two gates using advanced circuit design techniques. This layout avoids setup and hold time violations, which might ultimately be limited by race conditions.

This thesis will work on 3 bit asynchronous counter is best implemented using the 0.12micron technology. In this the required switching delay will be minimum i.e. 90ps, power consumption is 2.087 m. Watt, Max operating frequency is 1.4 GHz, layout size area is 440.6 micro sq. meter. Thus that 3 bit asynchronous counter is best implemented using the 0.12micron technology is preferable over .6 micron technologies in maintaining the logic density in fabrication process, power optimization, reducing the propagation delay

& surface area. Thus this counter implemented in CMOS chip technology, is the best illustration of VLSI.

II. PROPOSED PARALLEL COUNTER

A state look ahead logic can be proposed so that the counter will operate at different frequencies as per our requirements. A single clock input triggers all counting modules simultaneously, resulting in an operating frequency independent of counter width (assuming ideal parasitic capacitance on the clock wire path, without loss of generality). The total critical path delay (regardless of counter width) is uniform at all counting stages and is equal to the combination of the access time of a 2-bit counting module, a single three-input AND gate delay, and the DFF setup-hold time.[1]

Our parallel counter architecture leverages modularity, which enables high flexibility and reusability, and thus enables short design time for wide counter applications. The architecture is composed of three basic module types separated by DFFs in a pipelined organization. These three module types are placed in a highly repetitious structure in both the counting path and the state look-ahead paths, which limit localized connections to only three signals (thus, fan-in and fan-out).

The counter output is in radix-2 representation so the count value can be read on-the-fly with no additional logic decoding.

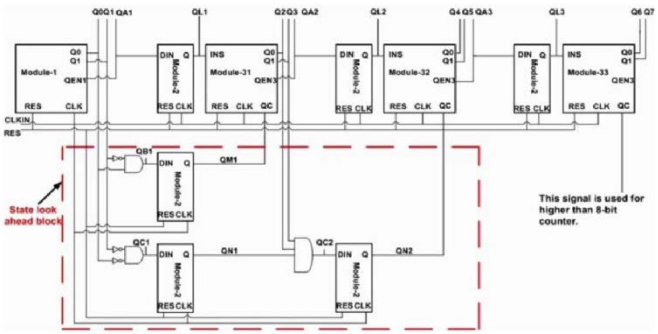


Figure 2.1 Functional block diagram of our proposed 8-bit parallel counter with state look-ahead logic and counting logic

Fig.2.1 depicts our proposed parallel counter architecture for a sample 8-bit counter. The main structure consists of the state look-ahead path (all logic encompassed by the dashed box) and the counting path (all logic not encompassed by the dashed box). We construct our counter as a single mode counter, which sequences through a fixed set of pre-assigned count states, of which every next count state represents the next counter value in sequence. The counter is divided into uniform 2-bit synchronous up counting modules. Next state transitions in counting modules of higher significance are enabled on the clock cycle preceding the state transition using stimulus from the state look-ahead path. Therefore all counting modules concurrently transition to their next states at the rising clock edge (CLK IN). [1]

Architectural Functionality:

The counting path's counting logic controls counting operations and the state look-ahead path's state look-ahead logic anticipates future states and thus prepares the counting path for these future states. Fig.2.1 shows the three module types (module-1, module-2 and module-3, where etc. (increasing from left to right) and represents the position of module-3) used to construct both paths.module-1 and module-3 are exclusive to the counting path and each module represents two counter bits.module-2 is a conventional positive edge triggered DFF and is present in both paths. In the counting path, each module-3 is preceded by an associated module-2.module-3 serve two main purposes. Their first purpose is to create all counter bits related with their ordered position and the second purpose is to enable (in conjunction with stimulus from the state look-ahead path) future states in subsequent module-3 (higher values) in conjunction with stimulus from the state look-ahead path.

Module-1 :

Module-1 is a standard parallel synchronous binary 2-bit counter, which is responsible for low-order bit counting and generating future states for all module-3 in the counting path by pipelining the enable for these future states through the state look-ahead path. Fig.2.2 depicts the (a) hardware schematic and (b) state diagram for module-1. Module-1 outputs (the counter's two low-order bits) and (the 1 in denotes that this is for module-1) connects to the module-2 input. The placement of module-2s in the counting path is critical to the novelty of our counter structure. Module-2s in the counting path act as a conduit between the module-1 and module-3(see Fig.2.1).

Module-2 placement (coupled with state look-ahead logic described in Section II-A2) increases counter operating frequency by eliminating the lengthy AND-gate rippling and large AND gate fan-in and fan-out typically present in large width parallel counters. Thus, instead of the modules of higher significance requiring the ANDing of all enable signals from modules of lower significance, modules of higher significance (module-3's in our design) are simply enabled by the module-3 pre- ceding module-2 and state look-ahead logic. Since the coupling of module- 2 with module-3 1 introduces

an extra cycle delay before module-3 1 is enabled, module-2's is triggered when the module-1 count (note that this is only the case for the left most module-2 in the counting path in Fig. 2.1, as subsequent module-2 require state look-ahead logic as well). Thus, the module-2s in the counting path provide a 1-cycle look-ahead mechanism for triggering the module-3.

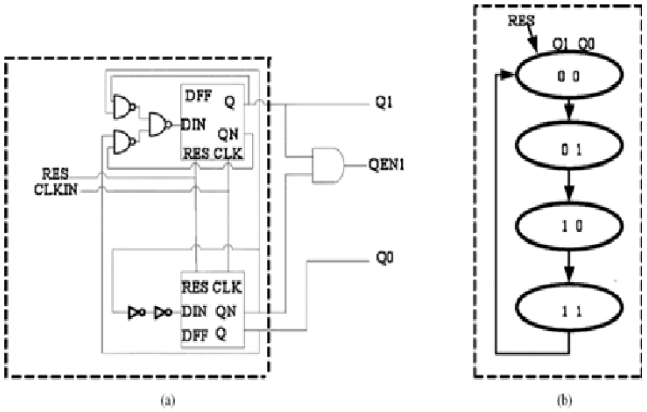


Figure: 2.2 Module-1 (a) hardware schematic and (b) state diagram. Note that the 1 in denotes that this is the for module-1

Module-2 :

The placement of module-2s in the counting path is critical to the novelty of our counter structure. Module-2s in the counting path act as a pipeline between the module-1 and module-3 1 and between subsequent module-3 (see Fig.4.1). Module-2 placement (coupled with state look-ahead logic) eliminates the lengthy AND-gate rippling and large AND gate fan-in and fan-out typically present in large width parallel counters. Thus, instead of the modules of higher significance requiring the ANDing of all enable signals from modules of lower significance, modules of higher significance are simply enabled by the module-3S preceding module-2 and state look-ahead logic.

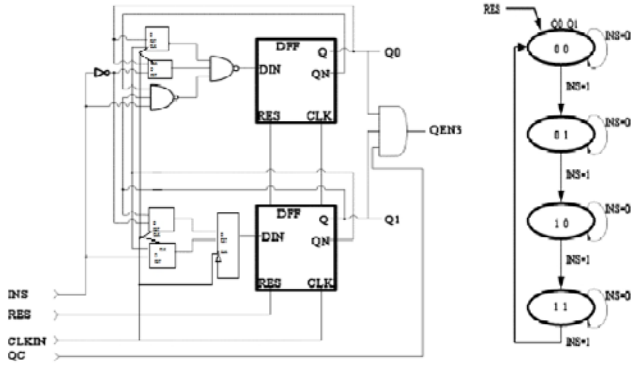


Figure.2.3 Module-2S (a) Hardware Schematic and (b) State Diagram

Since the coupling of module-2 with module-3 1 introduces an extra cycle delay before module-3 1 is enabled, module-2's is triggered when the module-1's count (note that this is only the case for the left most module-2 in the counting path in Fig.2.1, as subsequent module-2s require state look-ahead logic as well). Thus, the module-2s in the counting path provide a 1-cycle look-ahead mechanism for triggering the module-3's, enabling the module-2s to maintain a constant delay for all stages and all module-3S 's to count in parallel at the rising clock edge instead of waiting for the over flow rippling in a standard ripple counter. [6]

Module-3:

Module-3 S is a parallel synchronous binary 2-bit counter whose count is enabled by INS. INS connects to the Q output of the preceding module-2. Module-3 S outputs Q1Q0 and QEN3=Q1 AND Q0 AND QC. The state look-ahead logic provides the QC input. QEN3 connects to the subsequent module-2's DIN input and provides the one-cycle look ahead mechanism. The DIN input for the Module-1 is provide by flip flop which is being replaced instead of 2 inputs AND gate.

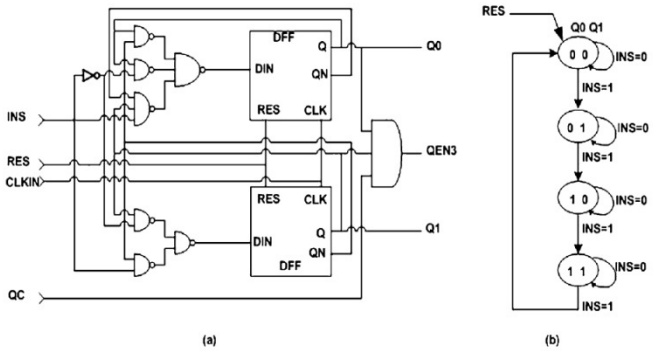


Figure: 2.4 Module-3*S* (a) hardware schematic and (b) state diagram

State Look-Ahead Path:

The state look-ahead path operates similarly to a carry look-ahead adder in that it decodes the low-order count states and carries this decoding over several clock cycles in order to trigger high-order count states. The state look-ahead logic is principally same to the one-cycle look ahead mechanism in the counting path. For example, in a 4-bit counter constructed of two 2-bit counting modules, the counting path's module-2 decodes the low-order state Q1Q0= 10 and carries this decoding across one clock cycle and enables Q3Q2=01 at module-3 1 on the next rising clock edge. This operation is same as to decoding Q1Q0=11 and enabling Q3Q2=01 on the next immediate rising clock edge. The state look-ahead logic expands this principle to a cycle look-ahead mechanism.

For example, in a traditional 6-bit ripple counter constructed of three 2-bit counting modules, the enabling of bits Q5Q4 happens only after decoding the overflow at Q1Q0 to enable Q3Q2 and decoding the overflow at Q3Q2 to enable Q5Q4. However, combining the one cycle look-ahead mechanism in the counting path for Q3Q2=10 and a two-cycle look-ahead mechanism for Q1Q0=01 from can enable Q5Q4. Thus, enabling the next state's high Thus, enabling the next state's high order bits depends on early overflow pipelining across clock cycles through the module-2s in the state look-ahead path. This state look-ahead logic organization and operation avoids the use of an overhead delay detector circuit that decodes the low order modules to generate the enable signals for higher order modules, and enables all modules to be triggered concurrently on the Clock edge, thus avoiding rippling and long frequency delay.

Counter topology of N bit counter depicts a generalized N-bit counter topology, revealing state look-ahead path details. Module-2s in the state look-ahead logic are responsible for propagating (pipelining) the early overflow detection to the appropriate module-3.Early overflow is initiated by the module-1 through the left-most column of decoders (state-2, state-3, etc.). The Q output of the right-most module-2 (Q1, Q2 etc.) in each early overflow pipelining chain is connected to the QC input of the appropriate module-3. The module-3's output), indicating that not only has that module-3 overflowed, but all modules preceding that module-3 have also overflowed, thus enabling the count in the subsequent module-3.

Each module-2s early overflow pipelining chain is preceded by a small logic block (State-X), which decodes the appropriate value for early overflow pipelining denotes the number of clock cycles that the early overflow pipelining must carry through. For example, State-3 means that the early overflow signal must carry through two clock cycles, and thus enable the appropriate module-3 on the third clock cycle. Each State block consists of simple two-input AND logic that decodes the module-1's output. shows the internal logic for State-2 and State-3 as an respectively, and whose outputs and, respectively, are connected to the appropriate module-2s input, thus starting the early overflow pipelining exactly clock cycles before the overflow must be detected to enable counting in a module-3. Note that module-1 and module-3 may be of arbitrary bit width, and thus the same look-ahead principle would equally apply. [1]

III. DESIGN OF TEST CIRCUIT

Module-1 is counter module and module-2 is selection module and module-3 is decision Logic decision logic takes decision and work accordingly for different frequencies of counter. Here we design module counter without changing hardware and design process.

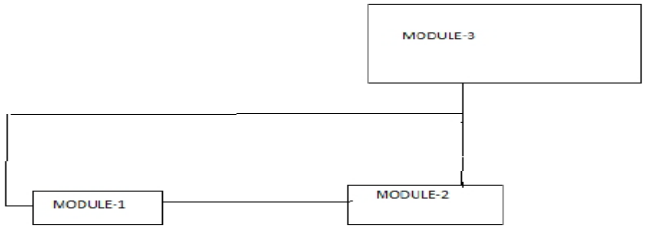


Figure: 3.1 Block diagram of state look-ahead logic

IV. SOFTWARE USED

For CMOS Layout design MICROWIND 3.1 is used. MICROWIND a program allows to design and simulate an integrated circuit. A specific command displays the characteristics of PMOS and NMOS where the size of device and process parameters easily changed. By MICROWIND node to node calculation is done.

4.1 Layout design for state look ahead logic

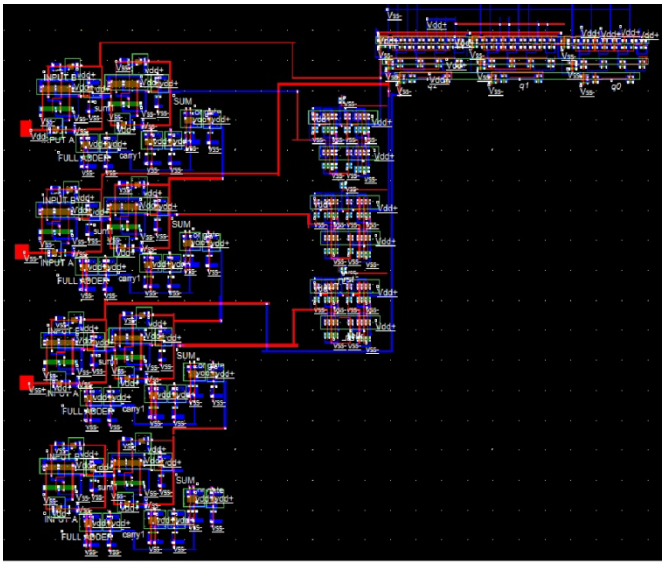
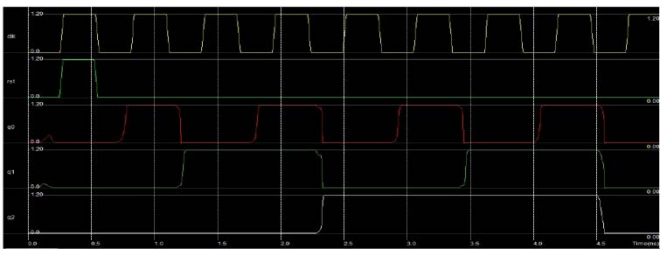


Figure: 4.1 Layout design for state look ahead logic



4.2 Timing simulation of state look-ahead logic

The analysis of the average power dissipation, timing analysis, and voltage vs. timing simulation and current vs.

timing simulation is estimated on Microwind layout tool. All the simulations have been done on Microwind layout design tool. Simulations are performing at the voltage level of 1.2V with the load capacitance of 1fF. The input clock frequency fed in the range of 0.49GHz to 2 GHz range with the output frequency calculates in the range of 30.49MHz to 1.3GHZ. The propagation delay of the circuits is 2ns.

However, the operating frequency is degraded by the increase in the number of cascaded cells, which are usually controlled by a synchronous binary programmable value. Furthermore, these counters suffer from a large accumulated jitter due to a long asynchronous cascaded cell topology. The proposed counter is a 4 bit pass transistor base counter, which sequences through a fixed set of pre assigned count states, of which each next count state represents the next counter value in sequence. The counter frequency is greatly improved by reducing the gate count on all timing paths to two gates using pass transistor circuit design techniques. In our work the counter operating frequency is improved by using a parallel counter architecture of pass transistor base flip-flops. All the Simulation has been done on Microwind layout design tool. Simulations are performing at the voltage level of 1.2V with the load capacitance of 1fF. The input clock frequency fed in the range of 0.49GHz to 2 GHz range with the output frequency calculates in the range of 30.49MHz to 1.3GHZ. The propagation delay of the circuits is 2ns.

V. RESULT ANALYSIS

5.1 Design constraints table:

Sr. no	Component	Conventional No of Transistor	No. of Transistor our design	Power
1	AND Gate	6	6	In µw
2	OR Gate	6	6	In µw
3	Latch	18	18	In µw
4	Flip-Flop	38	31	In µw
5	4 bit Counter	136	124	1.818 to 3.0mw
6	6 bit Counter	204	186	1.866 to 2.004mw
7	8 bit Counter	272	248	1.911 to 2.005 mw
8	Module 1	70	102	0.265 to 0.304 mw
9	Module 2	144	93	0.265 to 0.304 mw
10	Module 3	270	184	0.265 to 0.304 mw
11	State look A-head logic	414	379	0.265 to 0.304 mw

5.2 Comparative analysis table

References	Alioto et. Al	Kakarounts	Yeh	Saleh Abdel-Hafeez	Our design
Technology	0.18	0.6	0.15	0.12	0.12
Power	2.21mW	21.3Mw	7.64mW	13.89mW	0.265mW to 0.304mW
No. of transistor	160	286	373	510	379
Drawbacks	Require biasing	O/p not in binary	Latency depends on counter size	Large area	1. No biasing 2. Counter size fixed 3. Less no. of Transistor

VI. CONCLUSION

All the simulation have been done on Microwind layout design tool Simulation are perform at the voltage level of 1.2V with the load capacitance of 1fF. The input clock frequency fed in the range of 0.49GHz to 2 GHz range with the output frequency calculates in the range of 30.49MHz to 1.3GHZ. The propagation delay of the circuits is 2ns.

In this thesis we use the number of transistor as shown in table [6.2], then we have these result -

- Our Power Dissipation is 0.265mW to 0.304mW,this result is less than reference[1]
- Our No. of transistors is 379,this result is less reference[1]
- Our Technology is 0.12

VII. FUTURE SCOPE

- Non-ideal effects not consider such as body effect, odd electronic effect, drain punch through effect by considering these non ideal effect we can redesign the module.
- The performances of the proposed testing circuits should evaluate in terms of speed, area, and power and hardware.
- By applying power dissipation techniques work is done on this state look ahead module.

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