Simulation and Harmonics Analysis of a Diode Clamped 7-Level Inverter

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Abstract – This paper presents simulation and harmonics analysis of seven level inverter using PWM techniques which can minimize total harmonic distortion (THD) and enhance the output voltage. Also presents different topologies of multilevel inverter. For multilevel inverters IGBT's and MOSFET's are used as switching devices to make the inverter more accurate. Multilevel inverters are important for power electronics application such as, active power filters and uninterruptible power supplies Multilevel Inverters are used for power electronics application such as FACTS ups etc. The function of an inverter is to change a dc input voltage to a symmetrical ac output voltage of desired magnitude and frequency and the output can be fixed and variable at a fixed and variable frequency. A variable output voltage can be obtained by varying the gain of inverter which is normally found by Pulse width modulation control. In this paper we proposed the phase disposition PWM strategy. This PWM technique reduces the total harmonic distortion of different multilevel inverters.

***Keywords*: multilevel inverters, types of multilevel inverters, PWM technique, MATLAB/SIMULINK, total harmonics distortion.**

1. INTRODUCTION

In the recent years multilevel inverters are mostly used for medium voltages and high power applications. Multilevel inverters are having various advantages such as smaller common mode voltage, low electromagnetic interferences, low dv/dt ratio etc. Multilevel inverter is a worthwhile solution for increase power and reduces harmonics of AC waveforms. [1]

In this paper we present the simulation model of a 7-level inverter. The seven level inverters are most suitable for increasing the output level and reducing the total harmonic distortion of an AC waveform. If the THD is important, the 7-level inverters should be used, since it has a lower THD than the 5-level and 3-level inverter. For the analysis of seven levels inverter, pulse width modulation technique plays an importantrole. In general pulse width modulation technique is a modulation technique used to encode a message into a pulsing signal. Although this modulation technique can be used to encode the Information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors. In addition, PWM is one of the two principal algorithms used in multilevel inverters. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast rate.

2. MULTILEVEL INVERETRS

Three types of multilevel inverter have been investigated in this paper.

2.1. Diode Clamped multilevel inverters

2.2 Flying Capacitor multilevel inverters

2.3 Cascaded H-bridge multilevel inverters

2.1Diode Clamped multilevel inverter

The diode multilevel inverter is also called as neutral point inverter. As the name suggest, they need clamping devices so diodes are used for clamping devices. The diode clamped multilevel inverters have most attention to the industries purposes. For this type of multilevel inverter the main concept is to use diodes to limit the power devices voltages tress. The voltage over each capacitor and each switch is V_{dc}. An *n* level inverter needs (*n*-1) voltage sources, 2(*n*-1) switching devices and (*n*-1)(*n*-2)diodes. [4]

The three phase diode clamped inverters have three legs with a common DC bus. One phase of diode clamped multi level inverter is shown in Fig. 1.Switchingstatesare shownin Table.1.ForexampletohaveVdc/2intheoutput,switchesS1toS4s houldconductatthe same time. For each voltage level four switches shouldconduct.AsitcanbeseeninTable.1 the maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped multilevel inverter. This problem can be solved by using at wo times voltage source or cascading two diode clamped multilevel inverters.

Table 1 the switching states of Diode clamped multilevel inverter.

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

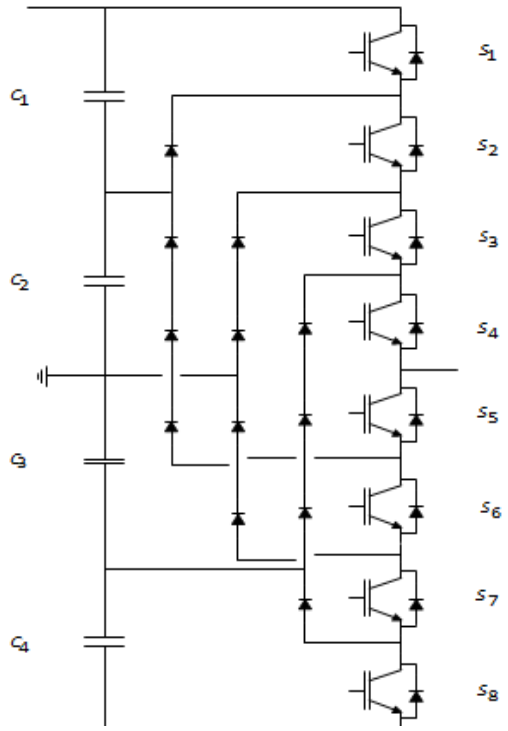

Figure 1 One phase of a diode clamped inverter

2.2 Flying Capacitor multilevel inverters

In this type of multilevel inverter, no clamping diodes are needed. This inverter uses capacitors to limit the voltage of the power devices. The configuration of the flying capacitor multilevel inverter is like a diode clamped multilevel inverter except that capacitors are used to divide the input DC voltage. The voltage over each capacitor and each switch is V_{dc}.

Fig. 2 show flying capacitor multilevel inverter. The switching states in this inverter are like in the diode clamped multilevel inverter. It means that for each output voltage level 4 switches should be on. Table.2 shows the switching states for a flying capacitor clamped multilevel inverter. The output voltage was shown before in Fig.1.

The switching angles like the diode clamped multilevel inverter should be calculated in such a way that the THD of the output voltage becomes as low as possible. The method is the same as the diode clamped inverter.

Table 2 the switching pattern for capacitor clamped multilevel inverter.

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-V_{dc}/4$	1	0	0	0	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

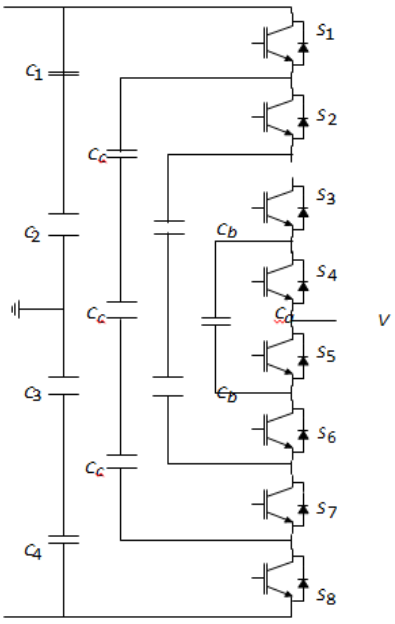

Figure 2 One phase of a Flying capacitor multilevel inverter

2.3 Cascaded H-bridge multilevel inverters

In this type of multilevel inverter, IGBT has used for switching devices. These switches are having high switching frequency and low blocking voltage. A single-phase structure of an m-level cascaded inverter is illustrated in Figure.3. Each separate DC source (SDCS) is connected to a single-phase full-bridge, orH-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S1 , S2 , S3 , and S4 .To obtain $+V_{dc}$, switches S1 and S4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S2 and S3 . By turning on S1, S2, S3, and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are

connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources.

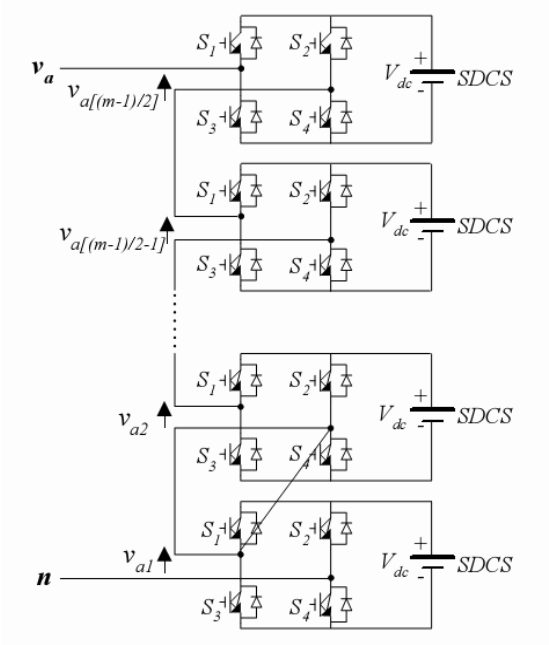

Figure 3 single phase structure of cascade h-bridge multilevel inverter

3. PROPOSED METHODOLOGY

In this paper we proposed phase disposition PWM technique for the simulation and harmonic analysis of seven levels multilevel inverter. In the multilevel inverter, the control techniques are based on high switching frequency.For the diode-clamped multilevel inverter several sinusoidal PWM techniques have developed. The most popular and simple switching scheme for multilevel inverter is the phase disposition PWM technique. The sinusoidal pulse width modulation of an m-level inverter, (m-1) carriers with the same frequency fc and same amplitude Ac are positioned such that the bands they occupy are contiguous. The reference waveform has peak to peak amplitude of Am and a frequency fm. Its zero amplitude is centered in the middle of the carrier set. The reference is continuously compared to each of the carrier signals. If the amplitude of the reference is greater than the amplitude of the carrier signal, then the switch corresponding to that carrier is switched.

4.SIMULATION/EXPERIMENTAL RESULTS

The 7-level topology is similar to 5-level inverter. In this paper we use GTOs for the switching devices. The gate turn off (GTO) is a semiconductor device that can be turned on and off via a gate signal. Like a conventional thyristor, the GTO can be turned on by a positive gate signal (g > 0). However, unlike the thyristor, which can be turned off only at a zero crossing of current, the GTO can be turned off at any time by the application of a gate signal equal to 0. The GTO thyristor is very popular for the switching devices which help to increase the output voltage and decrease the harmonic distortion [10].

In a 7-level diode clamped multilevel:

n=7

Therefore:

Number of switches=2(n-1) =12

Number of diodes= (n-1) (n-2) =30

Number of capacitors= (n-1) =6

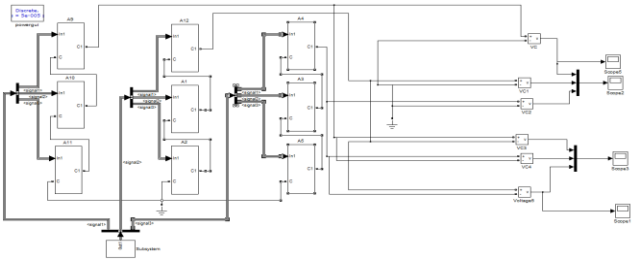

Figure 4 Simulink model of seven levels multilevel inverter

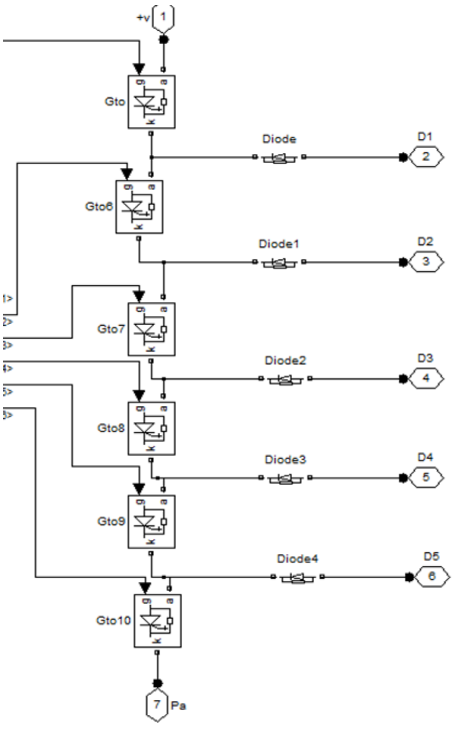

Figure 5 Switching diagram of seven levels multilevel inverter

A 7-level diode clamped multilevel inverter is shown. Switching states are shown in Table. For example to have $V_{dc}/2$ in the output, switches S1 to S6 should conduct at the same time. For each voltage level six switches should conduct. As it can be seen in Table, the maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped multilevel inverter.

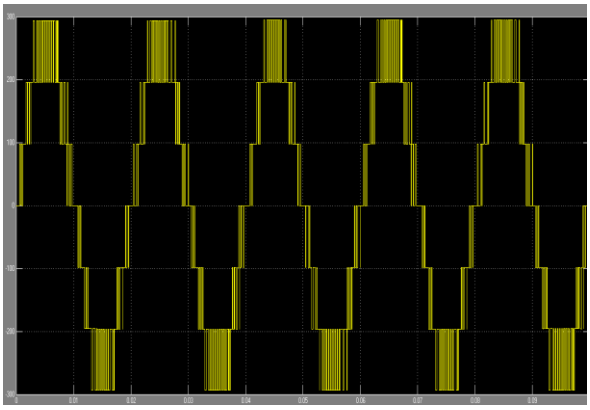

Figure 6 simulation result of seven levels multilevel inverter

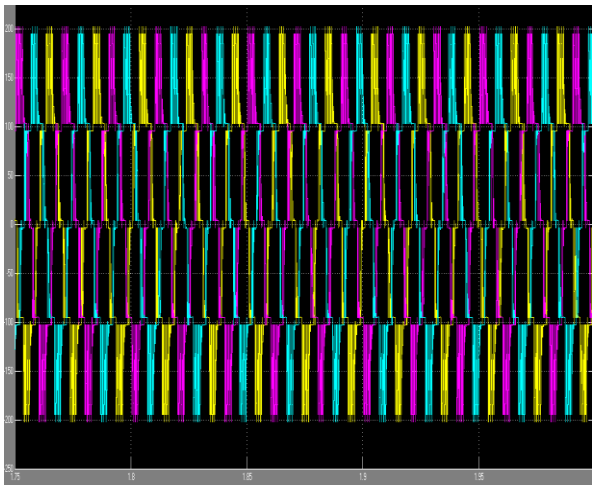

Figure 7 Phase disposition result of seven levels multilevel inverter

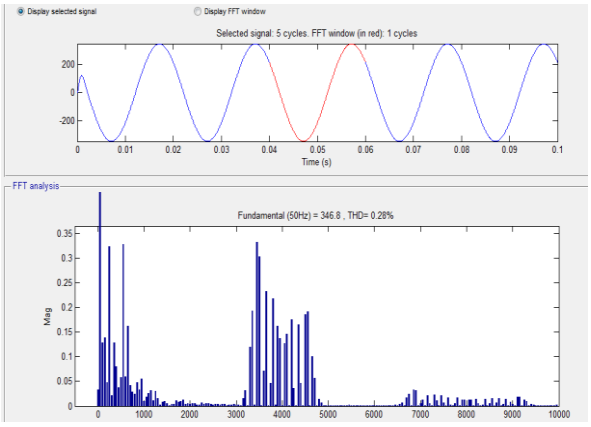

Figure 8 FFT analysis of seven- level multilevel inverter

5. CONCLUSION

The choice of topology for each inverter should bebased on what is the usage of the inverter. Eachtopology has some advantages and disadvantages. By increasing the number of levels, the THD will be decreased but on the other hand cost and weight will be increased as well. Also since the switching angles for switches are not the same, the drive circuit for each switch is separate from other switches.

The two-level inverter has the lowest cost and weight in comparison with the other topologies. But this inverter has a very high THD; its THD is about 40% when one switching event for fundamental period isused. In weight and cost calculations, the price and weight of the filter should be considered, since it is not practical to have an output voltage with 40% THD. The cost and the weight of the 5-level multi level inverters seem better than the 7-level multilevel inverters. By increasing the number of levels, the cost and weight of the multilevel inverter will be increased. The advantage of the 7-levelmultilevelinverters overthe5-level multilevel inverters is their THD before filters, thus a filter will be needed. The 7-level multilevel inverters have lower THD than the 5-levelmultilevelinverters.The Flying capacitor clamped inverter has the lowest power losses between all of the other topologies, since there is no diode in itstopology. For example the power losses in the 5-level flying capacitor multilevel inverter infull load are 625W, but it has two big problems. Firstis that it is heavier than the other topologies. It is not practical to use this heavy inverter in applications that are going to be used in applications that are not stable Also the cost of this inverter is more than other inverters. It seems that the flying capacitor clamped multilevel inverter can be used in applications where the power losses are more important compared to the weight and cost.

The cascadedH-bridgehasthe lowest weight andcost between themultilevel inverters, but its power lossesismore thatalltheothers.

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