Time Interleaved ADC Different Mismatch Calibration using Blackman-Harris Low Pass Filter

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Abstract - Every communication system or digital processing system has an operation of conversion of analog signals into digital form for the processing of information. Such all devices uses analog to digital converter (ADC) chips, i.e. Integrated Circuits (ICs). But during manufacturing process these ICs are not made identical for conversion operations. As a result the output of multi-channel TI-ADC system affected with different mismatches e.g. frequency mismatch, time mismatch, gain mismatch and offset mismatch. This mismatched need to be calibrated for efficient functioning of system. In the similar context in this paper an efficient mismatch calibration methodology is proposed utilizing Fx-LMS algorithm and Blackman-Harris low pass filter. The figure of merit is SFDR which shows the efficiency of the calibration methodology, here we have achieved.

Keywords - SFDR, TI-ADC, Digital Filter and Mismatch Calibration.

I. INTRODUCTION

Nowadays all communication is getting faster and faster. Therefore, the demand for high data rate wireless digital communication is high and research into 60GHz communication and above with several GSps data rate is done. The data rate of the wireless digital communication is limited by the sampling rate and the accuracy of the data converters. Other applications are fast and accurate oscilloscopes that are designed to measure signals in the GHz range.

These applications require high bandwidth analog to digital converters (ADCs) with high accuracy and high sampling rate. These requirements are difficult to realize in a single ADC.

Therefore, Black and Hodges proposed the Time-Interleaved ADC (TI-ADC) architecture [1] in 1980. Since then lots of research has been done into the possibilities of TI-ADCs. The time-interleaving architecture brings some problems with respect to mismatch between its channels.

There are three main mismatch problems: gain-mismatch, offset-mismatch and timing-mismatch. Since TI-ADCs are mainly used in high frequency applications, where the timing-mismatch is dominant, timing-mismatch is the most challenging problem.

II. TIME-INTERLEAVED ADC MODEL

The basic idea of a TI-ADC is to make a fast ADC out of several relatively slow sub-ADCs working together in time-multiplexed mode. The basic concept of a M channel TI-ADC is shown in figure 2.1. In this figure $x(t)$ is a time-continuous and amplitude-continuous signal which is fed to M sample and holds (S&H). Each S&H takes a sample at time *Øi* (i from 0 to M¡1). *Øi* are the sample moments shifted in time as shown in figure 2.2. Ideally the sample moments are equidistant with time *Ts*.

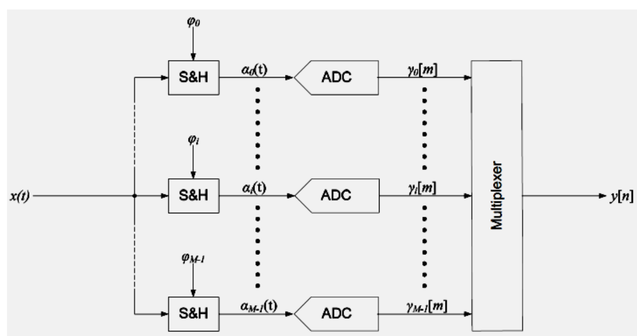

Figure 2.1: Basic Time-Interleaved ADC.

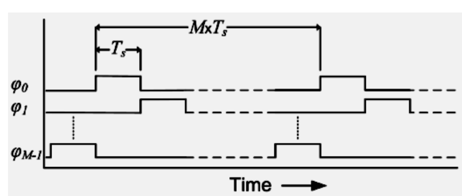

Figure 2.2: Signals *Øi*.

The three most common ADC problems are described in this section, they are sampling jitter, quantization noise and nonlinearity. There has already been a lot of research into these problems and several solutions are available. Therefore, these problems are taken notice of, but will not be considered in the error correction algorithm.

Sampling Jitter:

Sampling jitter are random variations of the sample moments of the S&Hs. The main cause of sampling jitter is device noise and random noise from the power supply and substrate. Sampling jitter is also known as phase noise. Because of the random nature of this error it spreads out through the whole spectrum and increases the noise foor, which results in a decrease of the signal to noise ratio (SNR) [3]. Figure 2.4 shows an example of a simulated spectrum of an ideal ADC, without sampling jitter (a) and with sampling jitter (b).

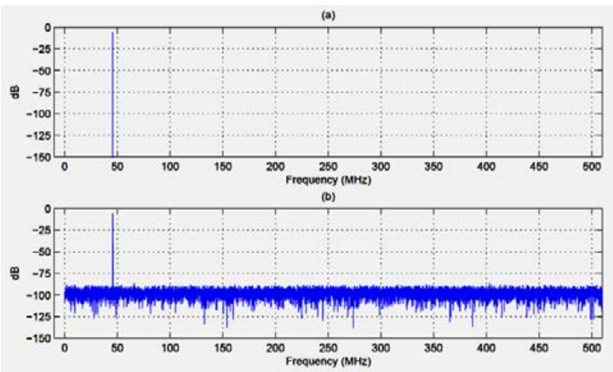

Figure 2.4: Simulated Spectrum of a sine wave (a) without sampling jitter, (b) with sampling jitter

Quantization Noise:

Quantization noise is the error introduced by the amplitude discretization of the signal and is therefore signal dependent `noise', but can be considered to be stochastic noise under the following conditions: transitions equally distributed in time, many transitions and equal quantization steps.

The noise power under these conditions is $q2=12$, where q is the quantization step size. Since q is inversely proportional to the number of bits this error decreases when more bits are used.

This is shown in figure 2.5 for (a) an ideal ADC (no quantization noise), (b) an 8-bit ADC (with quantization noise) and (c) a 16-bit ADC (with quantization noise). For a sine wave with maximal swing SNR=$6{:}02n + 1{:}76$, where n is the number of bits.

Nonlinearity:

ADCs and S&Hs have certain nonlinearities. Their static nonlinearities are expressed in integral nonlinearity (INL) and differential nonlinearity (DNL). For periodic input signals nonlinearities show up in the frequency spectrum as harmonic distortion tones and determine, a.o., the spurious free dynamic range (SFDR) and the signal to noise and distortion ratio (SNDR).

Offset Mismatch:

For the discussion about offset-mismatch the offset errors are assumed to be different for each channel, and all other characteristics are the same. Offset is a DC error per sub-ADC which becomes periodic with time-interleaving. Therefore, the offset-mismatch is periodic with period *MTs* and independent of the input signal. In the frequency-domain the offset-mismatch appears as tones at frequencies independent of the input frequency and independent of the input amplitude.

Gain Mismatch:

For the discussion about gain-mismatch the gain errors are assumed to be different for each channel, and all other characteristics are the same. The errors also occur with a period of *MTs*, just as offset mismatch, but the errors are amplitude modulated with the input frequency -0. The largest absolute errors occur at the peaks off the input signal.

Timing Mismatch:

For the discussion about timing-mismatch, the timing error, due to clock-skew, is assumed to be different for each channel, and all other characteristics are the same. The errors again occur with a period of *MTs* and are amplitude modulated with the input frequency -0 just as the gain-mismatch. The largest errors occur at the largest slew-rate of the sine wave.

III. PROPOSED METHODOLOGY

The proposed TI-ADC mismatch calibration methodology is explained below.

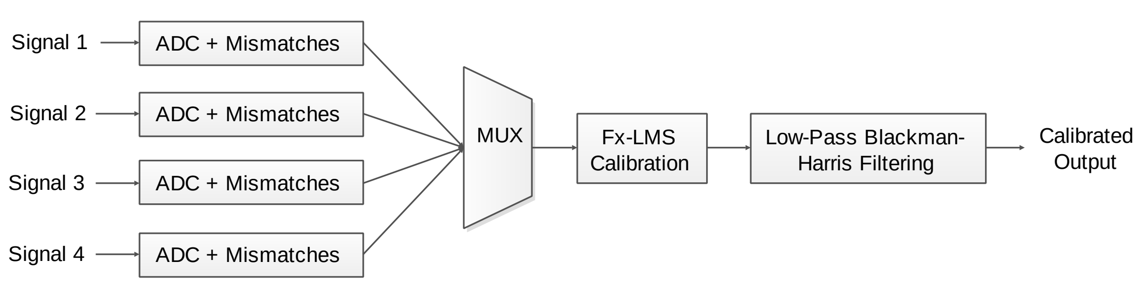

Fig. 3.1 Block Diagram of The Proposed Methodology

The block diagram of the proposed system is shown in Fig. 3.1. Here we have used 4-Channel TI-ADC system with multiplexer followed by calibration techniques first is Fx-LMS followed by Low Pass Blackman-Harris Filter.

Above system is implemented on the simulation tool and the program flow of algorithm is shown in Fig. 3.2 with the help of Flow chart.

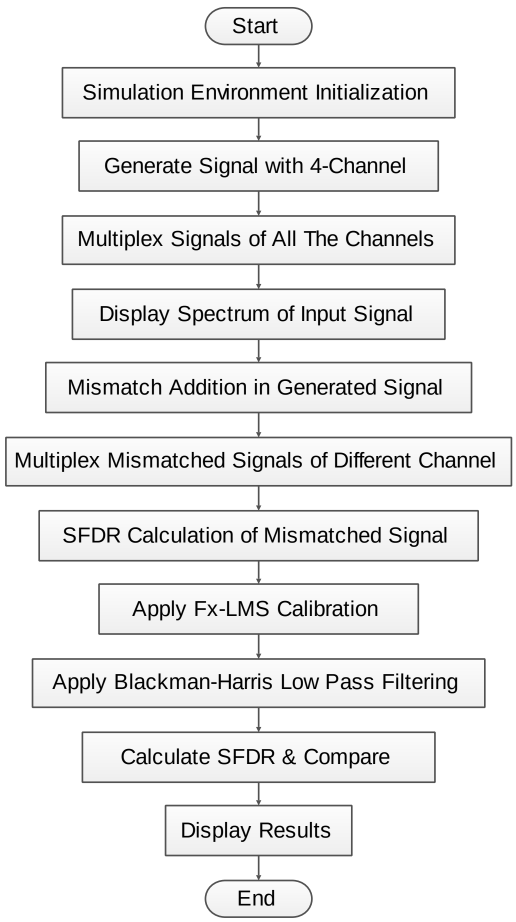

Fig. 3.2 Flow Chart of The Proposed Methodology

The above flow chart is showing step by step executing of the computer algorithm.

IV. SIMULATION RESULTS

The simulation results are shown in the below figures. The comparison of the system performance is shown in table below.

Table I: SFDR Comparison

Methodology	SFDR (dB)
Proposed Methodology	78.76 dB
Previous Work	77.50 dB

From the above table it is clear that the spurious free dynamic range (SFDR) for the proposed approach is better than the previous work.

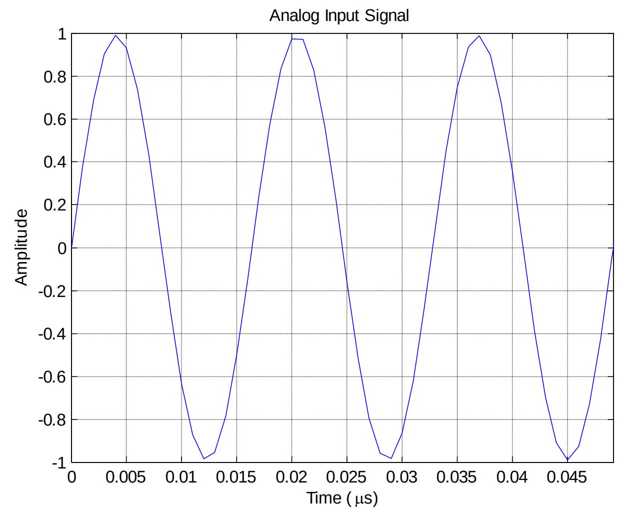

Fig. 4.1 Input Analog Signal

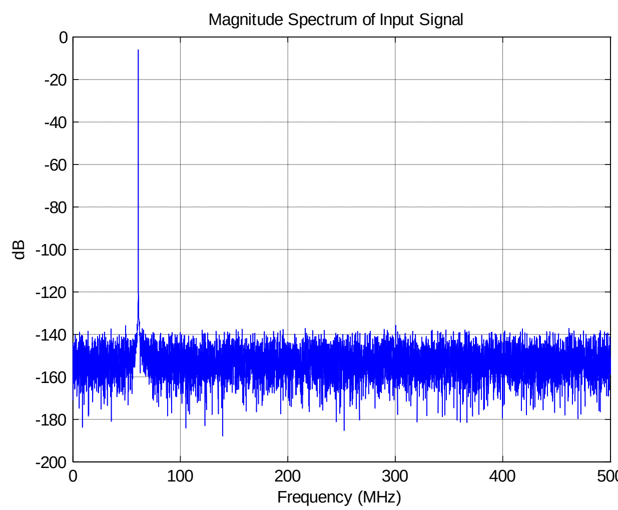

Fig. 4.2 Magnitude Spectrum of Input Signal without mismatches

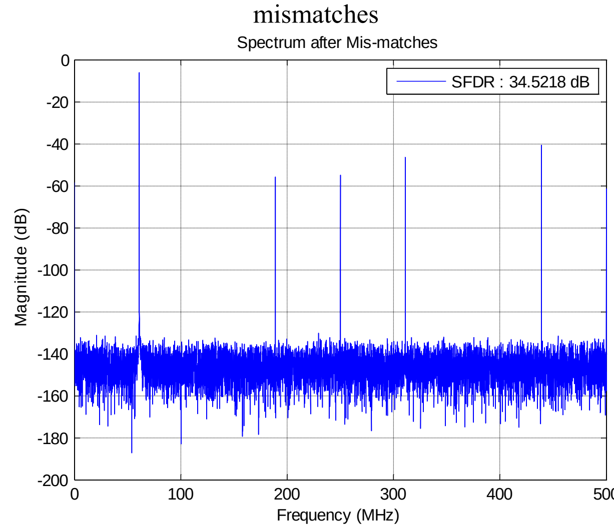

Fig. 4.3 Magnitude Spectrum of Input Signal with mismatches

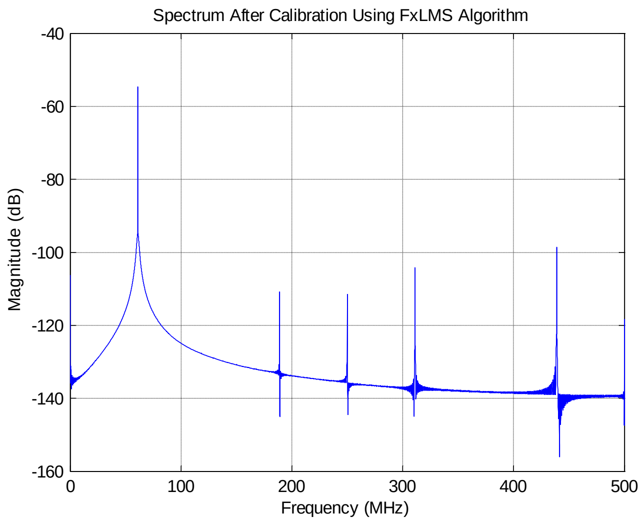

Fig. 4.4 Magnitude Spectrum of Calibrated Signal using Fx-LMS Algorithm

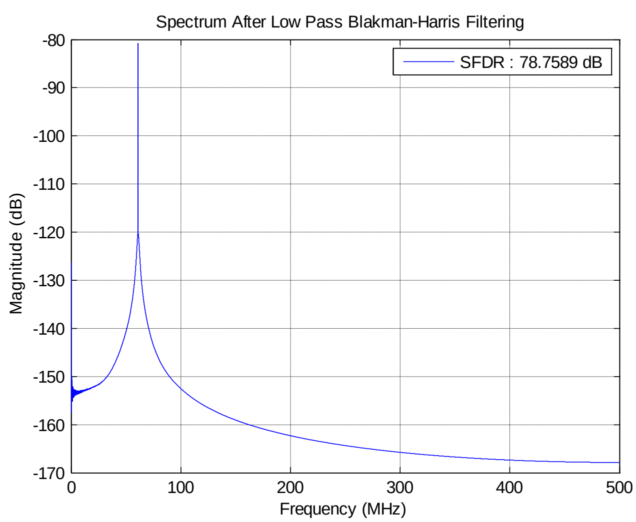

Fig. 4.5 Magnitude Spectrum of Final Output Calibrated Signal using Low pass Blackman Harris Filtering

V. CONCLUSION AND FUTURE SCOPE

The time interleaved analog to digital converter system is proposed in this paper has the optimized version of the calibration structure than the previous methodologies. Our approach is simplified version and has two stages only. first one is filtered least mean square algorithm which is a kind of feedback system and further mismatched calibrated with the utilization of the low pass Blackman-Harris filter. From whole discussion the proposed approach proved to be good for futuristic TI-ADC systems and as well also shown the different direction of non-complex calibration structure. Such approach also perform better with the utilization of filter banks and other series techniques which will make system little bit complex but offer better performance.

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