An Optimized VLSI Architecture of Manchester Encoding Using Efficient Similarity Oriented Logic Simplification Scheme

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Abstract - In this paper the work pointing towards the consumption of power and speed of the system to generated Manchester or FM0 encoding using Similarity Oriented Logic Simplification Scheme. Here the Similarity Oriented Logic Simplification Scheme is modified to increase the system calculation speed and to reduce the consumption of power. The power consumption is 21mW and frequency of the system is 355.413MHz.

Keywords - FPGA, Similarity Oriented Logic Simplification Scheme, Frequency, Fast Calculations, Power Optimization, DSRC System.

I. INTRODUCTION

In the past five years there has been an explosive growth in the demand for portable computation and communication devices, from portable telephones to sophisticated portable multimedia terminals. This interest in portable devices has fueled the development of low-power signal processors and algorithms, as well as the development of low-power general purpose processors. In the digital signal processing area, the results of this attention to power are quite remarkable. Designers have been able to reduce the energy requirements of particular functions, such as video compression, by several orders of magnitude. This reduction has come as a result of focusing on the power dissipation at all levels of the design process, from algorithm design to the detailed implementation. In the general purpose processor area, however, there has been little work done to understand how to design energy efficient processors. This thesis is a start atbridging this gap and explores power and performance tradeoffs in the design and implementation of energy-efficient processors.

Performance of processors has been growing at an exponential rate, doubling every 18 to24 months, as is shown in Figure 1.1. The bad news is that the power dissipated by these processors has also been growing exponentially, as is shown in Figure 1.2. Although the rate of growth of power is perhaps not quite as fast as the performance curve, it still has led to processors which dissipated more than 50W [4]. Such high power levels make cooling these processors difficult and expensive. If this trend continues processors will soon dissipate hundreds of watts, which is unacceptable in most systems. Thus there is great interest in understanding how to continue increasing performance without also increasing power dissipation.

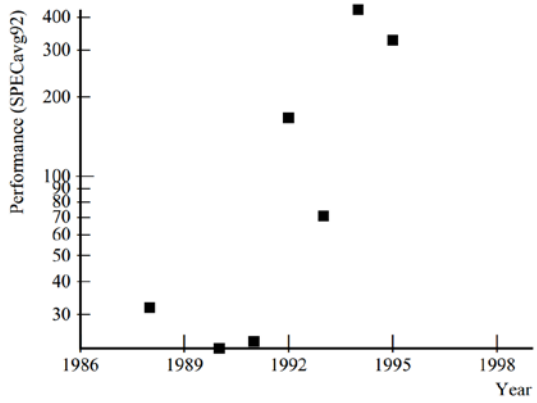


Figure 1.1: Evolution of processor performance.

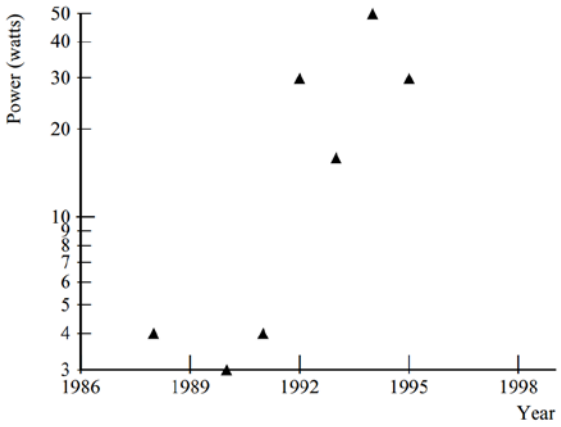


Figure 1.2: Evolution of processor power

For portable applications the problem is even more severe since battery life depends on the power dissipation. Lithium-ion batteries have an energy density of approximately 100Wh/Kg, the highest available today [5]. To operate a 50W processor for 4 hours requires a 2Kg battery, hardly a portable device.

To address this problem processors manufacturers have introduced a variety of low-power chips. The problem with these processors is that they tend to have poor performance, as is shown in Figure 1.3. Thisfigure plots on the Y-axis performance, measured as the average of SPECint92 and SPECfp92 [6], and on the X-axis energy, measured as watt/SPEC.

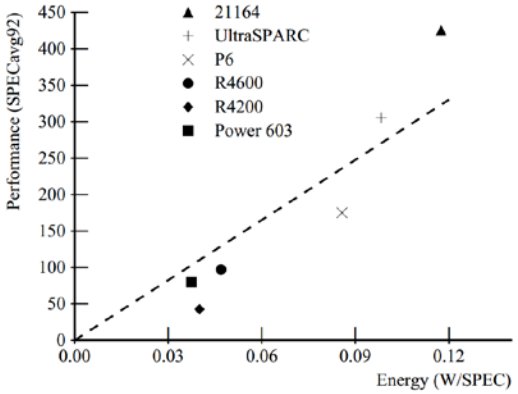


Figure 1.3: Performance and energy of processors.

II. SYSTEM MODEL

Energy Dissipation in CMOS Circuits

There are three sources of energy dissipation in CMOS circuits; dynamic energy, static energy, and short-circuit energy. A simple CMOS gate consists of two transistors,represented as a resistor and a switch, connected to a fixed output load capacitance and aconstant voltage source, as shown in Figure 2.1. Dynamic energy is due to the charging and discharging of the load capacitance. If the output node is originally at ground and assuming that it swings full rail, then an amount of energy equal to CV^2 is drawn from the voltage source on a low to high transition. Of this amount, $1/2CV^2$ is dissipated in the ptransistor to charge the load capacitance and $1/2CV^2$is stored in the capacitor itself. The stored energy is dissipated in the n-transistor to discharge the load. Thus $1/2CV^2$is dissipated on each transition. The circuit only dissipates dynamic energy when it is active or switching. If the output node remains at a fixed voltage level, then no energy is dissipated. Most nodes in CMOS circuits transition only infrequently; therefore the energy per cycle is usually written as,

$$E = \frac{nCV^2}{2}$$

where*n* is the number of transitions during the period of interest. If the circuit is synchronous and clocked at a frequency *f* then the average power can be written as,

$$P = aCV^2f$$

where a is the probability of a transition at the output node divided by 2. If a node transitions every cycle then a=0.5.

Static energy is due to resistive paths between the supply and ground. The two main sources of static energy are analog or analog-like circuits which require constant current sources, and leakage current. Although there is some leakage current through the reverse biased diode between the source/drain and the bulk, the more important component is leakage through the channel when the transistor is nominally off [7].

Low-Power Metrics

When optimizing a design for low power it is necessary to have a metric that can be used to compare different alternatives. The most obvious choice is power, measured in watts. Power is the rate of energy use, or $P=dE/dT$. A more useful definition, however, is average power, or the energy spent to perform a particular operation divided by the time taken to perform the operation $P_{avg}=E_{op}/T_{op}$. How to define the operation of interest is arbitrary and depends on what is being compared. In the case of a processor, it could be the energy to run a benchmark to completion or the energy to execute an instruction—as long as all processors compared execute the same instructions.

Power is important for two reasons. The first is that it determines what kind of package can be used for the chip. For example, a small plastic package, the cheapest form of packaging, can only dissipate a few watts. A processor which dissipates more than that

will have to be sold in a more expensive package. The second reason power is important isbecause it limits how long the system battery will last. But power as a metric of "goodness" of low-power designs has some drawbacks. The most important drawback is that power is proportional to the operation rate, so one can reduce the power by slowing down the system. In CMOS circuits this is very easy to do, one simply reduces the clock frequency.

Low-Power Design Techniques

From below Equation one simple way to reduce the energy per operation is to lower the power-supply voltage. However, since both capacitance and threshold voltage areconstant, the speed of the basic gates will also decrease with this voltage scaling. The delay of a CMOS gate can be modeled as the time required to discharge the output capacitance by the transistor current, *Tg = CV/I*. Using the current model presented by [10] this gives,

$$T_g = K\frac{V}{(V - V_{th})\propto}$$

where α is the velocity saturation coefficient and K is a technology specific constant. When transistors are not velocity saturated α=2.0 and the equation reduces to the quadratic model for transistor current. As transistors become more velocity saturated α decreases towards one. For typical 0.25µm technologies α=1.3-1.5.

III. PROPOSED ARCHITECTURE

To enhance the signal reliability in communication system the signal needs to be encoded before transmission. But FM0 and Manchester encoding reduces the performance of the VLSI architecture to maintain diversity in encoding. To overcome this problem the architecture is optimized using Similarity Oriented Logic Simplification Schemetechnique in the previous researches, and now further optimizing in this paper using modified Similarity Oriented Logic Simplification Schemetechnique. The modified architecture of the system significantlyreduce the power utilization and speed up the calculation as circuit works on higher frequency.

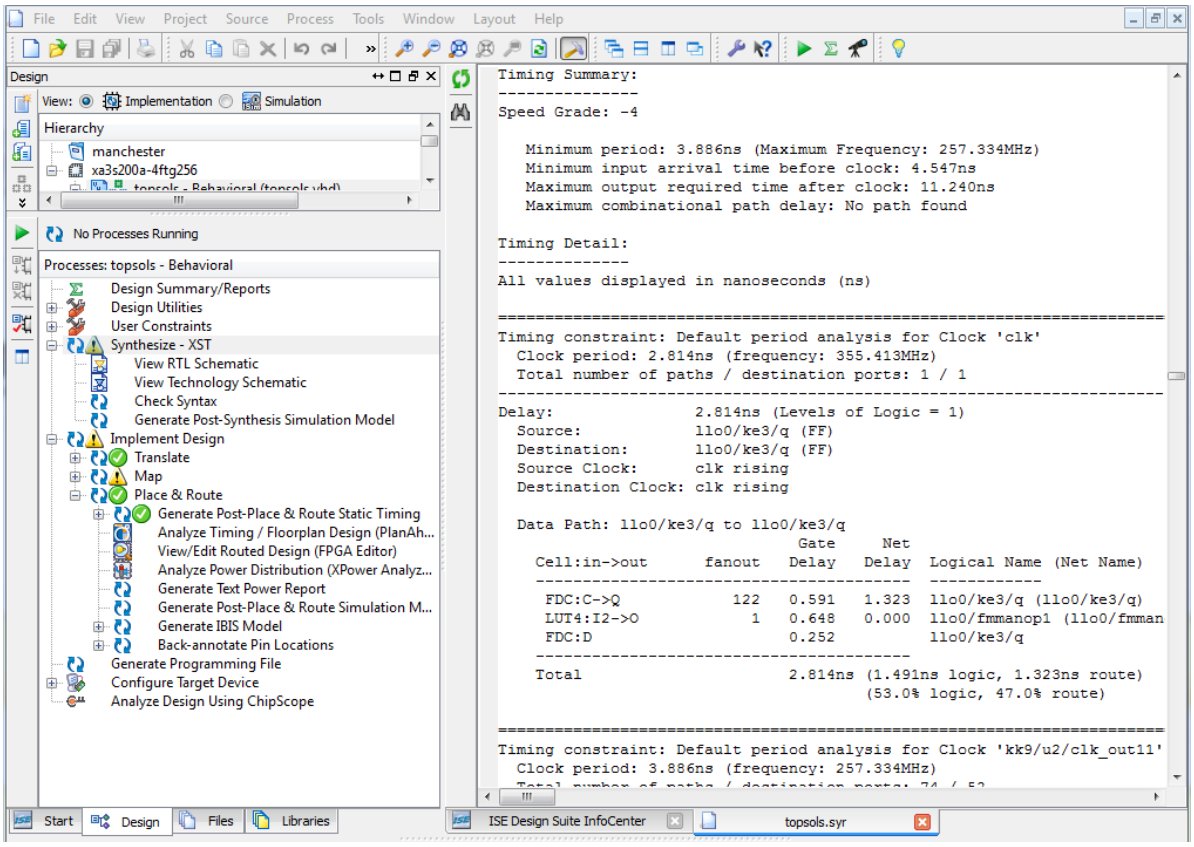


Fig.3.1. User Interfaceof XILINX ISE

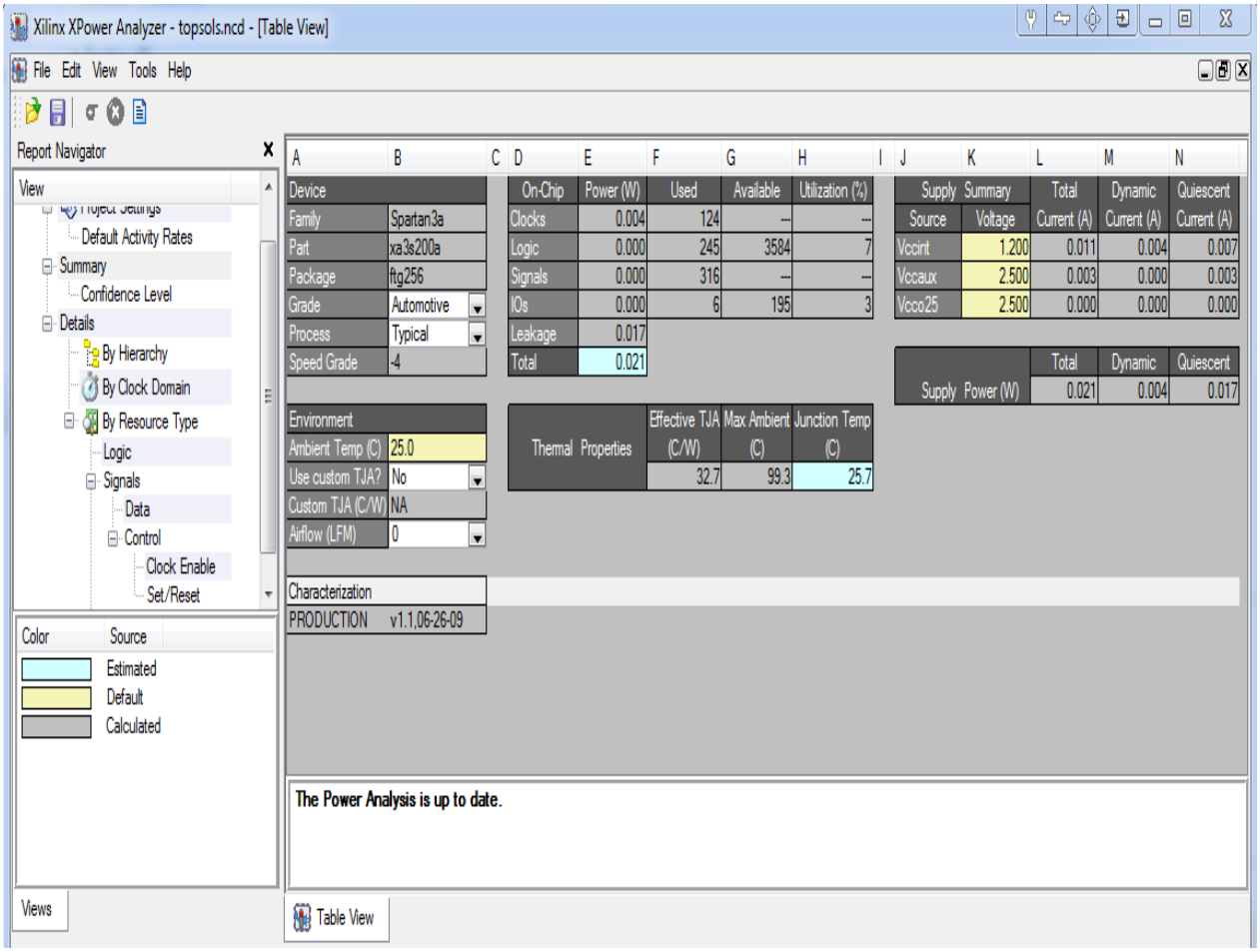


Fig.3.2. User Interface of X Power Analyzer

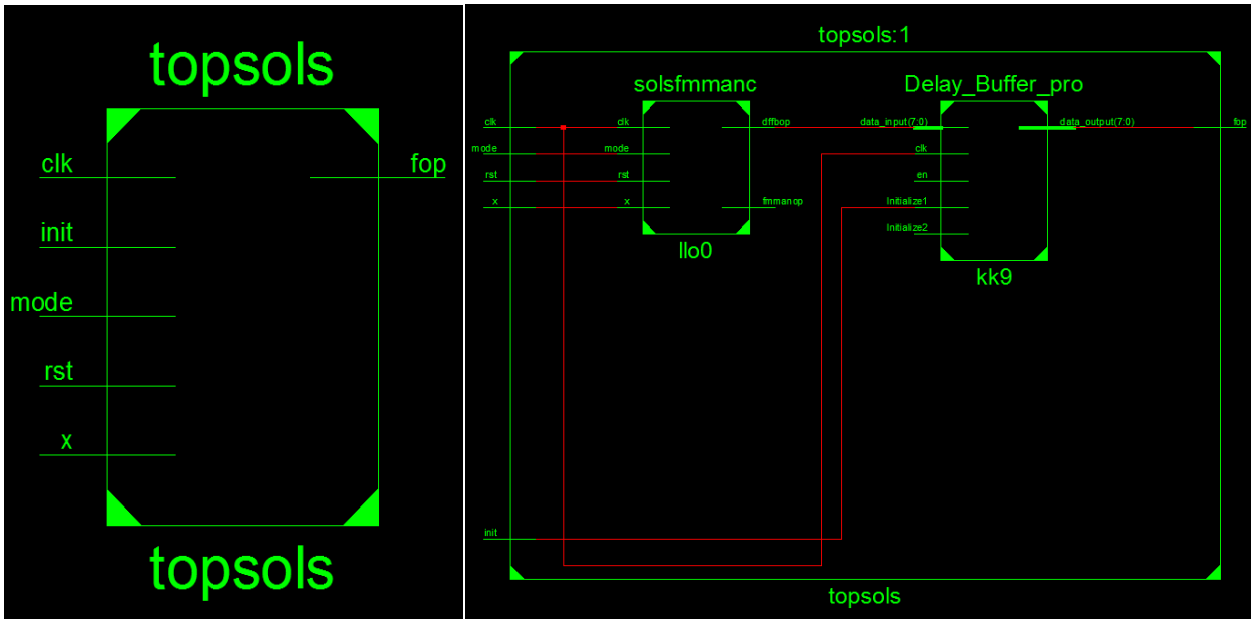


Fig.3.3. Top Module of Proposed Architecture (SOLS FM/Manchester and Delay Buffer)

Synthesis Outcomes

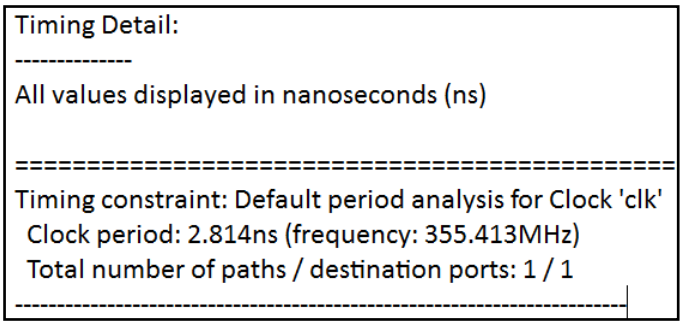
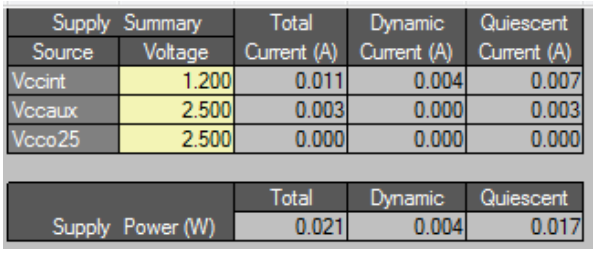


Fig.3.4. Frequency of the proposed architecture355.413MHz



Supply Summary Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.011	0.004	0.007
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.000	0.000	0.000

	Total	Dynamic	Quiescent
Supply Power (W)	0.021	0.004	0.017

Fig.3.5 Power Consumption of Proposed Architecture 21mW

Table 1: Comparison of Parameters

System	Device Utilization	Power Consumption	Frequency
Proposed System	Spartan 3	21mW	301.445 MHz
Existing System	Spartan 2	28.30 mW	296 MHz
Improvements		25.7%	20.07%

IV. CONCLUSION AND FUTURE SCOPE

The proposed system is analyzed and synthesized in the XILINX which shows different outcomes of the architecture tested. The proposed architecture is optimized to speed up the system and consume less power than the previous system. The frequency and power consumption is better than the previous system which is explained in the Table 1 in previous section of the paper. Here the proposed system has 20.07% improvements and 25.7% improvements in frequency and power respectively.

REFERENCES

[1] Y. H. Lee and C. W. Pan, "Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 1, pp. 18-29, Jan. 2015.

[2] J. F. Huang, Y. J. Jiangn and R. Y. Liu, "The RF receiver front-end chip design with the transformer balun for DSRC applications," VLSI Design, Automation and Test (VLSI-DAT), 2011 International Symposium on, Hsinchu, 2011, pp. 1-4.

[3] Hung-Wen Lin, Jin-Yi Lin and Min-Tai Chuang, "A low-area digitalized channel selection filter for DSRC system," VLSI Design, Automation and Test (VLSI-DAT), 2014 International Symposium on, Hsinchu, 2014, pp. 1-4.

[4] P. Benabes, A. Gauthier, and J. Oksman, “A Manchester code generator running at 1 GHz,” in Proc. IEEE, Int. Conf. Electron., Circuits Syst., vol. 3. Dec. 2003, pp. 1156–1159.

[5] A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, “A 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz,” in Proc. 16th Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1–4.

[6] Y.-C. Hung, M.-M.Kuo, C.-K.Tung, and S.-H. Shieh, “High-speed CMOS chip design for Manchester and Miller encoder,” in Proc. Intell. Inf. Hiding Multimedia Signal Process., Sep. 2009, pp. 538–541.

[7] M. A. Khan, M. Sharma, and P. R. Brahmanandha, “FSM based Manchester encoder for UHF RFID tag emulator,” in Proc. Int. Conf. Comput., Commun. Netw., Dec. 2008, pp. 1–6.

[8] M. A. Khan, M. Sharma, and P. R. Brahmanandha, “FSM based FM0 and Miller encoder for UHF RFID tag emulator,” in Proc. IEEE Adv. Comput. Conf., Mar. 2009, pp. 1317–1322.

[9] J.-H. Deng, F.-C.Hsiao, and Y.-H. Lin, “Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels,” in Proc. Adv. Commun. Technol. Jan. 2013, pp. 98–103.

[10] I.-M. Liu, T.-H.Liu, H. Zhou, and A. Aziz, “Simultaneous PTL buffer insertion and sizing for minimizing Elmore delay,” in Proc. Int. Workshop Logic Synth., May 1998, pp. 162–168.

[11] H. Zhou and A. Aziz, “Buffer minimization in pass transistor logic,” IEEE Trans. Comput.Aided Des.Integr. Circuits Syst., vol. 20, no. 5, pp. 693–697, May 2001.

[12] N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, 2nd ed., Upper Saddle River, NJ, USA: Pearson Educ. Ltd., 1993, pp. 98–103.