Design and Simulation of Semiconductor Memory EDAC using Decimal Matrix Code

Heena Saravgi[1]

[1]*M.tech Student, RITS, RGPV, Bhopal, Madhya Pradesh, India*

Abstract—When memories are exposed to radiation environment, Multiple cells upsets (MCUs) is an important issue regarding the reliability of memories. In such case to protect data from radiations and transient a number of techniques are available. However, memories can be protected from a limited variation of radiations through the proper packaging. In the present scenario of wireless communication, devices are exposed to a vast range of environmental radiation for the various numbers of applications. Hence many additional data preservation technique are utilised to authenticating the data before it is processed. The most common technique for the encoded data is error correction codes (ECCs). The data is then stored in memories after the encoded process. The preferred implementation technique is error correction code as this method requires minimized delay overhead in data correction and a less number of redundant bits to be stored. In this paper the simple decimal addition algorithm is used for memory data error detection and correction code. The encoded data then is to be stored in memory and the implementation is based on FPGA. The preferred code for decoding of the data for error detection and correction is Hamming Code. This technique used a divide-symbol concept to represent the linear data in groups to make symbolic code and the length of the symbol is inversely proportional to the delay overhead of the code.

Index Terms— Decimal Adder, Error Correction Codes, Error Syndrome, Multiple Cell Upsets (MCUs) , Semiconductor Hardware Memory.

I. INTRODUCTION

The reason behind rapidly increasing soft error rate in memory cells today is the space environment radiation that affects the memories in the electronics system. The other factors that also affect the soft error rate is the number of transistors per area is increasing day by day as the CMOS technology scale down to deep nanoscale technology also the increasing size of embedded memories in electronic systems affects the soft error rate. The data is stored in the form of charge in memory cell and this data can be affected by the ionized character of exposed radiation and this led to the soft error rate in the memories. The phenomena of error generation due to radiation in the memories that are exposed to the environmental radiations are shown with the help of memory block in Fig. 1.

The single bit data error in memory is a serious reliability concern but in some cases multiple bit errors /upsets of MCUs are becomes the major concern. The error correction codes (ECCs) may be utilized for finding the faults coming in the memory up to the maximum possible extent. Many error correction codes were suggested by various researchers and they have been widely used for many years. The data that is to be stored in fault tolerant memory architecture is first encoded to generate redundant bits with the help of encoder circuit.

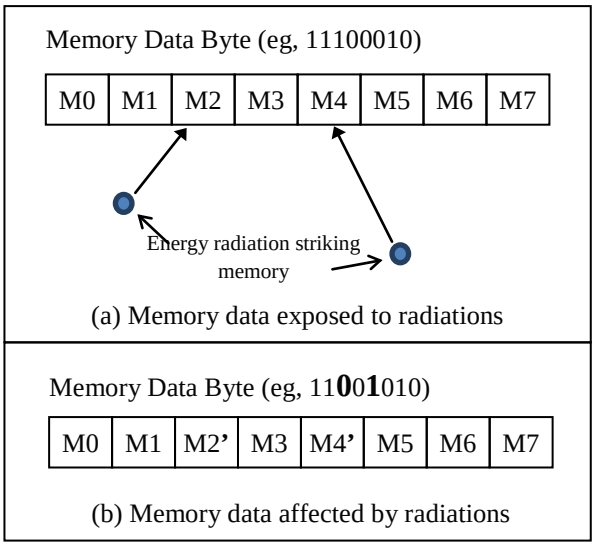

Fig. 1 Soft Error in semiconductormemory due to exposure to radiation

The data and the redundant bites are then stored to memory with the help of memory interface circuit. These redundant bits are then used from the memory by the decoder for correcting the errors. A small number of the most reliable codes include Bose-Choudhary-Hocquenghem (BCH) code, Reed-Solomon (RS) code and Punctured Difference Set (PDS) code. These codes handle the MCUs in memories. The physical re-arrangement of cells to separate the bits into different physical words from the same logical word is the way to retain MCUs and this technique is known as interleaving. The tight coupling hardware architecture from both cells and comparison circuit structure might not practically allow interleaving to be effectively used with content-addressable memory (CAM). The proposed 2-D matrix code can be utilized efficiently to correct the MCUs per word. One word is divided into multiple columns and multiple rows in 2-D matrix code, where the bits per row are protected by

Hamming Code and the bits per column are protected by parity code. The errors detected by Hamming code are corrected by the vertical syndrome bits code if the error is in two bits.The 2-D MC is capable of correcting only two errors in all cases. This code has a benefit as compared to other codes as this has a lower delay overhead. The proposed technique in this paper is novel decimal matrix code. The divide-symbol is used for the proposed code to provide enhanced memory reliability. The proposed DMC utilizes decimal integer addition (decimal algorithm) on the divided symbols of binary code. A logic comparator is used in the proposed work to find the error syndrome bits to detect and correct error in the decoder. The decimal algorithm enhances the reliability of the error detection capability of the code.

The rest of this paper is arranged as follows: section-II presents the work published by some recent scholars under the title 'Literature Review.Section-III presents the proposed design of DMC Encoder and Decoder. The simulation and synthesis based results and comparative analysis of the proposed designs are given in section-IV. Finally the conclusion based on the proposed work is discussed in section-V.

II. SYSTEM MODEL

A simple block diagram of the fault tolerant memory encoder implementation is shown in fig. 2.

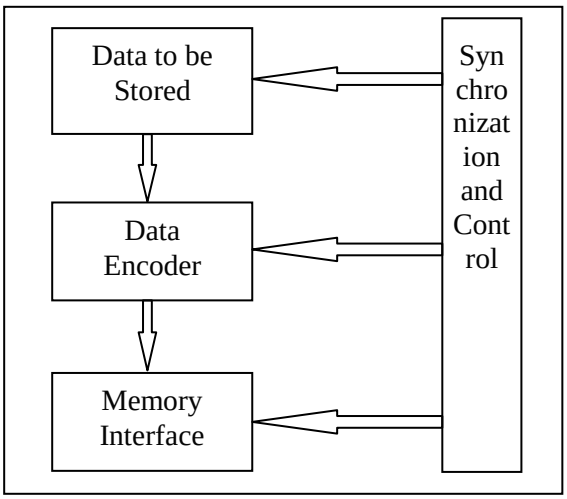

Fig. 2 A simple data encoder block diagram

It is clear from the above figure that the data is to be stored is first encoded to generate the redundant bits with the help of encoder circuit and with the help of memory interface the data and the redundant bites are stored in the memory. Decoder uses these redundant bits for correcting the errors from the memory data.

III. PREVIOUS WORK

In [1] a novel per-word DMC was proposed to utilize the decimal algorithm to provide the guarantee and the consistency of memory to detect errors, so that detection and correction or more errors may be possible. Various alternatives are also employed to overcome reliability issue of radiation exposed memories in reference [2] which gives acomparative study of various error correction codes.In Reference [3] and [4] hamming code is proposed for a high reliability decimal code for implementation of error correction technique. Reference [5] gives a mechanism for: (i) single error correction, double error detection, triple-adjacent error detection using hamming code, and (ii) single error correction, double error detection, double adjacent error correction Codes. These are derived from Orthogonal Latin Square Codes. A CAM data protection scheme using DMC is proposed in [6, 9, 11, 12, 14, and 15] decimal algorithm for protection code; as a result further errors were detected and corrected. The protection level against large MCUs in memory is better chandelled by the proposed algorithm. In reference [7] two Error Correction Codes are used such as Parity Matrix Code (PMC) and Decimal Matrix Code (DMC). To obtain the maximum error detection capability the decimal algorithm uses DMC. In reference [8] a new methodology for error detection and correction to realize fault-tolerant memory cells, Error Correction Codes (ECCs) are used, but the requirement of such codes is more power, area, and higher delay overhead. In reference [10] the design of HMC is proposed for which a hybrid matrix code improved memory consistency against multiple cell upsets. Less number of redundant bits is required for security as compared to accessible approaches. In reference [13] proposed a prevention technique to protect the memories from the MCUs that is decimal code matrix. In the proposed method for detection and correction of errors in the memories and maintaining memory reliability the 128 bit Decimal Matrix code are used. In reference [16] to assurance the dependability of the memory the author uses the HMC (Hybrid Matrix Code). In order to keep the reliability high the hybrid matrix code employs more number of redundant bits is the main disadvantage of this technique. In reference [17] the technique used for memory protection and detection for multiple MCUs is DMC with the help of encoder technique. Reference [18] proposed DMC which provides a competent error correction code in which the dependability and security of the memory is improved.

IV. PROPOSED DESIGN OF DECIMAL MATRIX CODE ENCODER AND DECODER

The work proposed in this paper implements the DMC encoder that follows the division of 128 bit data and then the data is encoded to generate the redundant bits. The

architecture for encoder of fault-tolerant memory that is proposed in work is depicted in Fig. 3.

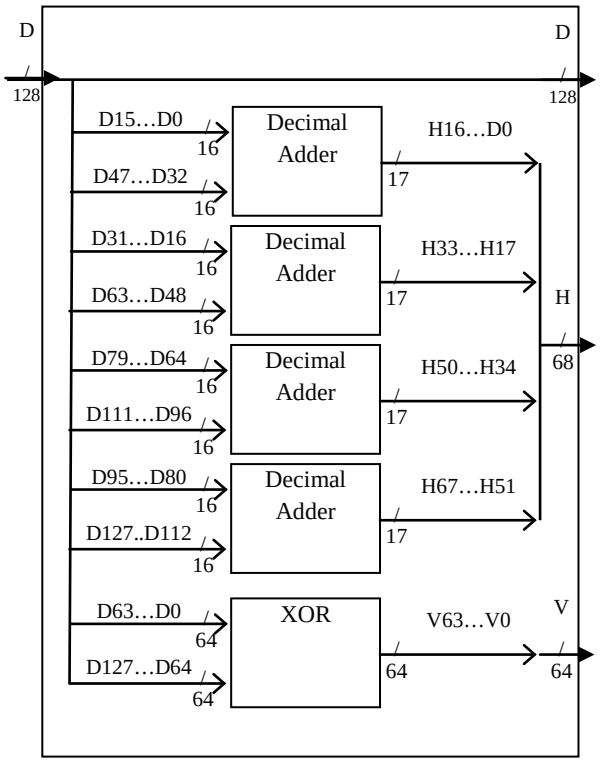

Fig. 3: Proposed 128-bit Architecture of DMC Encoder

To generate the horizontal redundant bits of selected symbols per row of each m-bit symbol are performed by using the decimal integer addition. To perform decimal addition each symbol is considered as a decimal integer. To obtain the vertical redundant bits Parity generation operation is to be performed among the bits of the column. There is no need to change the physical structure of the memory for the proposed DMC; here the steps are implemented in logical form. While performing the encoding process on the 128-bits data, the data from D128....D0 are arranged in a matrix of 2 rows and 4 columns and considered as symbol of 16 bit data. To obtain the horizontal and vertical redundant bits the equations that are implemented are shown as follows:

Equations for generating vertical bits

V0 = D0 xor D64

V1 = D1 xor D65

V2 = D2 xor D66

: : :

: : :

: : :

V62 = D14 xor D126

V63 = D15 xor D127

Equations for generating horizontal bits

$H_{16}…H_0 = D_{47}…D_{32} + D_{15}…D_0$

$H_{33}…H_{17} = D_{63}…D_{48} + D_{31}…D_{16}$

$H_{50}…H_{34} = D_{111}…D_{96} + D_{79}…D_{64}$

$H_{67}…H_{51} = D_{127}…D_{112} + D_{95}…D_{80}$

The encoder provides the vertical redundant bit V and horizontal redundant bit H. The DMC encoded codeword consist of D, H and V. The code word generated after the process is stored in the Memory.

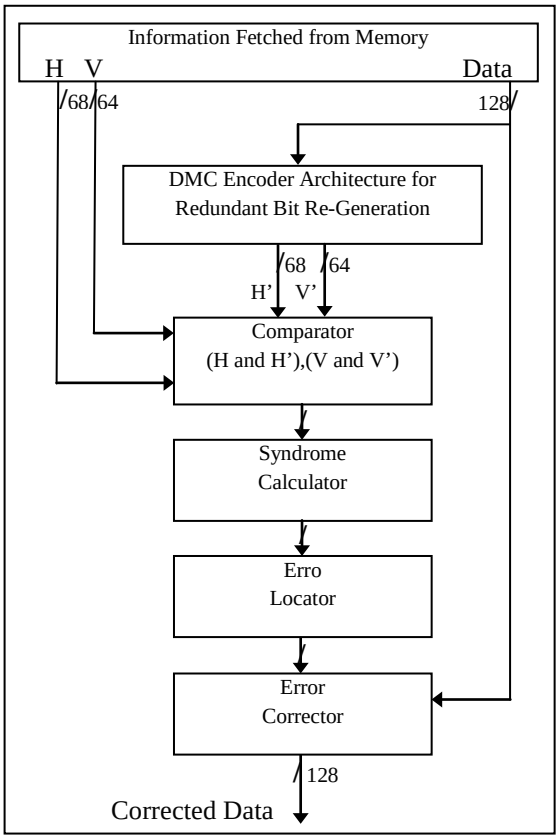

Fig. 4 Architecture of Decimal Matrix Decoder

The decoder is implemented to correct the errors which are introduced by the use of MCUs in memory. The redundant bits of the decoder are generated by the data bits that are stored in the memory location. If the data in the memory location is represented as D then the redundant bits by the decoder are represented by H' and V'. Now the syndrome bits are generated by the stored redundant bits (H and V) and the generated redundant bits (H' and V'), then the data which is fetched from memory if have some error are corrected and the syndrome bits are used as to detect the

error location on memory. The architecture of the proposed decoder is shown in fig. 4.

In the proposed work to generate the syndrome bits the logical comparator using XOR gate is used .The equations that are implemented to obtain the horizontal and vertical syndrome bits are shown as follows:

$$V_{syn} = V \text{ xor } V'$$

$$H_{syn} = H \text{ xor } H'$$

The error in the stored data can be detected if any bit or bits of Hsyn or Vsyn is non-zero. The horizontal and vertical syndrome bits are grouped with the same length as that of horizontal and vertical redundant bits to locate the symbol that contains error. The grouped data bits are shown in Fig. 5.

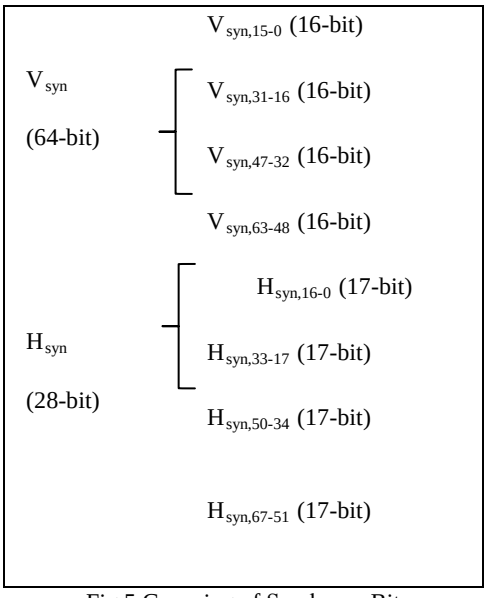

Fig 5.Grouping of Syndrome Bit

After looking for the common symbol in the data matrix from the non-zero syndrome horizontal and vertical symbols the error location in the data matrix can be identified. Once we get the location of the error, this error can be rectified later by error corrector logic by performing the bit inversion.

IV. Simulation and Synthesis Results

The Xilinx tool is used to perform the simulation result in this work. The Block Diagram and the RTL Schematic diagrams of Encoder and Decoder designs are shown in Fig. 6 and Fig. 7 respectively

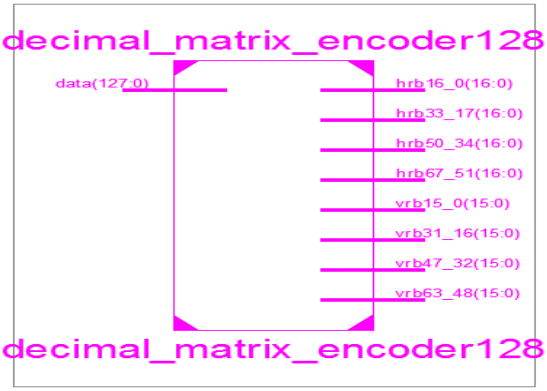

Fig. 6 RTL Block Diagram of DMC Encoder

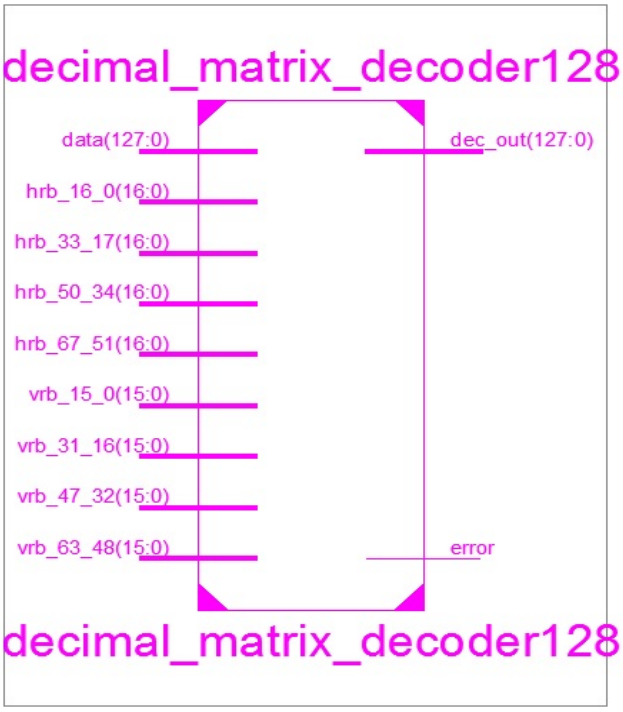

Fig. 7 RTL Block Diagram of DMC Decoder

The hardware utilization summary based on the FPGA for the proposed Encoder and Decoder are shown in Table-I and Table-II respectively.

Table 1: Hardware Utilization Summary of 128-bit DMC Encoder

Spartan-3E XC6SLX100-3FGG676	*Total*	*128-bit DMC Encoder*	
		Used	*%*
Slices	15822	40	1
LUTs 4-Inputs	63288	96	1
Bonded IOBs	480	260	54
Slice register	126,576	4	1

Table 2: Hardware Utilization Summary Of 128-Bit Dmc Decoder

Spartan-3E XC6SLX100-3FGG676	*Total*	*128-bit DMC Decoder*	
		Used	*%*
Slices	4656	138	1
LUTs 4-Inputs	9312	270	1

Spartan-3E XC6SLX100-	*Total*	*128-bit DMC Decoder*	
Bonded IOBs	158	389	81
Slice register	126,576	4	1

The Testbench based simulation waveform of present encoder design is shown in Fig. 7.

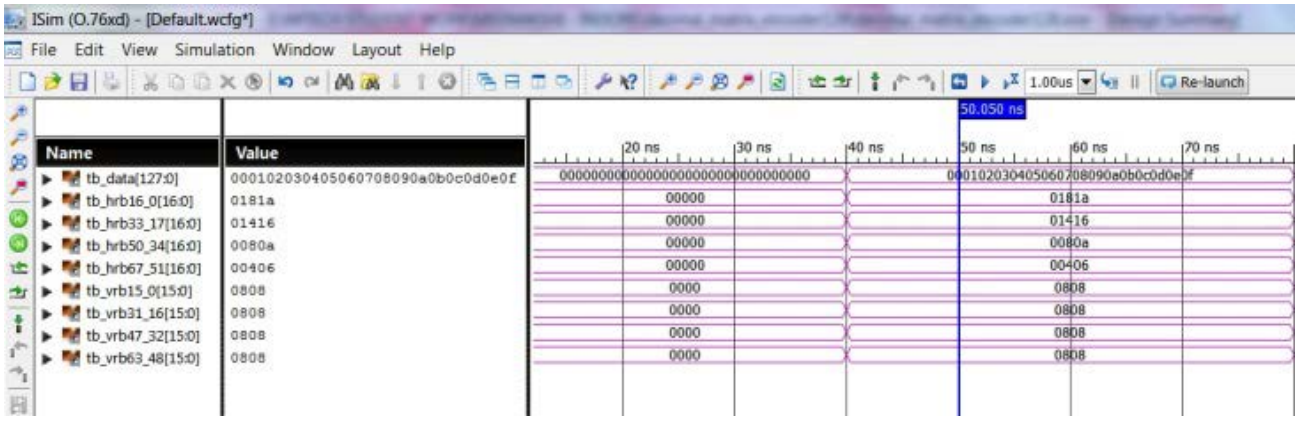

Fig. 8 Simulation of Proposed 128-bit Encoder

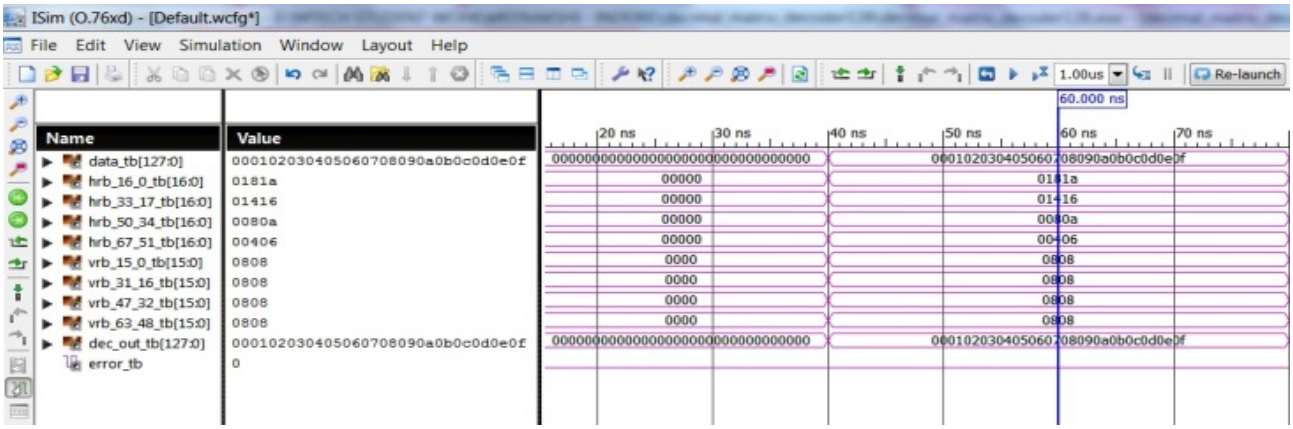

Fig. 9 Simulation of Proposed 128-bit Decoder (without data error)

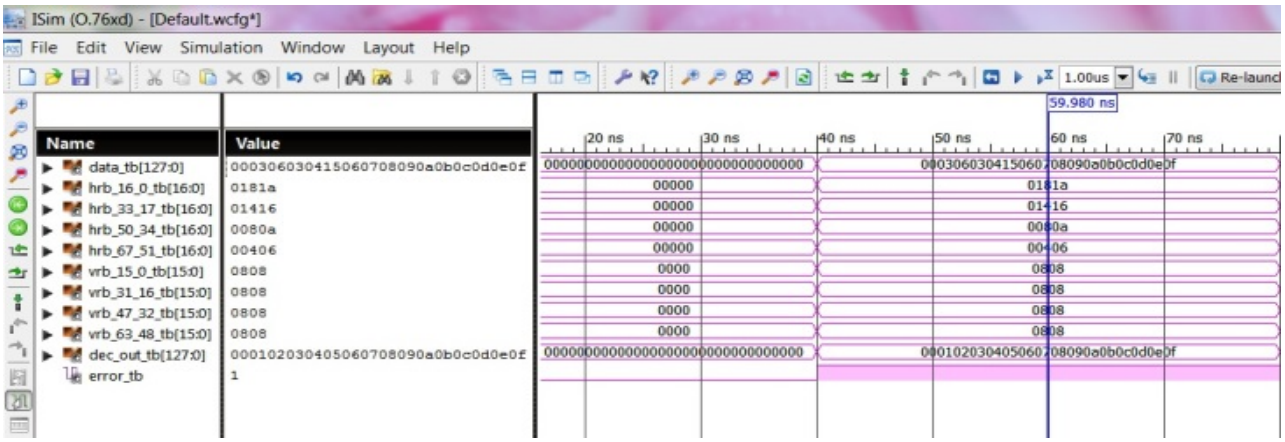

Fig. 10 Simulation of Proposed 128-bit Decoder (with data error detection and correction)

VI. CONCLUSION

In this proposed paper a 128-bit word is encoded and decoded to assure reliability and to show the presence of MCUs with the reduced performance overheads as an example to support the proposed methodology. As to perform the encoding process firstly we provide the information bits D to the DMC encoder and after that the vertically redundant and horizontally redundant bits V,H respectively are received from DMC encoder, after this the decoding process gives us the corrected words Fig 4 shows the proposed DMC decoder. In order to minimize the circuit area (ERT) of DMC encoder can be reused to achieve the desired output. This process hence without creating any disturbance to the encoding and decoding process successfully reduces the overhead area of DMC. To perform this process uses the syndrome bits in the DMC decoder.. As a result the whole circuit area of DMC can be minimized with the help of the existing encoder circuit and this shows how the area overhead of extra circuits can be significantly reduced.

VII. FUTURE SCOPE

The proposed work will be designed and simulated using Xilinx ISE Design Tool for VHDL design entry and Xilinx ISIM for hardware performance simulation for functional verification. A Hardware utilization summary will be proposed for various Xilinx Field Programmable Gate Array Devices to analyze the percentage utilization of hardware of the proposed ALU design. The dynamic power consumption of the proposed design for the simulated hardware will also be carried out using Xilinx Power Tool to present power performance of the proposed work.

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