A Fast-Locking Digital PLL: Using Integrated and Differentiator Controlling Using Matlab

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Abstract— In this paper we are using new method called "A fast–locking digital DPLL using integrator and diffentiator controlling with Matlab. This method reduces the locking Time and improves performance of DPLL. In the Previous method the fast locking DPLL operation Reduces the lock time by a factor about 4.40 Compared to its conventional DPLL counterpart. But this method more effective to reduce locking time with few nano second. It has less computational complexity compare to the previous method.

Keywords-DPLL, fast-locking phase tracking, lock time, HPF, LPF, CP.

I. INTRODUCTION

A phase-locked loop is a feedback control system that generates an output signal whose phase is related to the phase of an input "reference" signal. It is an electronic circuit consisting of a voltage controlled oscillator and a phase/frequency detector. This circuit compares the phase of the input signal with the phase of the signal derived from its feedback generated by its output oscillator and adjusts the frequency of its oscillator to keep the input and output signal phases matched. The signal from the phase detector is used to control the oscillator in a feedback loop [5]. A digital Phase-locked loop is also feedback system that compares the output phase with the reference input phase. The difference is that a digital phase locked loop (DPLL) contains purely digital phase/frequency detector, loop filter and controlled oscillator. A digital phase detector suitable for square wave signals can be made from an exclusive-OR (XOR) logic gate. A Phase-frequency detector is an asynchronous sequential logic circuit originally made of four flip-flops Phase Frequency Detector is used in a PLL application; lock can be achieved even when it is off frequency. Such a detector has the advantage of producing an output even when the two signals being compared different only in phase but in frequency. The phase frequency detector prevents a "false lock" condition in PLL applications, with the wrong phase of the input signal or with the wrong frequency [7]. Phase-locked loop are mostly used in radio, telecommunications, computers and other electronic applications to recover a signal from a noisy communication channel, generate stable frequencies at a multiple of an input frequency etc [8].

II. THEORY OF OPERATION

The block diagram of the digital phase looked loop employing HPF is shown in Fig. 1. The DPLL circuit consists of a phase frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), High Pass Filter (HPF) and a voltage-controlled oscillator (VCO) for fine tuning along with a High pass filter (HPF) .

In the block diagram, the phase frequency detector (PFD) compares the output phase with input phase.

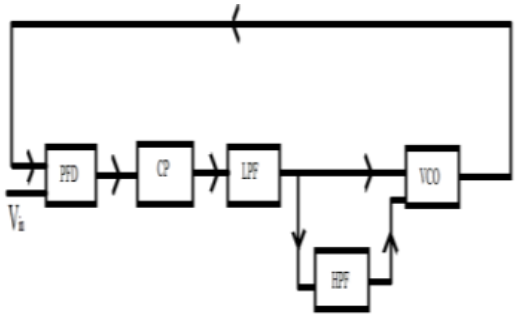


Figure:1 Block Diagram of the DPLL(Employing HPF)

The output of PFD is fed into charge pump and charge pump output fed into Low pass filter (LPF). The LPF suppress the high frequency components from PFD output. The LPF output is fed into Voltage controlled oscillator (VCO) and HPF also. The HPF an active filter consists of resistor and capacitor, works as a differentiator. The HPF generates the difference frequency of LPF by which VCO can be made stable or locked electronic circuit. The VCO has to oscillate the system with the addition of HPF and LPF output frequencies. By using operating frequency f= 1.2GHZ with R= 100Ω and C= 1µf, locking time is 40ns but previous method has 130ns at f=1.2GHZ The locking time is of this new technique is much faster than the previous one and the size of electronic system is also reduced due to use of less electronic circuit.

III. DPLL DESIGN

In this section individual blocks of Fig. 1 has been explained.

A. Phase Frequency Detector (PFD)

The PFD is built using two D flip flops whose output is denoted by U and D respectively. The PFD can be in one of the four states:

1. U = 1, D = 1
2. U = 1, D = 0
3. U = 0, D = 1
4. U = 0, D = 0

Whenever both the flip flops are in a high state, the AND gate will reset both the flip flops, hence the device acts as a tristable device. If PFD generates U signal, the VCO speed up The output from the PFD is given to a charge pump loop filter as shown in figure 2.

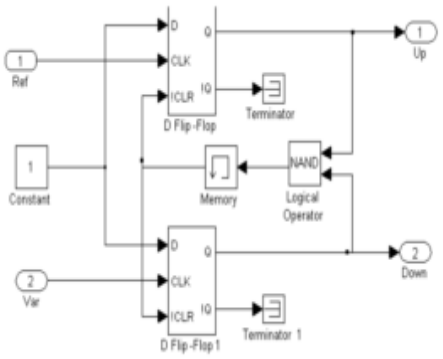


Figure 2 Digital Phase frequency detector

B. Charge Pump and Low pass filter

A charge pump uses capacitors as energy storage element to create either a higher or lower voltage power source. Charge pump circuits are capable of high efficiencies. Charge pumps use some form of switching device(s) to control the connection of voltages to the capacitor. The block diagram of Charge Pump is shown in [12].

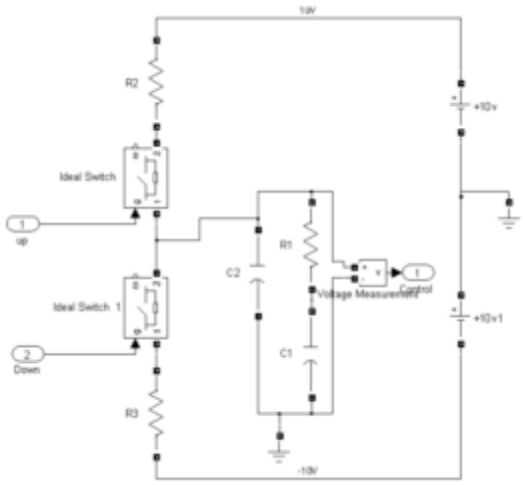


Figure 3 Charge pump loop filter

The charge pump pumps current into a second order loop filter. The branch voltage of the loop filter is used as input to the VCO. The PFD determines whether a positive or negative current is pumped into the filter Phase lead of the variable source corresponds to negative current, which decreases the VCO frequency and phase lag corresponds to positive current. The transfer function of the loop filter is given as:

$$G(s) = \frac{sR1C1 + 1}{s^2 c1c2R1 + s(c1 + c2)} \qquad (1)$$

C. Low Pass Filter (LPF)

Low pass filter can be easily made by connecting together in series a single Resistor with a single Capacitor . In this type of filter arrangement the input signal (Vin) is applied to the series combination (both the Resistor and Capacitor together) but the output signal (V out) is taken across the capacitor only [9].

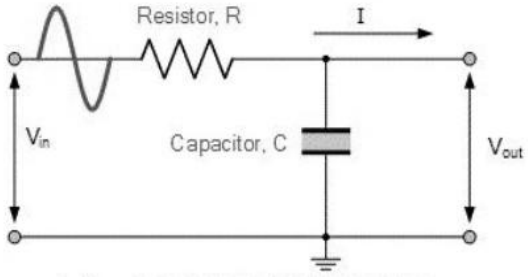


Figure 4 Low Pass Filter

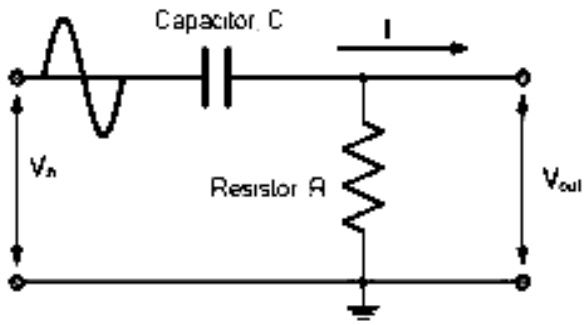


Fig. 5 High pass Filter

D. High Pass Filter (differentiator RC circuit).

High Pass Filter (HPF) can be made by connecting together in series a single Capacitor with a single Resistor as shown in Fig 5. In this type of filter arrangement the input signal (Vin) is applied to the series combination (both the Resistor and Capacitor together) but the output signal (V out) is taken across the resistor only. When we write the output voltage equation of capacitor and resistance of HPF circuit, its gives the differential output with to time. Thus we can say that the HPF acts a differentiator. [10] & [11]

E. Voltage Controlled Oscillator

A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by an input voltage. It produces a digital pulse train whose frequency is proportional to the voltage across capacitor of the LPF. The VCO block diagram is given in [12].

We assign C2 = 17e-12; C1 = 82e-12; R1 = 23e3; R2 = R3 =10e3

The digital PLL model is shown in figure 6.

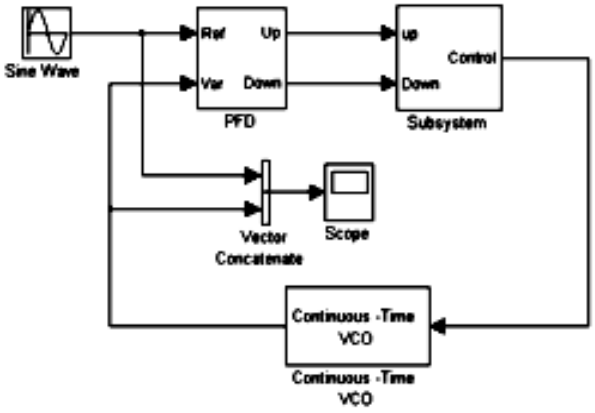
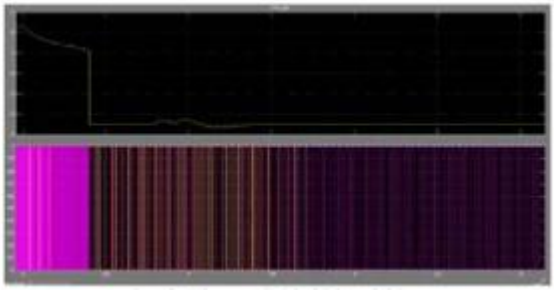


Fig. 6 Digital phase locked loop (DPLL)

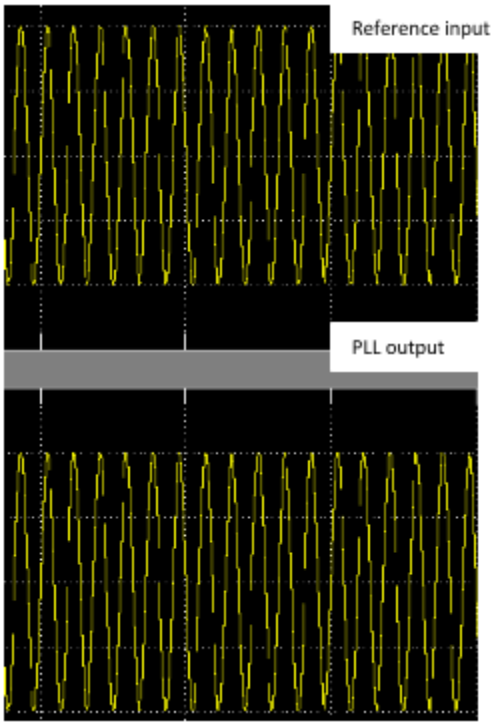
IV. MATLAB/SIMULINK SIMULATIONS

This paper reviews the PLL technique which is applicable to communication and servo control system. It is pointed out that the development of better PLL technology is continuing. The locking time of frequency range 1.5GHz-245MHZ in DPLL (Matlab) is 162ns, but in Fast locking DPLL with HPF (Differentiator) is 39ns.

Locking Time Graph of Fast Locking Flash DPLL



Look time=765-603=162ns



Output waveform of digital PLL

V. CONCLUSIONS

In the fast locking DPLL using HPF uses PF, LPF, HPF, and VCO. The LPF is consists of R and C. By adjusting the values of R and C we can improve the locking time. Phase -locked

loop is widely used in communication system. In the phase-locked loop, the input frequency waveform and feedback frequency waveform are overlap each other and said that system is locked. The time at which the system is locked called the locking time of that system.

REFERENCES

[1] Mao Lai and Michino Nakano, " Special Section on Phase Locked Loop Techniques", Guest Editorial, IEEE Transactions on Industrial Electronics,Vol 43, No 6, December 1996.

[2] Guan Chyun Hsich and James C Hung, "Phase Locked Loop Techniques –A Survey", IEEE Transactions on Industrial Electronics, Vol 43, No 6, December 1996.

[3] P. Larsson, "Reduced Pull-In Time of Phase-Locked Loops Using a Simple Nonlinear Phase Detector", IEE Proc. On Communications, Vol. 142, pp. 221-226, 1995.

[4] M. F. Wagdy and S. Vaishnava, "A Fast-Locking Digital Phase-Locked Loop", Proc. Of the 3rd Intl. Conf. on Information Technology: New Generations (ITNG-2006), Las Vegas, Nevada pp. 742-746, April 10-12, 2006.

[5] M. F. Wagdy and M. S. Waheed, "Design of a 2-GHz Fast-Locking Digital PLL Using Multiple Charge Pumps", Proc. of the IEEE 2nd Intl. Comp. Eng. Conf. (ICENCO 2006), Cairo, Egypt, pp. HW 67-73, Dec. 26-28, 2006.

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[6] M. F. Wagdy and M. S. Waheed, Behavioral Modeling of Fast-Locking Digital PLL Using Multiple Charge Pumps", IEEE 3rd Int. Comp. Eng. Conf.(ICENCO 2007), Cairo University, Giza, Egypt, pp. IP 25-31, Dec. 26-27, 2007.

[7] A. Bellaouar and K. Sharaf "Fast Lock Self Tuning VCO Based PLL", U. S. Patent #6,566,966, May 20, 2003

[8] C.M. Davis, D. L. Broughton, and E. W. Porter, "Method and Circuit For Improving Lock-Time Performance for a Phase-Locked Loop", U.S. Patent # 6,624,707, September 23, 2003.

[9] J. J. McDonald, II and R. B. Hulfachor, "Circuitry to Reduce PLL Lock Acquisition Time", U. S. Patent # 6,940,356, Sept. 6, 2005.

[10] Analog Devices Inc.,"ADF4007–High Frequency Divider/PLL FrequencSynthesizer",http://www.analog.com

[11] TrueCircuitsInc.,www.truecircuits.com/product_matrix.html.

[12] R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, pp. 373-424, IEEE Press (Wiley), Piscataway, NJ, 2010.

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