A Novel Low Ground Bounce Noise and Low Leakage Technique for Adder Circuit

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Abstract— ***Leakage power dissipation increases exponentially with technology scaling and degrade the performance of IC. Multi threshold CMOS technique which is called as Power gating is a well-known way to reduce leakage current but abrupt transitions from sleep to active mode introduces Ground Bounce Noise appear which effects normal working of circuit and reduces the reliability of circuit. An effective technique is proposed here to deal with ground bounce noise and leakage problem in the circuit. For that an additional wait mode is added in the circuit to reduce the ground bounce noise and to reduce leakage, ultra-low power diode technique is used. A comparison between existing techniques is done on 45nm technology node which shows that the proposed technique reduces leak age by 54.68% and ground bounce noise by 30.72%.***

Keywords— ***Leakage current, Ground Bounce Noise, Ultra Low Power Diode, Forward Body biasing, Reverse Body Biasing.***

I. INTRODUCTION

The Leakage power of a circuit is one of the biggest challenges related to low-power designs. Power Gating is an efficient technique to suppress the Leakage current, and improves Leakage Power [1][2][10]. In this technique, a High Threshold (High-Vth) transistor is added either between Supply Rail and Logic block (Header) or Logic block and Ground Rail (Footer), or a combination of both is used. Power Gating is a technique which turns off certain part of the chip, when chip is idle. At the same time, during mode transition from sleep mode to active mode power gated circuit suffers from ground Bounce Current due to sudden discharge path from virtual Vdd to Ground line, which results from parasitic inductance of circuit [3]. High Threshold voltage for sleep transistor is chosen due to fact that it restricts the leakage current and Logic block consists of low voltage transistors to increase the performance of the circuit.

In Fig.1 drain of the nMOS sleep transistor is at ≈Vdd, when transistor switches from sleep mode to active mode, surge current flows owing to discharge of the drain terminal of nMOS sleep transistor, known as Ground Bounce Noise. Power Gating needs special attention in case of Current surge produced during switching between sleep to active mode. At the same time we need to take care of reliability issues occurring due to parameter variations.

Paper organization is as follows, Section II describes Power Gating techniques to minimize Ground Bounce Noise and Leakage of the Circuit, followed by Section III which discusses proposed technique to reduce leakage and ground bounce noise. Section IV shows the Experimental analysis of current techniques and proposed techniques, followed by Conclusion in Section V.

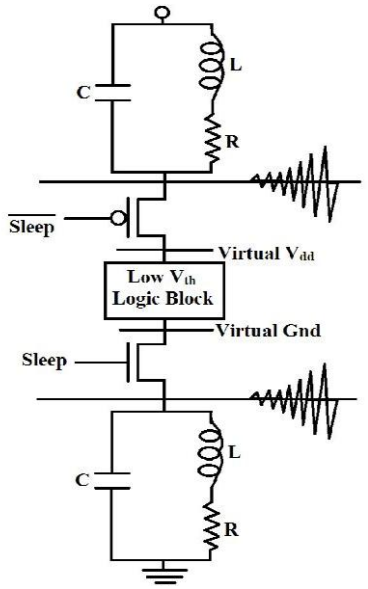

Fig.1 Power gating circuit

II. DIODE BASED TRIMODE MTCMOS TECHNIQUE

In the design given in (Fig.2) the transistor N1, N2 and P1 are high threshold sleep transistors. The gate of N 2 transistor is connected to drain of N1 to make a MOS diode and this is connected inseries with transistor N1 [6].The capacitor C1 isconnected to control the drain current of transistor N_1 and to control the intermediate voltage V_{gnd2}. Additional wait mode is being introduced between sleep to active mode transition of circuit by adding an extra pMOS transistor P_1 in parallel.

When circuit is in standby mode all sleep transistors N_1, N_2 and P_1 are turned off. The sub threshold Leakage current expression is given by equation (1) [6][7] and [9].

$$I_{SUB} = A.\exp\left(\left({}^{q}/_{nkT}\right)\left(V_{gs} - V_{th0} + \lambda V_{bs} + nV_{ds}\right)\right).$$

$$\left(1 - exp\left(^{-qV_{ds}}/_{kT}\right)\right) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where

$$A = \mu_n C_{ox} \frac{W}{L} \left(\frac{kT}{q}\right)^2 e^{1.8} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

V_{gs}, V_{ds} and V_{bs} are the gate to source, drain to source and bulk to source voltages correspondingly.V_{th0} is the zero bias threshold voltage, η is the drain induced barrier lowering coefficient (DIBL) and γ is the body effect co efficient ,C_{ox} is the gate oxide capacitance and μ_n is mobility . Equation (1) and (2) shows leakage current reduces exponentially when drain to source voltage decreases and if body effect increases (negative V_{bs}).

In standby mode, sleep transistors N_1, N_2 and P_1 are turned off so intermediate node V_{gnd2} is charged up to some positive potential due to small drain current of sleep transistor N_1, due to this positive potential at the intermediate node V_{gnd2}, the drain-to source potential V_{ds1} of sleep transistor N_1 reduces, which causes less drain induced barrier lowering effect and negative body-to-source voltage V_{bs1} of sleep transistor P_1 leads to body effect. This way stacking of transistor reduces sub threshold leakage in the given circuit. As the transistor N_2 is diode connected, when the diode is reverse biased, whereas the source is seemed to be connected with gate so V_{ds} of transistor reduces and due to this reduction in V_{ds} of transistor N_2 the leakage also reduces.

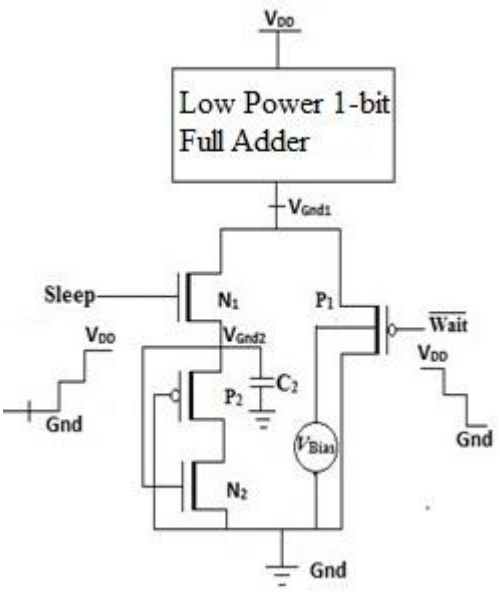

Fig. 2.Ultra low power diode based MTCMOS technique.

When circuit goes from sleep to active mode it firstly goes from sleep to wait mode and then from wait to active mode. When circuit goes from sleep to wait mode the transistor P1 turns on but N1 and N2 are turned off .Wait transistor P1 is forward body biased, due to which virtual ground Vgnd1 discharges up to threshold voltage of P1 transistor easily without increasing the width of transistor and the first peak of ground bounce noise across it will increase. For completing the reactivation cycle transition, circuit goes from wait to active mode in which transistor P1 turns off and transistors N1 and N2 are turned on. By controlling the V_{ds} drain to source voltage of transistor N2 and intermediate node voltage Vgnd2 the ground bounce noise can be controlled more efficiently. Wait to active mode transition the transistor N1 turns on first, at this moment the capacitance C_2 starts charging. When the capacitor C_2 is charged up to the threshold value of transistor N_2, the N_2 turns on and capacitor C_2 starts discharging. Therefore the ground bounce noise reduces.

III. PROPOSED ULTRA LOW POWER DIODE BASED TECHNIQUE WITH PARALLEL SLEEP PMOS TRANSISTORS

In the proposed design N1, N2, P1, P2 and P3 are high threshold sleep transistors. The transistor P2 and N2 forms Ultra low power (ULP) diode a s shown in (Fig.3) [8][11]. High threshold sleep transistor N1 in stacking with ULP diode is used here to reduce the leakage and ground bounce noise and parallel pMOS transistor P1 and P3 are used to add an extra wait state [4][6].

Ultra low power diode is the combination of nMOS and pMOS transistors which are use d to reduce leakage more effectively. The weak inversion d rain current for nMOS and pMOS transistors are given by

$$I_{d,N_2} = I_{sn0}.\exp\left(\left(V_{gs,N2} + \eta V_{dsN2}\right)/nV_T\right)(1 - \exp(-V_{dsN2}/V_T)) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

$$I_{d,P_2} = I_{sp0}.\exp\left(-\left(V_{gs,P2} - \eta V_{dsP2}\right)/nV_T\right)(1 - \exp(-V_{dsP2}/V_T)) \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where Vgs and Vds are gate-to-source and drain-to-source voltage respectively, n is body coefficient, VT = kT/q is the thermal voltage and η is drain induced barrier lowering (DIBL) coefficient. Isno and Ispo are the reference currents that correspond to the extrapolation of weak inversion drain current for Vgs=0 and Vds in saturation (but low enough to neglect DIBL).

In standby mode Ultra low power diode is in reverse bias condition, so sleep transistor P2 and N2 are operating with negative gate to source voltage Vgs, which reduces the

leakage current. The circuit uses two parallel sleep pMOS transistors, the width (W) of parallel sleep pMOS transistors P1 and P3 in (Fig. 3) is half of the width of the transistor P 1 of (Fig. 2). The leakage current is directly proportional to the width of transistor, as given in equation (1) and (2), if W of transistor decreases the leakage also reduces. In this way the leakage reduces more effectively by reducing the W of transistor P1 of (Fig.2) to W/2 of transistors P1 and P3 (Fig.3).

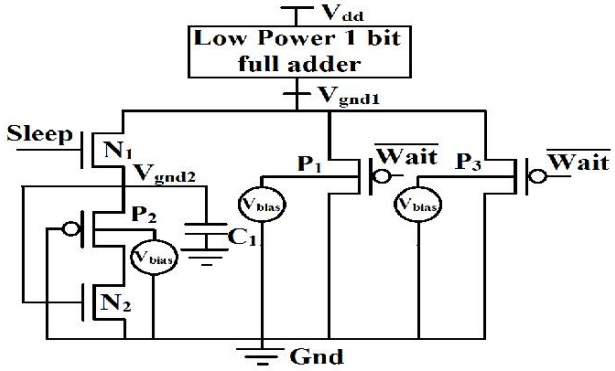

Fig.3 Ultra low power diode based technique with parallel sleep pMOS transistors

When circuit goes from sleep to wait mode the transistor P3 turns on but N1, N2, P1 and P2 are turned off and virtual ground discharges through P3 to the threshold voltage Vtp3 of P3 transistor. The virtual ground can be discharged easily by using forward body biasing (FBB) on P3 and first ground bounce noise peak comes across it. After this the second wait transistor P1 turns on and forward body biasing is applied on it, so again virtual ground voltage Vgnd1 is discharged through it up to the amount of threshold voltage Vtp1 of transistor P 1 and a second peak of ground bounce comes across it. The virtual ground can be discharged easily by using Forward body biasing on P 1and P3 transistors. To complete the reactivation process the circuit goes from wait to active mode and transistor P 1 and P3 turns off and transistor N1 turns on, due to which capacitor starts charging. When capacitor is charged up to the threshold voltage of transistor N2 the transistor N 2 turns on and capacitor starts discharging. This way the use of transistor stacking, ultralow power diode and parallel pMOS sleep transistor 'P3' reduces the Ground bounce noise to a considerable amount.

IV. SIMULATION RESULTS AND COMPARISON WITH PREVIOUS TECHNIQUE

The simulation setup has been done for low power 1 bit full adder, including activation noise model. Here the effectiveness of activation noise-aware ultra-low power diode based MTCMOS technique has been demonstrated using 1 bit full adder circuit for standby leakage current and activation noise reduction. This is the very important block in any of the logic circuitry, consequently all the observations are made for this circuit topology.

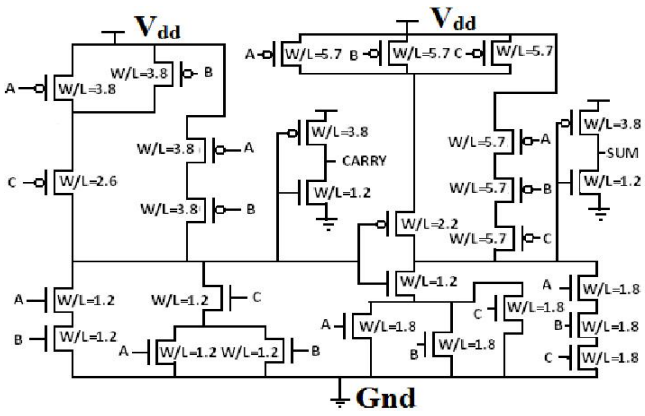

Fig.4 1-bit full adder design

Fig. 4 shows design of 1-bit full adder and is being taken as a Design Under Test (DUT). Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays an important role in static CMOS style. The smallest transistor considered has a width of 60nm and length of 45nm and gives W/L ratio of 1.2 for 45nm technology. Fig. 7 shows design of 16 bit full adder design.

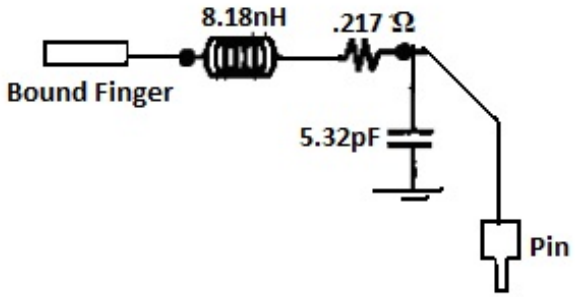

Fig.5 DIP -40 package pin activation noise model

The simulation has been done using Tanner SpiceV14.1 simulator using BPTM 45nm technology with supply voltage of 1V at room temperature. For modelling activation noise the electrical characteristics of 40-pin dual in–line Package (DIP-40) has been used [10] as shown in fig. 5.

A. Ground bounce noise analysis

All simulation is done on one bit full adder circuit. The circuit diagram of one bit full adder is given in Fig.4 [5]. The simulation results are given for changes in ground bounce noise due to change i n Body Bias voltage and changes in size of wait transistor.

TABLE I. GROUND BOUNCE NOISE ANALYSIS WITH CHANGE IN BODY BIAS VOLTAGE

Body bias voltage (V)	Ground Bounce noise in (mv)	
	Diode based trimode MTCMOS technique [6]	Proposed ULP diode with parallel sleep pMOS transistor
1.6	0.92	0.58
1.4	1.24	0.63
1.2	1.47	0.86
1	1.53	1.06
0.8	1.84	1.21
0.6	1.89	1.31
0.4	2.15	1.39

Table 1 shows the Ground Bounce Noise analysis of previous and proposed technique with change in Body bias voltage. The result shows that G round bounce noise in the system increases by using Forward body biasing and reduces with increment in Reverse body biasing voltage. The comparison graph of designs for Ground Bounce Noise variations with respect to supply voltage is shown in (Fig. 6).

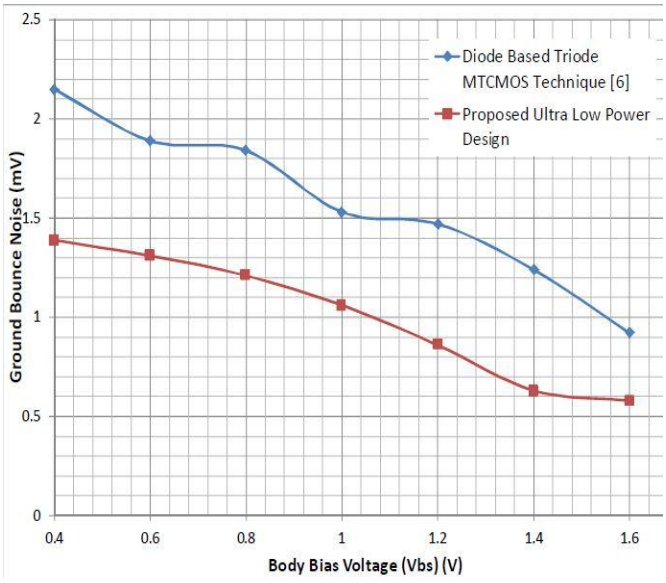

Fig.6 Ground Bounce noise analysis with change in Body Bias Voltage

Fig.7 and fig.8 shows the analysis of ground bounce noise peaks for Diode based Trimode MTCMOS technique and Ultra Low Power Diode based technique with parallel sleep transistors respectively.

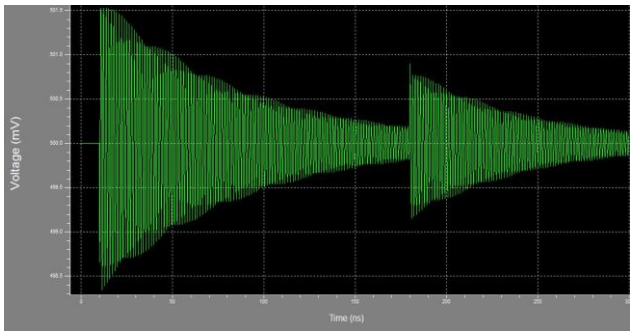

Fig.7 Ground bounce noise alalysis for Diode based Trimode MTCMOS technique [6]

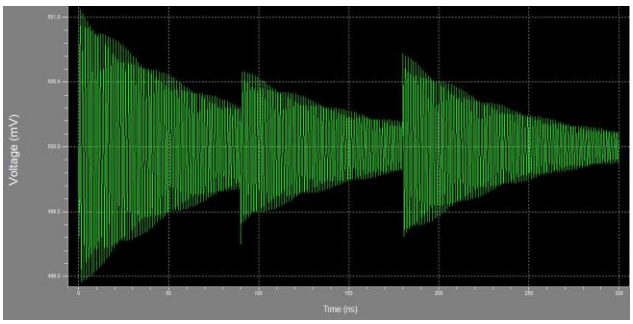

Fig.8 Ground Bounce noise analysis for Ultra low power diode based technique with parallel sleep pMOS transistors

TABLE II. GROUND BOUNCE NOISE ANALYSIS WITH CHANGE IN WAIT TRANSISTOR SIZE

Wait transistor size in (um)	Ground Bounce noise in (mv)	
	Diode based trimode MTCMOS technique [6]	Proposed ULP diode with parallel sleep pMOS transistor
1	0.52	0.58
3	0.62	0.65
6	0.8	0.86
9	1.09	1.26
13	1.48	1.56
15	1.53	1.78
17	1.67	2

Table II shows the comparison result of design with change in size of wait transistors (P_1 and P_3), the comparison result shows that the Ground Bounce Noise in the system increases with increasing the size of wait transistors. The comparison graph is shown in (Fig.9).

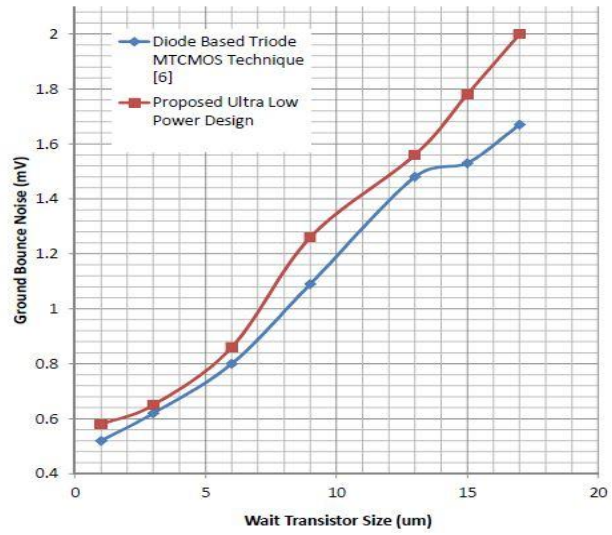

Fig.9 Ground Bounce noise analysis with change in wait transistor size

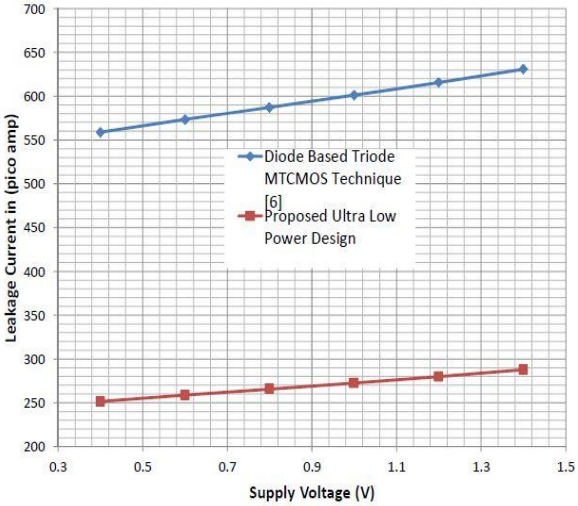

Fig.10 Leakage current analysis with change in Supply voltage

B. Leakage current analysis

The Leakage current simulation is done for one bit full adder circuit with change in Body Bias voltage and results are shown in table III.

TABLE III. LEAKAGE CURRENT ANALYSIS WITH CHANGE IN SUPPLY VOLTAGE

Supply Voltage (V)	Leakage current in (pico amp.)	
	Diode based trimode MTCMOS technique	ULP diode with parallel sleep pMOS transistor
0.4	558.95	251.59
0.6	573.41	258.67
0.8	587.23	265.6
1	601.14	272.61
1.2	615.58	279.94
1.4	630.86	287.9

Table III shows the change in leakage current in different power gating designs with change in supply voltage. As the supply voltage reduces the leakage current reduces in the circuit as shown in result. The comparison graph is shown in (Fig.10).

V. CONCLUSION

Leakage Power reduction and Reliability of the circuit are the major design goals with technology scaling down. In this paper we have proposed a leakage and Ground Bounce Noise improvement technique using Ultra low power diode based with parallel sleep pMOS transistors, which has proved to be a better technique for leakage and ground bounce noise reduction as compared to Diode Based Trimode MTCMOS power gating technique. There is a small area overhead for the proposed technique. The leakage reduces by up to 54.68% as compared to Diode Based Trimode MTCMOS power gating technique and Ground Bounce noise reduction improvement is 30.72% by using forward body biasing in active mode.

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