Design of Low Power and Area Efficient Full Adder using Modified Gate Diffusion Input

Hemant Rajoriya[1*], Sachin Bandewar[2]

[1]*M.Tech (Student VLSI), Professor,* [2]*Department of ECE*

[1, 2]*Sri SatyaSai College of Engineering, Bhopal, M.P.- India.*

Abstract - Low Power procedures are getting to be distinctly critical and valuable as the quantity of transistors is expanding each day. It is essential to lessen the power dissemination for long life, more dependable and superior frameworks. Door Diffusion Input (GDI) is one system to accomplish low power. GDI requires less number of transistors when contrasted with relating CMOS rationale. The fundamental GDI cell comprises of just two transistors, where all the three terminals Gate, Source and Drain of the transistors are dealt with as inputs.GDI system additionally has the benefit of less postponement and decreased region. Alternate applies Gate-Diffusion-Input (GDI) strategy to full adders. Reproductions are performed by utilizing Cadence Virtuoso in view of 65nm CMOS innovation. In correlation with Static Energy Recovery Full (SERF) snake cell module, the proposed four full viper cells exhibit their focal points, including lower control utilization, littler region, and higher speed. Additionally it demonstrates less power and less postponement with around 60% region increment when contrasted with fundamental GDI. This paper exhibits low power superior multiplexer based full viper outline in CADENCE VIRTUOSO GPDK 45nm Technology. The power utilization examination is additionally made in view of CMOS and GDI plan system.

Keywords: Full Adder, Pass transistor logic, Low power, GDI, XOR, XNOR.

I. INTRODUCTION

As the many-sided quality of the electronic circuits increment, the power dispersal gets to be distinctly one of the critical components to be considered for higher execution of the outline. Consequently there is a requirement for a plan that diminishes the unpredictability furthermore decreases the power scattering.

There are basically two sorts of force dispersal, viz dynamic power and static power. The dynamic power scattering is because of the exchanging of the hubs. Static power is because of spillage and sub-edge current. There are numerous methods which are utilized to decrease the power scattering without debasing the outline execution, for example, Clock gating, Power gating, Multi Vt, Gate Diffusion Technique (GDI) and so on. The GDI method is the most intriguing low power system.

The fundamental GDI cell comprises of just two transistors, for example, nMOS and pMOS. The principle preferences of GDI methods are less power, fast, not so much range but rather more adaptability to the planner [2]. With the assistance of this GDI cell essential rationale capacities can be actualized as appeared in Table 1. The constraint of the GDI strategy is the decreased swing as clarified: The fundamental GDI cell has 3 inputs named as G, P and N as appeared in Fig 1. These 3 sources of info are intended to execute any Boolean capacity. Since nMOS produces feeble rationale 1 and pMOS gives frail rationale 0 [3], the yield will be debased at whatever point the information goes through these transistors. This debased yield is what is alluded to as decreased swing in this paper

The present paper addresses this issue of diminished swing and gives answer for acquiring a solid 1 and solid 0 at the yield of a GDI cell. Initial a XOR door is actualized utilizing essential GDI cell and it is indicated how the yield has a diminished swing for both rationale 1 and rationale 0. This XOR entryway is changed to get the full positive (Strong 1) and negative (Strong 0) swings. The imperatives for the alteration incorporate not surpassing the region, power and deferral in contrast with the comparing CMOS execution. The 1-bit Full Adder (FA) is initially executed utilizing essential GDI entryways with diminished swing [4]. This plan is then enhanced utilizing the changed GDI method to acquire solid 1 and solid 0. Examination of the three FA (Basic GDI, Modified GDI and CMOS) outlines is performed utilizing Cadence Virtuoso in light of 45nm Technology.

II. GDI BASIC FUNCTIONS

The fundamental GDI cell comprises of two transistors as appeared in Fig 1. It has three information sources: G, P and N. utilizing these 3 inputs it is anything but difficult to actualize any Boolean expression with less number of transistors. For instance to actualize AND door in CMOS, the quantity of transistors required are six.

Function	G	P	N	OUT
AND	**A**	**0**	**B**	**AB**
OR	**A**	**B**	**1**	**A+B**
NOT	**A**	**1**	**0**	$\bar{A}$
MUX	**S**	**A**	**B**	SA+SB

Table I. Basic Gates Using GDI Cell

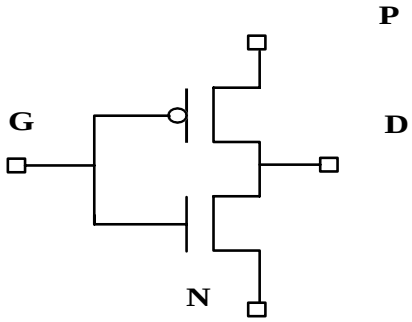

Fig.1 Basic GDI Cell [2]

Correspondingly essential entryways can be planned utilizing just two transistors by giving the fitting contributions at G, P and N terminals of the fundamental GDI cell. These information and the comparing rationale operations are appeared in the Table I. The restriction of GDI cell is that the yield is debased when a logic0 is being transmitted by pMOS. Also, there is corrupted yield when nMOS is transmitting logic1. Since pMOS transistor produces powerless rationale 0 and nMOS gives feeble rationale 1. Nonetheless, there will be full swing when pMOS is passing the logic1 and Nmos passing rationale 0. Contingent on the G info, P and N data sources are chosen at the yield.

III. XOR GATE

For planning a full snake circuit the essential door required is a XOR entryway. The quantity of transistors (Tr) required to execute XOR door utilizing CMOS are 12. Utilizing GDI method, just 4 transistors (4 Tr) are required to plan XOR entryway as appeared in Fig 2.

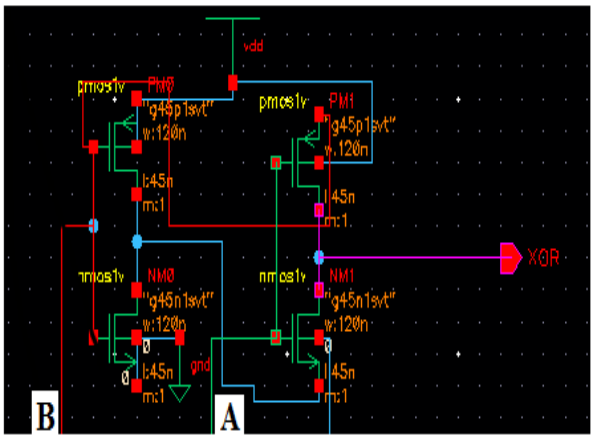

Fig 2: GDI XOR gate (4Tr)

As said in the past area GDI gives feeble 0 and frail 1 relying upon the information P and N. The GDI XOR yield is as specified in Table II. The reenactment waveform of 4 Tr GDI XOR entryway is appeared in Fig 3; In this waveform, when inputs An and B are relegated the estimation of rationale 0, the XOR yield is a corrupted rationale 0. Also when A=1, B=0, then XOR yield is a feeble rationale 1.

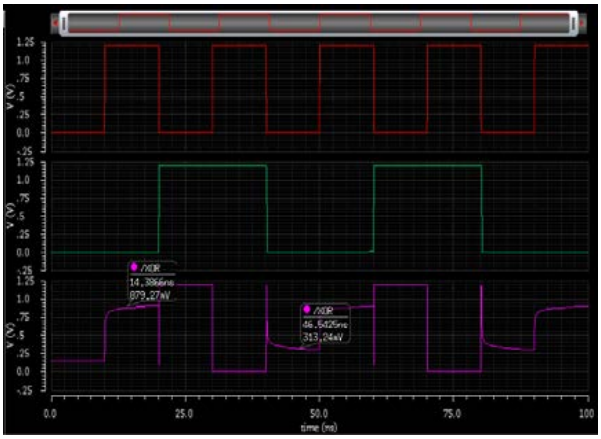

Fig 3: Simulation waveform of GDI XOR gate (4Tr)

Table II. TRUTH TABLE OF XOR GATE

INPUT		OUTPUT
A	**B**	**A XOR B**
0	0	0
0	1	1
1	0	1
1	1	0

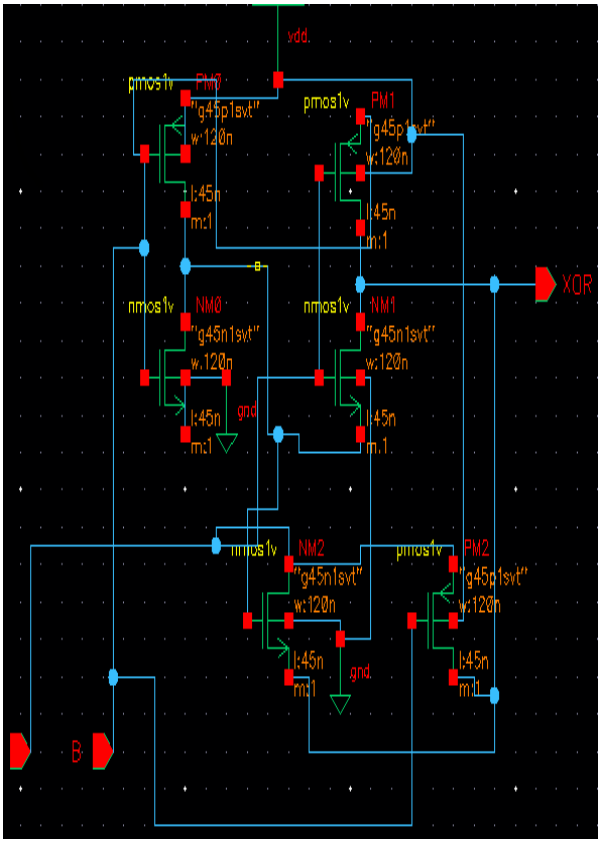

Fig 4: GDI XOR gate (6Tr)

In order to improve the swing to get a strong logic 1 and strong logic 0, extra transistors are added as shown in Fig 4. It requires only 2 extra transistors. Addition of these transistors does not affect the functioning of the basic GDI circuit. It only aids in obtaining both strong 0 and 1 at the output of the XOR as depicted in the simulation results (Fig 5)

The average power of XOR gate using 4 Tr and 6 Tr GDI technique and CMOS technique are calculated from the simulation waveform. The average power results obtained from Cadence Virtuoso for 45 nm technology are shown in Table III.

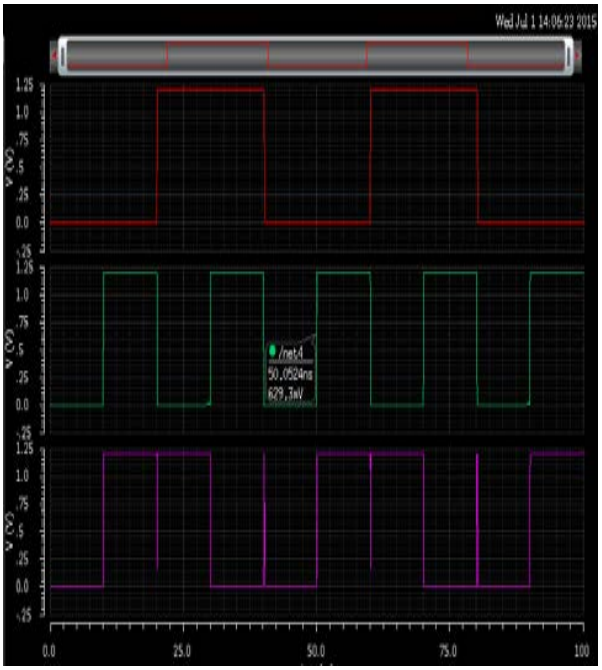

Fig 5: Simulation Waveform of GDI XOR gate (6 Tr)

TABLE III. AVERAGE POWER OF XOR GATE

XOR	Average Power (nw)
GDI (4 Tr)	9.02
Modified GDI (6Tr)	17.05
CMOS (12 Tr)	84.67

IV. Full Adder

A 1-bit full adder circuit can be designed using (1).

$$Sum = A \text{ xor } B \text{ xor } Cin$$

$$Cout = (AxorB)Cin + AB \text{ ..... } (1)$$

As said in the past area GDI gives feeble 0 and frail 1 relying upon the information P and N. The GDI XOR yield is as specified in Table II. The reenactment waveform of 4 Tr GDI XOR entryway is appeared in Fig 3; In this waveform, when inputs An and B are relegated the estimation of rationale 0, the XOR yield is a corrupted rationale 0. Also when A=1, B=0, then XOR yield is a feeble rationale 1

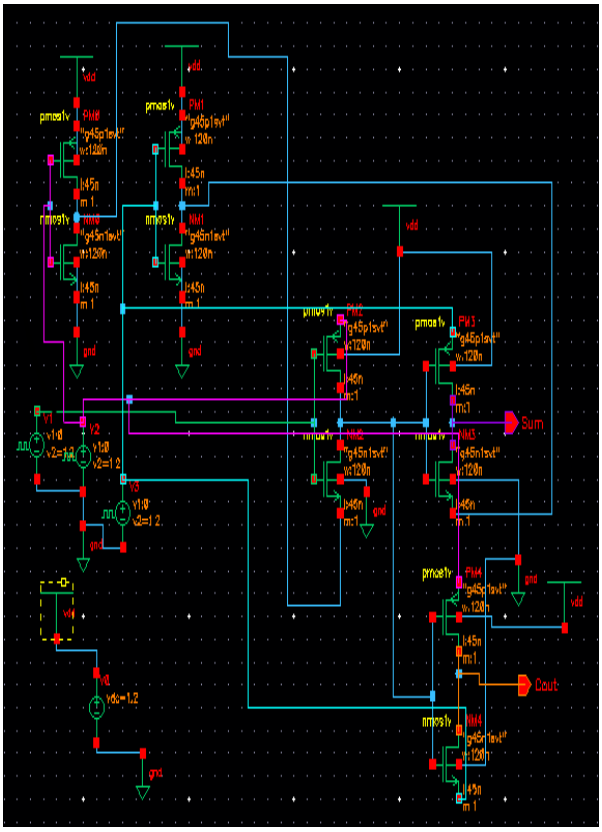

Fig 6: GDI Full Adder (10T)

Table IV Full Adder Truth Table

A	B	Cin	SUM	GDI SUM	Cout	GDI Cout
0	0	0	0	Weak0	0	Weak0
0	0	1	1	1	0	Weak0
0	1	0	1	Weak1	0	0
0	1	1	0	0	1	Weak1
1	0	0	1	Weak 1	0	0
1	0	1	0	0	1	Weak1
1	1	0	0	Weak 0	1	1
1	1	1	1	1	1	1

The full viper circuit is changed keeping in mind the end goal to evade the Weak1 and Weak 0 yields and the outline utilized 17 Tr [5]. In this paper the full viper circuit is actualized by utilizing the altered GDI XOR door (depicted in Section III). Utilizing this XOR Gate the full viper was

actualized utilizing just 14Tr. Fig 8 demonstrates the recreated yield of the 14Tr full viper.

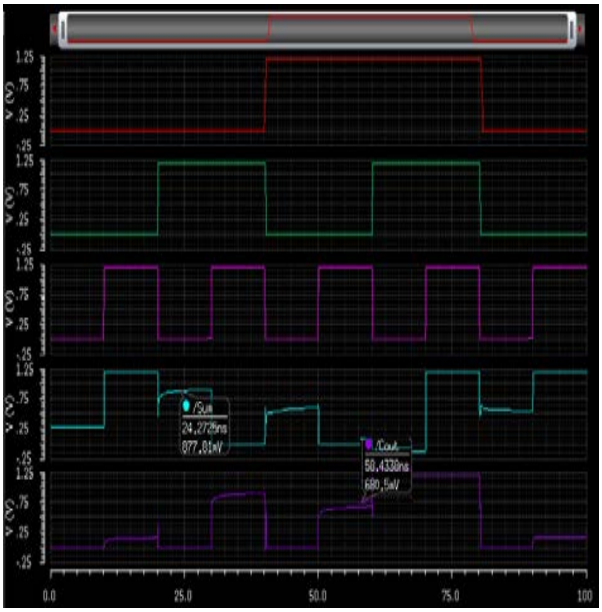

Fig 7: Simulation output of GDI Full Adder (10T)

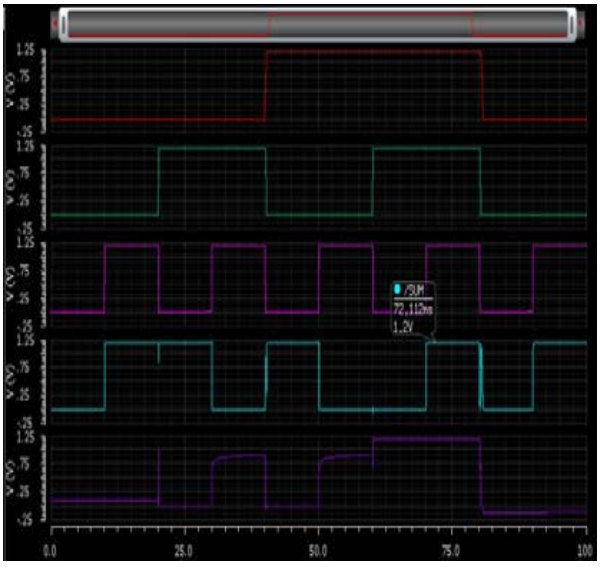

Fig 8: Simulation of Modified GDI Full Adder (14T)

IV. RESULT

Since XOR gate is basic circuit for full adder, XOR GDI is modified to achieve full swing of logic 1 and logic 0. Using this XOR gate, the full adder is implemented with a total of 14 Tr. The average power is reduced with improved swing in the modified GDI full adder. Table V depicts the average power of basic GDI FA with 10Tr and modified GDI FA with 14Tr.

Full Adder	Average Power (nw)
GDI (10T)	31.94
Modified GDI (14T)	28.9
CMOS	360

Table V. Average Power Of Adder Circuit

V. CONCLUSIONS

The Gate Diffusion Input is an effective low power plan strategy. Complex capacities can be executed utilizing this procedure utilizing less number of transistors. The inconvenience of the GDI strategy is that, it is unrealistic to acquire a solid 0 and solid 1 at the yield under specific mixes of information sources and past state. A change was specified in this paper to beat the impediment of the GDI cell. The GDI cell is altered to acquire the full swing at the yield. Because of this change, the quantity of transistors is expanded yet at the same time the check is not as much as that utilized as a part of the CMOS plan. A XOR entryway was actualized utilizing the essential GDI cell and afterward the door configuration was adjusted to obtain\ the full swing at the yield. This XOR door was then utilized as a part of a basic outline of 1-bit full viper. It was demonstrated that utilizing the GDI method, it is conceivable to lessen the range and energy all things considered. Examination between changed GDI procedure and CMOS execution was accomplished for the outlines utilizing Cadence Virtuoso 45nm innovation. Future work includes confirming the pertinence and reasonableness of the GDI method to more unpredictable and bigger outlines. The creators are as of now investigating the GDI procedure on 8-bit 16-bit adders, 4-bit multipliers. Creators plan to contrast the GDI circuits and the comparing CMOS outlines.

VI. REFERENCES

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