Design of high Order Digital Phase-Locked Loops Using Matlab

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***Abstract*—this paper presents a "design of high order digital phase locked loop". This paper also present novel approach to overcome these difficulties by allowing high order loops to be viewed as a natural extension of lower order ones. This is accomplished by adding nested first-order feedback loops around a basic first-order Loop Filter. In the Previous method the fast locking DPLL operation Reduces the lock time by a factor about 4.40 Compared to its conventional DPLL counterpart. But this method more effective model presented has been implemented and tested in Simulink®.**

***Keywords*—Analog Signal Processing, Feedback Systems, Loop Filters, Phase-Locked Loops**.

1. INTRODUCTION

The exact analysis of 3rd order PLLs, i.e., those including a 2nd order Loop Filter (LF), is normally eluded because it is very complex. Even most recent books on DPLL limit themselves, at best, to calculating s-domain equations without giving any practical design guidelines [1-2]. A general practice is to approximate the 3rd order response by a 2nd order and precede with the well known design equations. The goal of this paper however, is to create an alternative approach to the intuitive and analytic design of 3rd, and even 4th order loops, as a natural extension of second order digital phase locked loop. This approach will also be seen as related to the extension of a conventional DPLL (second order) with the so called Aided acquisition loops [3]. The concepts shown here are general, but of particular interest in applications where the DPLL needs to be operated in a wide hold range, i.e., not a small fraction of the Free Running Frequency (FRF) of the oscillator, such as in on-chip tuning applications [4], wideband signal generation detection, chirp radar signals or spread spectrum clocking.

II. THE SECOND-ORDER DPLL

The block diagram of the novel flash DPLL employing HPF is shown in Fig.1.The DPLL circuit consists of a phase frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), High Pass Filter (HPF) and a voltage-controlled oscillator (VCO) for fine tuning along with a High pass filter (HPF).

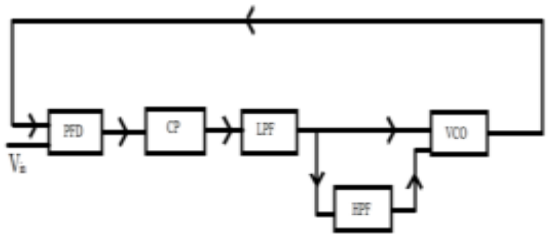

Figure.1block diagram of the Novel Flash Locking DPPL

VCO is usually modeled by an integrator, since phase is the integral of instantaneous frequency with gain K rads/(V.s). As for the Phase Detector, its model depends on the implementation (multiplier, digital, etc.), but it is usually approximated by the phase difference within a limited range, scaled by a gain K. Loop filter is assumed linear, and thus the simplest case, apart from a trivial PLL with no filter, is a first order one. Thus, its most general transfer function, assuming unity DC gain, is:

$$H_{LF}(s) = H_1(s) = \left(1 + \frac{s}{\omega_{1z}}\right) \Big/ \left(1 + \frac{s}{\omega_{1p}}\right) \qquad (1)$$

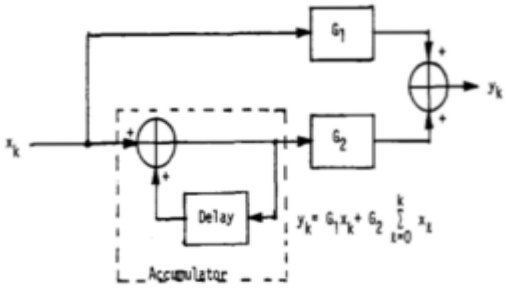

Figure 2: second order digital pll

Its bode plot is represented in Figure 2 for ω < ω. Design equations for this particular case can be found elsewhere, although they are quite often buried by particular electrical parameters dependent on the implementations of the filters (active, passive, switched capacitor, etc.). Since DC filter gain is unity, PLL gain is defined as K= K.K. In short, simple stability analysis shows that stability is guaranteed if ω >ω ≥ 0. An interesting case is when ω =0 giving rise to a 2nd order-Type II PLL.

III. THIRD-ORDER DPLL

To our view, the problem can be posed in terms of what thefunctional dependence of the phase at the output of the PD is like, how the frequency error information can be extracted from it, and how they are combined to attain a given dynamics of the loop. We can take an aided acquisition loop could be modelled as indicated in the Figure 4, where the low pass filter 1(LF1) and low pass filter 2 (LF2), and only a conventional PD is used. Differentiator represents derivative of the phase ($\theta \equiv \theta_{out} - \omega_{FRF} t$). Note that we do not claim this model is equivalent to that in Figure 3: Acquisition dynamics is a very complex process and a nonlinear device such as a FD cannot be substituted by a linear operator. In this sense architecture in figure 3 is more flexible and can provide faster phase and frequency error signals resulting in a wider lock-in range.

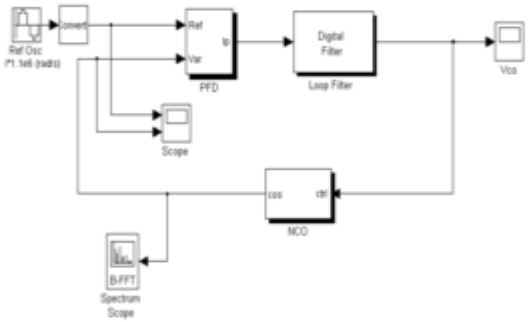

Figure3. all digital DPLL Simulink

Operation of the above model can be described as follows. When a transient is produced at the input, because of a frequency hop, the lower loop reacts and tries to correct the phase difference in the same way as a conventional PLL (Figure 1) would do. If LF2 is also low pass, and has a long time constant, it will filter out the fast variations at the differentiator output and error signal e will remain almost unchanged at its DC value. As the frequency at VCO output gets closer to the input value, and phase starts to be linear with time, the differentiator will give a DC value proportional to the frequency (to the difference with the FRF, actually), which will be transmitted at LF2 output, i.e., e. Then, signal e, which initially produced the frequency change, will reduce in the same amount. Clearly, Loop Filter 2 can be now combined with Loop Filter 1 to give a single Loop Filter. If Loop Filter 1 is of order one, as in Equation (1), and Loop Filter 2 is also of order one with a single pole at ω, i.e.

$$H_2(s) = 1/\left(1 + \frac{s}{\omega_2}\right) \qquad (2)$$

we come up with a second-order loop filter and thus a 3rd order PLL.

$$H_{LF}(s) = H_1(s)\frac{1}{1 - H_2(s)} = \frac{\omega_2}{s}\frac{\left(1 + \frac{s}{\omega_{1z}}\right)\left(1 + \frac{s}{\omega_2}\right)}{\left(1 + \frac{s}{\omega_{1p}}\right)} \qquad (3)$$

It is well known that this pole is the minimum requirement to allow the tracking of frequency hops with zero steady-state phase error. The point to remark now is that we have shown how a 2nd order PLL with the aided acquisition can be seen as equivalent to a 3rd order, Type II PLL. In this process we have gained some insight into the meaning of each one of the time constants and signals into the circuit:

(1) On one side $\omega_2 << \omega_{1P}$ so that the transient of the loop is similar to that of a 2nd order loop.

(2) Residual phase difference after a transient tends to be negligible within a time frame proportional to time constant $1/\omega_2$.

(3) Signal e, carries, in lock conditions, a value proportional to $\omega_0 - \omega_{FRF}$.

(4) Additionally, stability conditions are very easy to check.

Note that in the case of a zero of Loop Filter 1 at infinity, first condition is automatically fulfilled. The second inequality is also fulfilled if the 2nd order loop was stable, and the added feedback has, as suggested, a longer time constant. For sampled PLL, remarkably Charge Pump PLLs, additional stability conditions are obtained based on Z-domain analysis. Charge Pump PLLs are essentially Type II PLLs of order 2 or 3, and thus stability in terms of electrical variables, found elsewhere [6-7], can be easily translated to our parameters in Equation (3). In most practical cases LF1 and LF2 are merged into a single filter.

IV. HIGHER ORDER DPLL

The concept of introducing an additional feedback loop can be once more used to detect, and correct, a typical situation where the input signal is a chirp whose frequency varies linearly with time, either intentionally or due to Doppler

Effect. The modification in the loop studied so far is only able to correct the phase error when the input frequency is constant (possibly after a frequency step) but not to follow a chirp while keeping zero phase error.

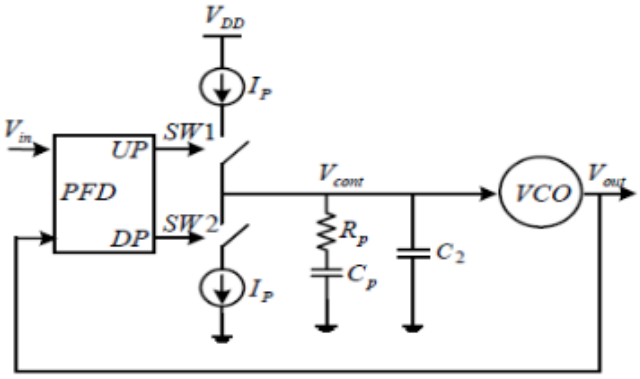

Figure 4- Structure of third order charge pump DPLL

If the filter LF3 is of first order too, with cut-off frequency ω_3 then, the overall performance of the two loops can be assimilated to a single loop filter whose response is now Equation 4[1]:

$$H_{LF}(s) = H_1(s)\frac{1}{(1-H_2(s))(1-H_3(s))} = \frac{\omega_2\omega_3}{s^2}\frac{\left(1+\frac{s}{\omega_{1z}}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)}{\left(1+\frac{s}{\omega_{1p}}\right)}$$

Third order Charge pump PLL filter output in Figure 6 where the time constant of the new filter, $1/\omega_{3,}$ is higher than $1/\omega_{2.}$ This condition is however not needed for the correct operation of the loop since, according to Equation 4 the two poles can be exchanged. The resulting filter is a generalization to third-order of the order two Loop Filter suggested by Gardner [6], giving rise to a Type III PLL of 4th order! (Gardner's filter can be recovered but just making $\omega_{1P} \equiv \omega_{3)}$. The double pole at the origin in the filter is an indication that the PLL is able to follow frequency chirps with zero steady-state phase error, as originally suggested for the Gardner's filter. Note that typical 4th order PLLs reported in most papers are not of this kind: the additional pole is not at the origin and its role is to reduce phase noise [10]. Stability conditions for a 4th order loop cannot be analytically obtained and approximations have not been reported to the best of our knowledge. However it can be expected that, in our particular design case, the conditions for the 3rd order loop are still valid.

V. SIMULATION RESULTS

A Simulink® model, which allows an evaluation of how the various feedback loops affect the operation of the DPLL, and the evolution of the signals involved, was implemented. We will proceed by analysing, first the operation of the 2nd order loop and then appraise how it is affected by the introduction of the new loops. This will mimic the design procedure to be followed, regardless of whether the loop filter is implemented in a compact manner in the final design (just plug-in the LF parameters from the design), or with the explicit feedback loops.

(A) Transient Analysis. The parameters chosen for the PLL are as shown in Table I. Assuming that only LF1 is active, and the other disconnected, the expected behaviour of the PLL can be summarized in the parameters also provided in table I. Phase Detector has been modelled as a perfect Analog multiplier, while VCO is assumed ideal.

Damping Fact	Natural Freq.	Hold-in Range	Lock-in Range
ξ = 0.14	2.10^4	~ (55%FRF)	~(30%FRF)

Table I. PLL parameters (frequencies in rads/sec)

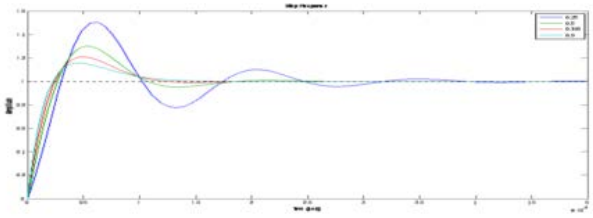

Figure 5- Step response for different values of ξ of Charge pump DPLL

Figure5 shows the step response of third order system for different damping factor. It can be obsered that, as the damping factor of the system. After the first transient at t=0, signal tends to a steady DC value, as a clear indication of a phase difference between input and output signals.

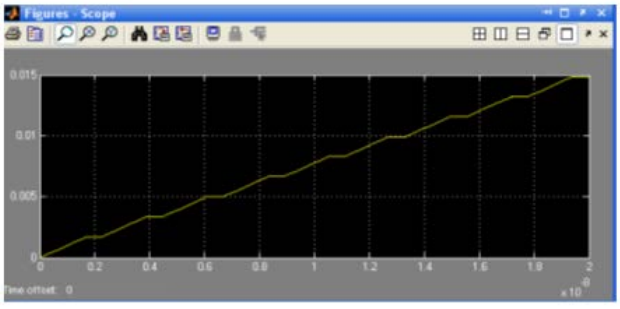

Figure 6-Third order Charge pump PLL filter output

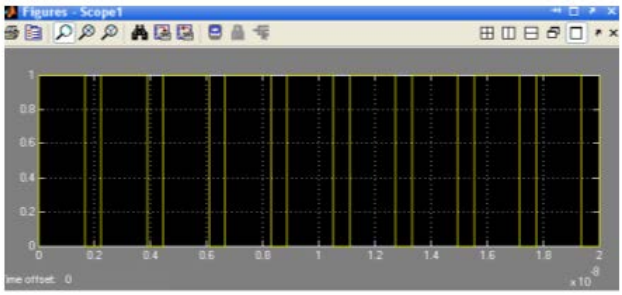

Figure7-Third order Charge pump PLL Phase detector output

(B) Steady State Analysis. Not only transient behaviour is important but also stationary response in terms of how filtering properties of the PLL preserve when the order is Figure 10, 11, 12 shows Third order Charge pump PLL filter output, Phase detector output and VCO output and input signalwith $\Delta\theta=90$ respectively. It can be obsered that when $\Delta\theta=90$,and the reference signal is track PD output is zero.

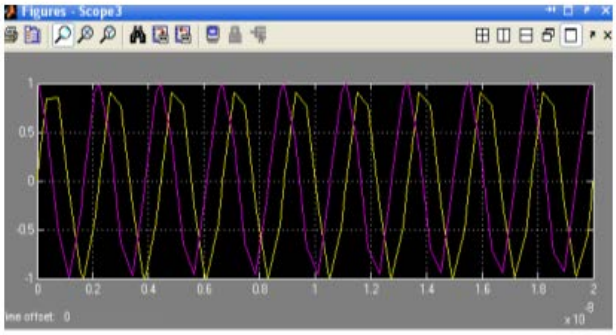

Figure-8 Third order Charge pumps DPLL VCO output and input signal

The input provided in set up is the order coefficient of Loop filter. For e.g., using the transfer function of Loop filter incorporated in automated program written in Matlab which guides to find the input to find the proper range of input applied to the set up assembly to get desired output. Similarly for other input parameters Like, VCO gain in Hz/volts and quiescent frequency were found out. For analysis of third order PLL setup used is almost same as second order PLL, Input for assemble are Transfer Function of loop filter, Kvco, quiescent frequency of VCO.

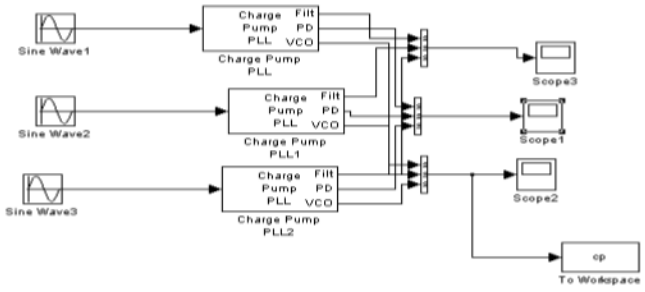

Figure9- Setup for measurement of PLL parameters in Simulink

VI. DISCUSSION OF RESULTS AND CONCLUSIONS

A Simulink® model has been developed to demonstrate the concepts presented here i.e. We have presented high order PLLs as a natural extension of lower order ones, by the addition of feedback loops. The aim of these loops is to reduce phase error under steady frequency at the input, and chirp variations. This model can be used regardless of whether implementation contains separated loops or not, to gain insight into the system's behaviour. The idea of using feedback loops in the Loop Filter has also been related to the concept of aided acquisition.

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