Selective Harmonic PWM based Cascaded Multilevel Inverter with Adjustable DC Voltage Levels Control for STATCOM Applications

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Abstract ***In This research work a new multilevel selective harmonic elimination pulse-width modulation (MSHE–PWM) technique has been proposed for a transformer less static synchronous compensator (STATCOM) system. Proposed strategy is utilized to employ cascaded H-bridge inverter (CHI) configuration. The proposed MSHE–PWM is a effective method to optimize both the switching angles and dc-voltage levels that enable maximum harmonics elimination without affecting the structure of the inverter circuit. The proposed technique gives constant switching points and a linear pattern of dc-voltage levels over the range of modulation index. This in turns dispenses with the monotonous advances required for controlling offline calculated switching angles and accordingly, facilitating the usage of the MSHE– PWM for dynamic systems. Although the strategy depends on the accessibility of the variable dc-voltage levels which can be acquired by different topologies, however, the quick development and improvement in the field of power semiconductor devices prompted deliver high-proficiency dc– dc converters with a generally high-voltage range and for simplicity, a buck dc– dc converter is considered in this work. Current and voltage closed loop controllers are implemented and simulated for both the STATCOM and the buck converter to take care of the reactive power demand at various loading conditions. The system is additionally contrasted and a proportionate regular carrier-based pulse-width modulation to outline its improved qualities. The adequacy and the theoretical examination of the proposed approach are checked through both simulation and experimental analysis.***

Keywords - STATCOM, MLI, Selective Harmonic PWM, DC. low voltage ride through (LVRT).

I. INTRODUCTION

In general inverters are used to convert the DC power supply to AC power supply. In the application point of view the multilevel inverters are used mostly. The multilevel were implemented in different topologies in respective applications. Basically the inverter should consist of power semiconductor switches and DC voltage sources. A block representation of a basic inverter with different levels has been shown in figure 1.1 (a) Two Levels (b) Three Levels (c) n Levels.

The semiconductor switches in the inverters half controlled in general. The control signals for this semiconductor switches will acquired from the relevant firing circuits. Fig. 1 shows the schematic diagram of one phase leg of inverter with different of levels in which the semiconductor device is represented by an ideal switch with several positions. In the above figure the basic view of the multilevel inverters with different number of voltage sources and voltage levels are shown briefly. From the above figure can understand that as the number of the voltage sources is increased the number of the levels in the output voltage is also increased.

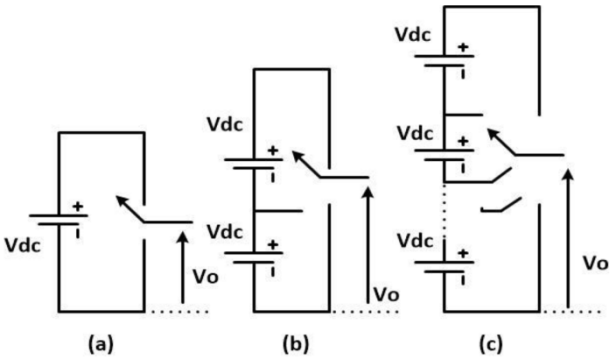

Figure 1.1 Basic view of an inverter with (a) Two Levels (b) Three Levels (c) n Levels.

Multilevel inverter technologies are receiving increased attention recently in high voltage-high power applications due to its high voltage handling and good harmonic rejection capabilities. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application.

This research work focuses on minimizing the most significant harmonic components of the generated waveform while keeping other harmonic components within the acceptable range for the cascaded multilevel

inverter with unequal or varying dc sources for STATCOM application.

An important issue in designing an effective multilevel inverter is to ensure the increase of power, the reduction of voltage stress on the power switching devices, and generation of high-quality output voltages and sinusoidal currents.

II. CASCADED MULTI LEVEL INVERTER

The cascaded multilevel inverter are recently, very popular in medium voltage, large power supplies and speed control applications. A cascaded MLI consists of a single phase full bridge inverter of each phases. Each H-bridge consist of one DC source separately. The each bridge consist single-phase full-bridge inverter having

switches, S1, $S2$, $S3$ andS4, each bridge can generate output voltages,Vdc, 0 and -Vdc. The outputs of each of its full-bridge converter are connected in series. So the output waveform is addition of individual converter outputs, which is staircase waveform. The number of total output voltage levels are $p = 2N + 1$.

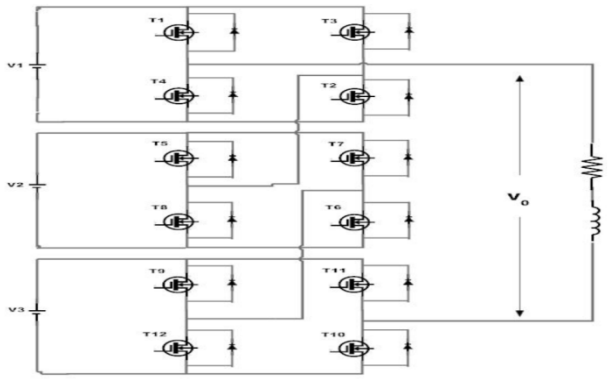

Figure Circuit diagram of the cascaded H-Bridge inverter.

Where $N = total\ number\ of\ DC\ sources\ of\ each\ ridge.$

Cascaded H-Bridge MLI are based on several single-phase inverter connected in series. So it is capable of reaching medium voltage levels. In case, any fault in one of these bridges, it can replace quickly and easily. With control strategy, it is possible to bypass the fault bridge without stop the load, with decrease output. Due to these features, the cascaded H-Bridge multilevel inverters has been more advantages than clamping diode, flying capacitor multilevel inverters.

Some of the advantages of the CHB converter can be summarized as below:

- Modular in structure so packing and circuit layout is easier
- No clamping diodes present as in NPC
- No voltage balancing capacitors present in FC
- Low voltage switching devices required
- No EMI problem
- Less common mode voltage and less
- Suitable for medium voltage, high power applications
- Separate DC sources eliminates the need of the voltage balancing circuits
- With the increase in the number of the level, the staircase waveform approximates to a sinusoid
- It can work at reduced power level when one of its cells is damaged
- Soft switching techniques can be applied to CHB
- No transformer required as in multi-pulse inverters
- Number of possible output voltage levels is more than twice the number of DC sources

III. PROPOSED SYSTEM

This work presents Cascaded Multilevel Inverter with adjustable DC voltage levels control for STATCOM applications in view of Selective Harmonic PWM. A selective harmonic elimination pulse width modulation SHE-PWM methods and their analysis are presented for the purpose of elimination of selected harmonics. The switching angles which are well separated can provide enough time for completion of consecutive transitions which can effectively reduce the switching losses and probability of switching damage in inverter bridges, improve the performance of PWM strategy, and extend life of inverter as well as the whole equipment. It is adaptable for an assortment of utilization necessities. The programmed method based on computer calculations generates a high quality output waveform through elimination of specific lower order harmonics. The critical factor which can heavily impact the calculation convergence is initial values. The selection of a group of bad initial values leads to a much longer calculation time and create wrong solutions. Figure 3.1 shows the Matlab Implementation of proposed selective harmonic PWM based cascaded multilevel inverter cascaded H-bridge STATCOM System.

The customary PWM strategies utilize substantially higher switching frequencies for two reasons. The primary reason concerns harmonics. Unwanted harmonics happen at considerably higher frequencies. Along these lines, filtering is considerably less demanding and more affordable. The second reason concerns capable of being heard commotion. Several kHz is well above the acoustic noise level. Also, if the generated high frequency harmonics are above the bandwidth of some actual

systems, there is no power dissipation due to these harmonics. Figure 3.2 shows the proposed Cascaded H-Bridge STATCOM subsystem of Proposed System.

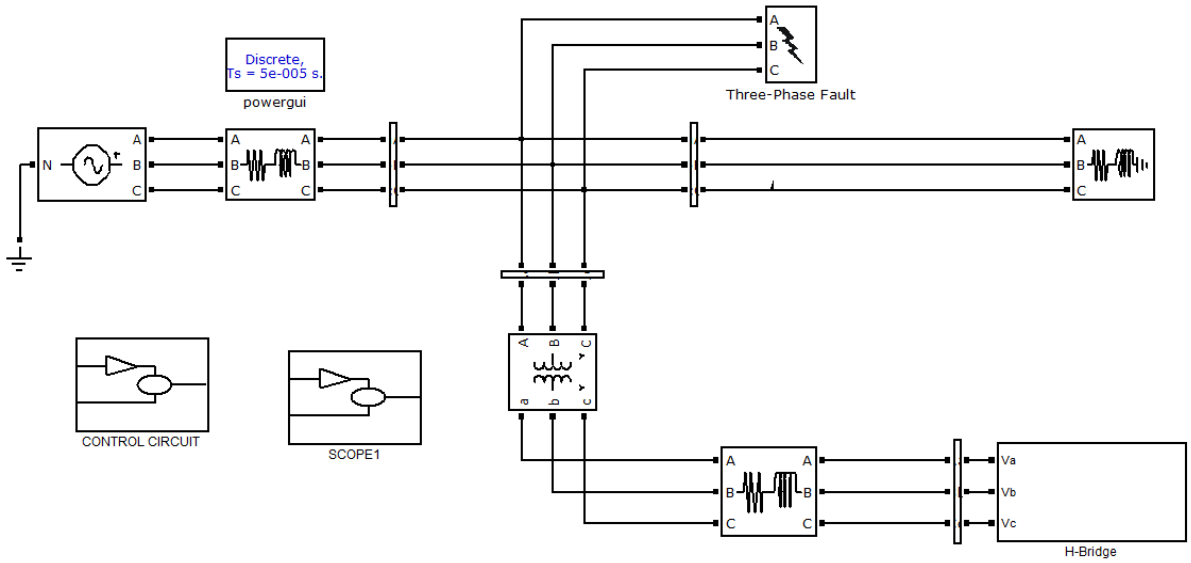

Fig. 3.1 Selective Harmonic PWM based Cascaded Multilevel Inverter Cascaded H-Bridge STATCOM System.

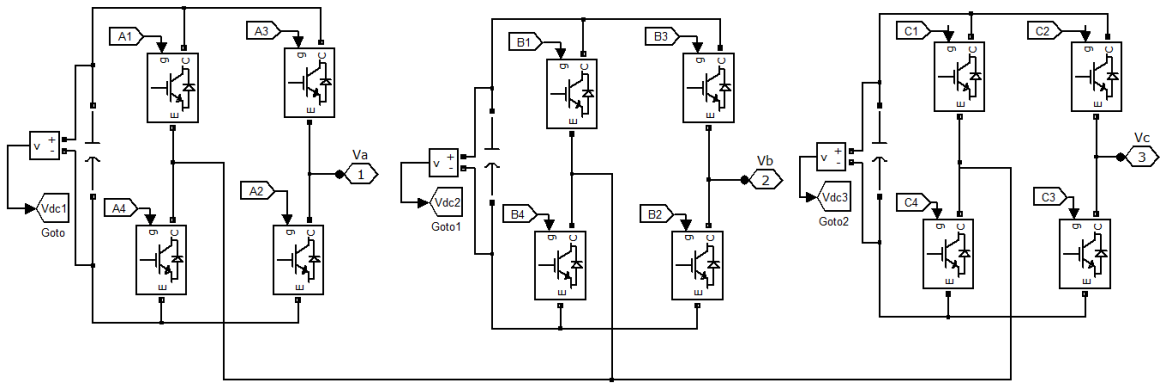

Fig. 3.2 Cascaded H-Bridge STATCOM subsystem of Proposed System

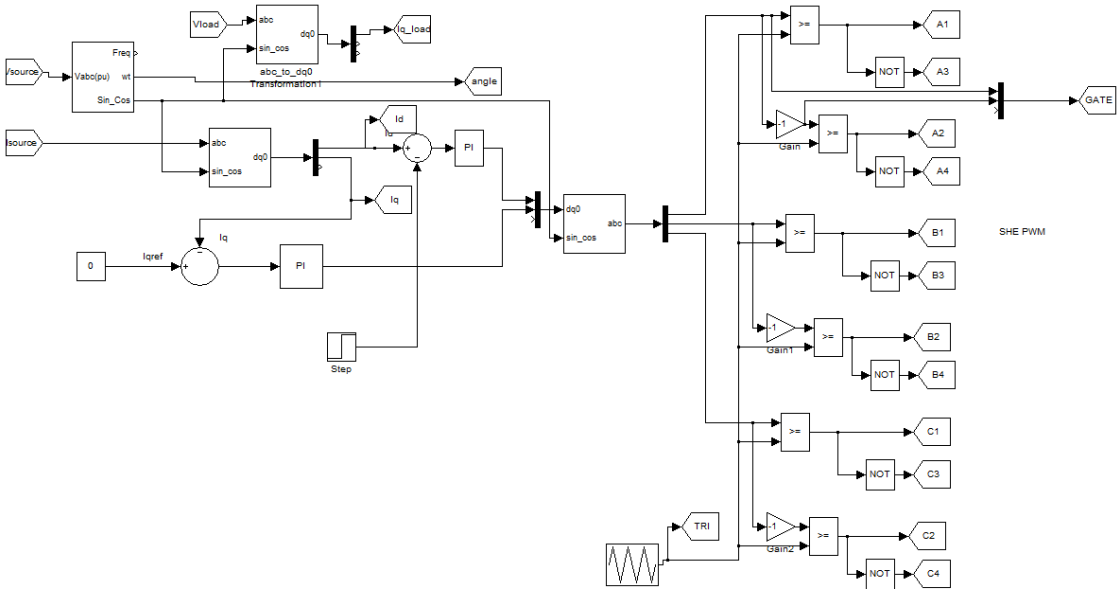

Fig. 3.3 Control Circuit with LVRT Operation and Control loop with SH-PWM.

A Control Circuit with LVRT Operation and Control loop with SH-PWM of proposed model has been shown in figure 3.3. Injecting reactive power for ensuring LVRT can be performed using var compensator devices such as STATCOM or capacitor banks. reducing power system cost can be an excellent motivation for minimizing STATCOM capacity that ensures LVRT

IV. SIMULATION RESULTS

Here the simulations were done on the matlab Simulink, the above diagrams show the output voltage and current waveform of the cascaded multi-level inverter. In the simulation that we performed for the seven levels cascaded multilevel inverter with the voltage of 80 volts to each H-bridge inverter and lagging load is considered to include the effect of the practical situations.

Here the concept of the selective harmonic elimination is applied in the firing circuit which was not shown which is hard to understand at this moment but the main observation which we should consider is in the output voltages for different modulation indexes is due to the error in the solution vectors of the switching angles and the truncation and the rounding off errors in this digital simulation results the improper functioning of the total simulation circuit that is the desired harmonics which should be eliminated are not completely getting eliminated.

Simulation outcome waveform of proposed work has been shown in below figures. In figure 4.1 a 1 grid voltage & current waveform of proposed system has been shown.

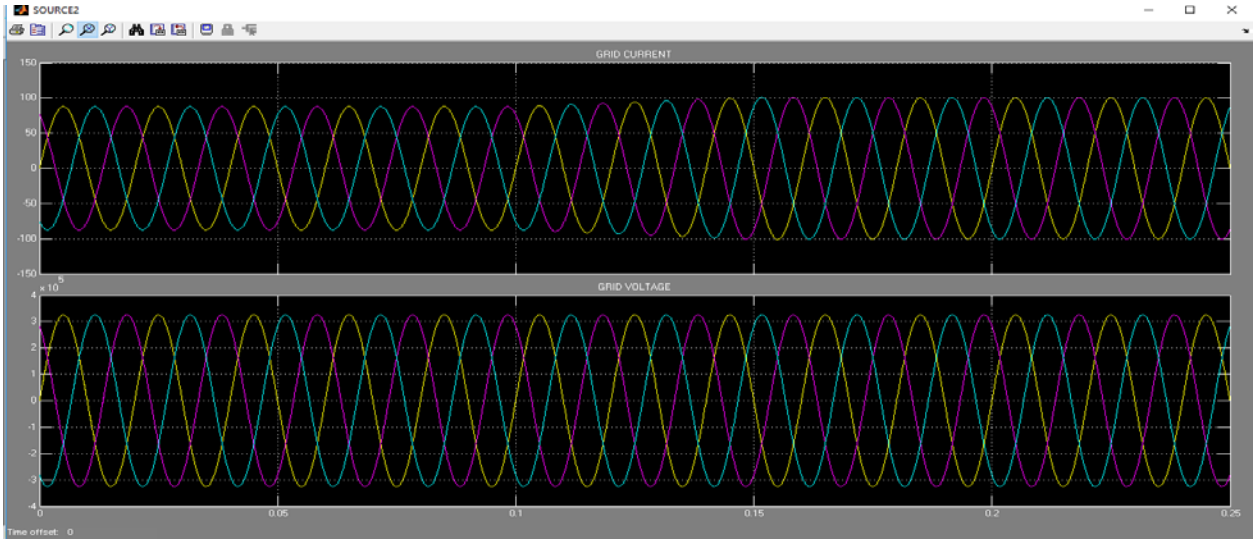

Fig. 4.1 Grid Voltage & Current.

STATCOM or Compensator Voltage & Current waveform of proposed system has been shown in figure 4.2 and Load Voltage & Current waveform of proposed model has been shown in figure 4.3.

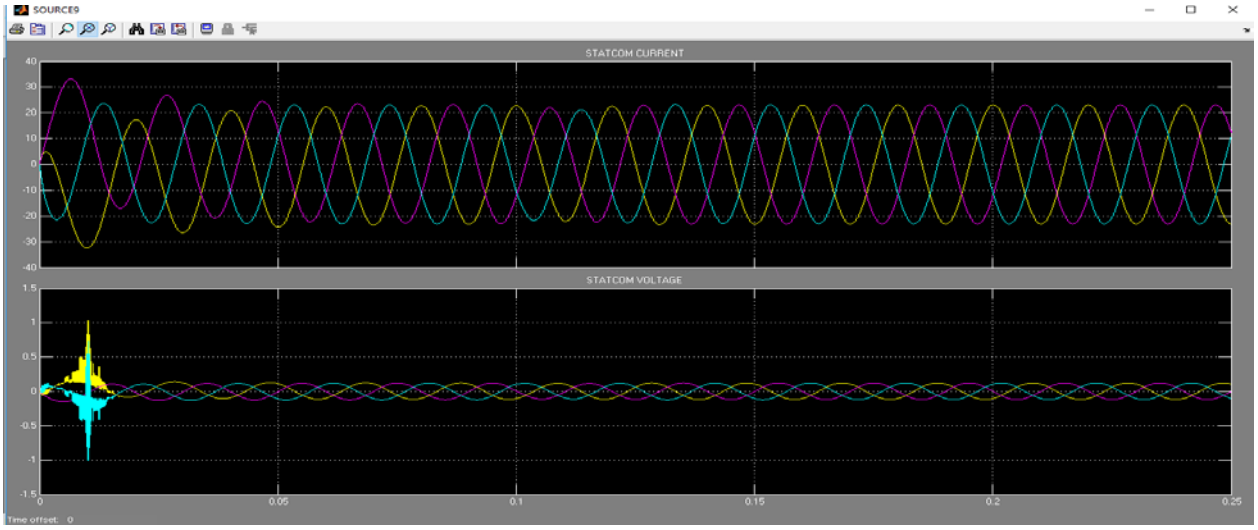

Fig. 4.2 STATCOM or Compensator Voltage & Current.

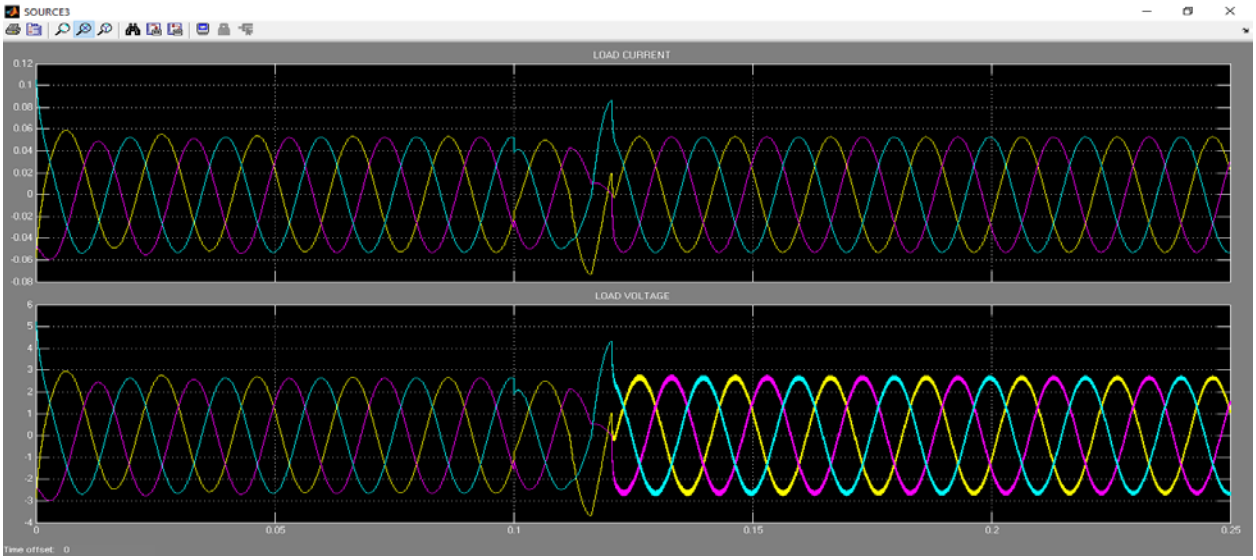

Fig. 4.3 Load Voltage & Current

In figure Fig. 4.4 a Single Phase Converter Current has been shown and DC voltage waveform has been shown in figure 4.5. The main advantage of the proposed strategy which is used is simplicity in the control for large number of the inverter modules in the cascaded multilevel inverter.

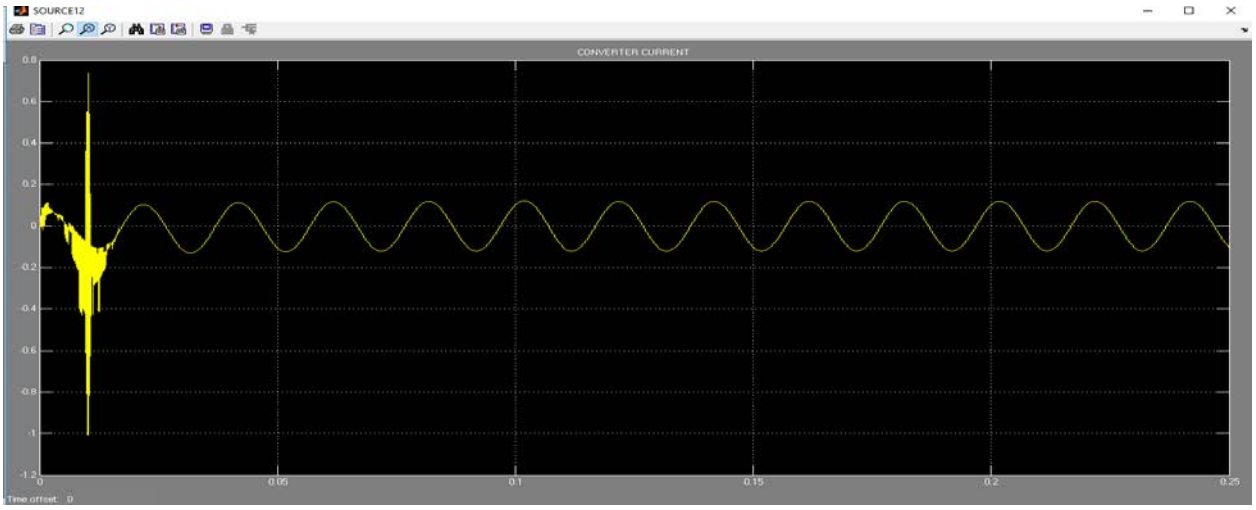

Fig. 4.4 Single Phase Converter Current.

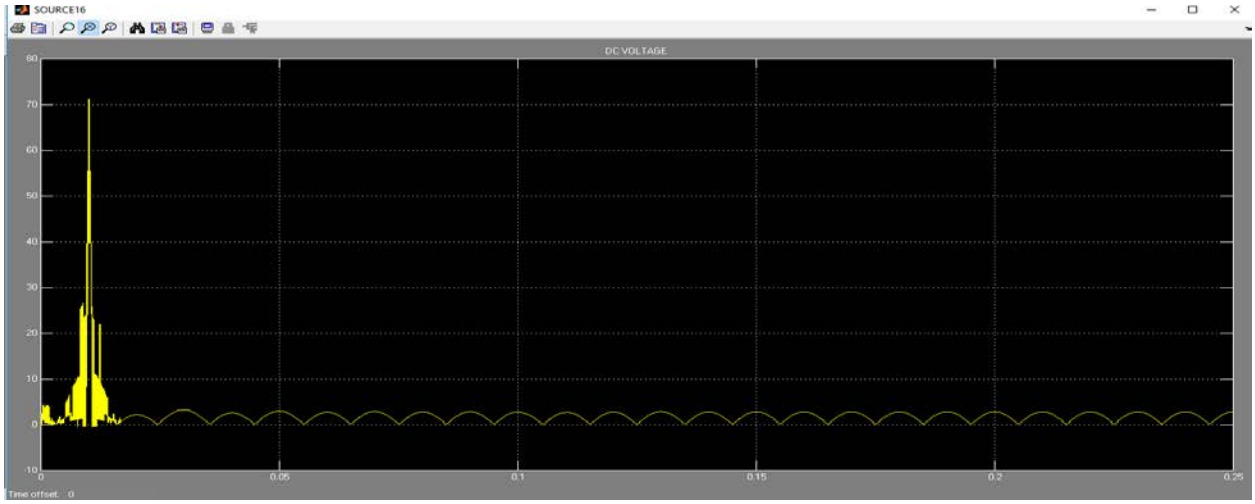

Fig. 4.5 DC voltage.

V. CONCLUSION AND FUTURE SCOPES

The key issue for multilevel inverter modulation is the harmonic elimination. All unbalanced or nonlinear loads draw harmonic currents. Those harmonics cause a lot of problems, such as distorted voltage, voltage flicking, overheated transformer, high torque ripple in the generator, severe EMI noise to communication systems and computer systems. But as mentioned above, traditional PWM schemes have the inherent problems of producing Electro Magnetic Interference (EMI). Rapid changes in voltages (dv/dt) are a source of EMI. The objective of this research exploration is to develop a simple and efficient control method for minimizing harmonic distortion. A specific harmonic PWM based cascaded multilevel inverter with Adjustable DC voltage levels control for STATCOM applications has been executed in this work. The control circuit for the cascaded multilevel inverter is was simulated in the matlab Simulink. The selective harmonic cancellation strategy has developed as a promising harmonic elimination technique for voltage source inverter.

The proposed selective harmonic eliminator methods in this work are for a time variant systems. This accepts all the equivalent or unequal voltages won't change with time. However, the voltages for a mealtime system will change with time. Hence, it is prescribed to propose another real time calculation to wipe out harmonics for time variation systems.

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