Delay Efficient Reversible RAM Design

Amit Kumar Tiwari[1], Prof. Bhagwat Kakde[2], Dr. Bharti Chourasia[3]

[1]Mtech Scholar, [2]Research Guide, [3]HOD

Department of Electronics and Communication Engineering, RKDF Institute of Science and Technology, Bhopal

Abstract - Reversible logic implementations are such that the estimations of info factors can be reasoned from the output values. Data loss does not contribute to heat dissipation in these circuits. Therefore, they potentially help to solve at least two problems: overheating and power saving, which implies longer life for batteries. The reversible logic arrangement might be particularly vital in low-voltage outlines of versatile frameworks, where both power saving and overheating are very important due to the need for light weight and independent power supply. Reversible implementations have applications in quantum computing and nanotechnology. Quantum innovation has received altogether more consideration, and is frequently thought to be the most encouraging application for reversible computations. Consequently, in work, proposed an efficient 32 bit reversible ram.

Keywords- Reversible Logic; Quantum Cost; Reversible D-FF; Reversible Decoder; RRRAM.

I. INTRODUCTION

Since ancient times, humanity has been seeking tools to help us perform tasks which involve calculations. Such are computing the area of a land, computing the stresses on rods in bridges, or finding the shortest route from one place to another. A common feature of all these tasks is their structure:

$$\boldsymbol{Input} \; ---> \; Computation \; ---> \; Output$$

The calculation some portion of the procedure is unavoidably performed by a dynamical physical framework, advancing in time. In this sense, the question of what can be computed is intermixed with the physical question of which frameworks can be physically figured it out. In the event that one needs to play out a specific calculation assignment, one ought to look for the suitable physical framework, with the end goal that the development in time of the framework compares to the coveted calculation prepares. If such a system is initialized according to the input, its final state will correspond to the desired output.

Reversible logic has caught critical consideration in late time as diminishing power utilization is one of the fundamental worry of advanced logic. It devours less power by recouping bit misfortune from its one of a kind info yield mapping. In this work, we propose a reversible fault tolerant move enlist, binary adder and multiplier which is first ever proposed in literature. Those register is one of the most important parts of any central processing Unit. A few Researchers have been led to make the reversible fault tolerant gates, successfully. Reversible calculation safeguards the coordinated mapping amongst info and yield vector by including refuse yields. The exploration objectives for any reversible calculation are to perform calculation with critical lessening of reversible gates and cost. Less number of steady info and trash yield. Fault tolerant reversible calculation is generally new for shift register, binary adder and multiplier.

A. Universal Quantum Gates

What kind of elementary gates can be used in a quantum computation program? We would like to write our program using elementary steps: i.e., the algorithm should be a sequence of steps, each potentially implementable in the laboratory. It seems that achieving controlled interactions between a large numbers of qubits in one elementary step is extremely difficult. Therefore it is reasonable to require an “elementary gate” to operate on a small number of qubits, (independent of n which can be very large.) We want our computer to be able to compute any function. The set of elementary gates used should thus be universal. For classical reversible computation, there exists a single universal gate called the Toffoli gate.

$$a, b, c \; ----\rightarrow a, b, ab \oplus c.$$

The claim is that any reversible function can be represented as a concatenation of the Toffoli gate on different inputs. For example, to construct the logical AND gate on a, b, we simply input c = 0, and the last bit will contain $ab \oplus 0 = AND(a, b)$. To implement the NOT gate on the third bit we set the first two bits to be equal to 1. We now have what is well known to be a universal set of gates, The NOT and AND gates. In the quantum case, the notion of universality is slightly more complicated, because operations are continuous. We need not require that all operations are achieved exactly, but a very good approximation suffices. The notion of approximation is very important in quantum computation. Frequently operations are approximated instead of achieved exactly, without significantly damaging the correctness of the computation.

B. Quantum Algorithm

The first and simplest quantum algorithm which achieves advantage over classical algorithms was presented by Deutsch and Jozsa. Deutsch and Jozsa's algorithm addresses a problem which we have encountered before, in the context of probabilistic algorithms.

f is a Boolean function from {1, N} to {0,1}. Assume N = 2n for some integer n. We are promised that f (i) are either all equal to 0, ("constant") or half are 0 and half are 1 ("balanced"). We are asked to distinguish between the two cases.

II. REVERSIBLE GATE

An $N \times N$ Reversible gate is a data stripe block that uniquely maps between input vector Iv = (I_o,I_i, ..,.In-1) and output vector O_v = (O_o ,O_i, . . . ,O_n-1) denoted as Iv ←→O_v. Two prime requirements for the reversible logic circuit are as follows:

- There should be equal number of inputs and outputs.
- There should be one-to-one correspondence between inputs and outputs for all possible input-output sequences.

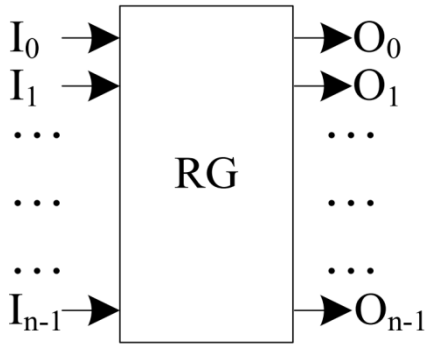

Fig.2.1 A $n \times n$ Reversible Gate.

Every gate output that is not used as input to other gates or as a primary output is known as garbage. Unused output of a reversible gate (or circuit) is known as garbage output, i.e. the output which are needed only to maintain the reversibility is the garbage output.

III. PROPOSED ARCHITECTURE

A RAM can be viewed as a 2-D array of flip-flops. In the proposed structure, 2 number of rows and j numbers of columns are present. Based on the given pattern at the input of reversible decoder, only one of the 21 output lines gets activated to select a single row of master-slave D flip-flops. Figure 3.1 demonstrate the architecture of proposed RAM.

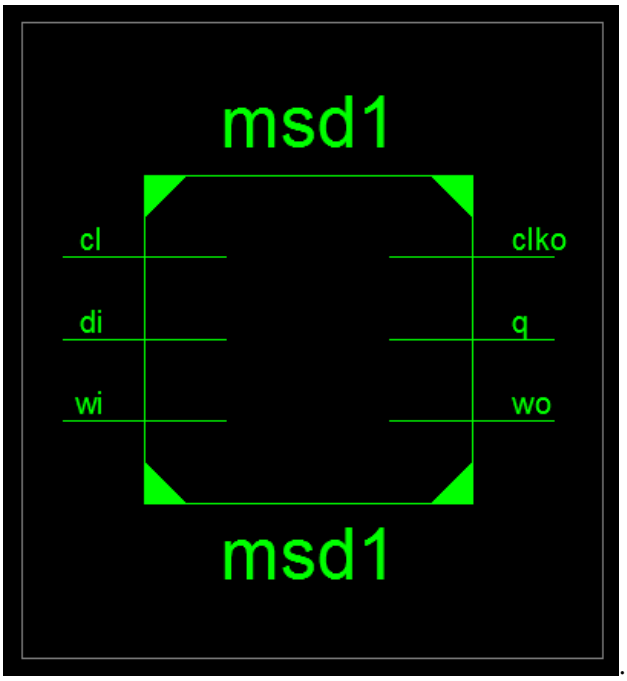

Fig. 3.1 RTL schematic of Ram_2_4.

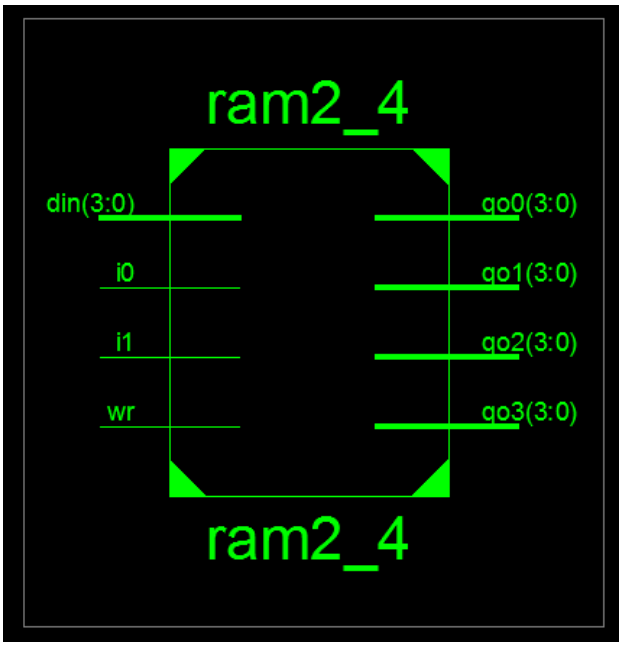

Fig. 3.2 RTL Schematic of ram2_4.

RTL schematic of Ram_2_4. Figure 3.2 RTL Schematic of ram2_4. and its corresponding internal technology schematic has been demonstrated n Figure 3.3. Figure 3.4 RTL schematic RAM 8_8, and Figure 3.5. Technology Schematic Ram_4_16. the result analysis of the proposed work has demonstrated in next section. Write signal decides when to read or write. When 'write' goes high, 'j' number of flip-flops of the selected row is written with the inputs Do to DJ. When, 'write' goes low, all the 'j' number of flip-flops of the selected row gets refreshed simultaneously with the previous bits at Qi to QJ The proposed internal architecture of reversible RAM can be realized below and the architecture is shown in figure.

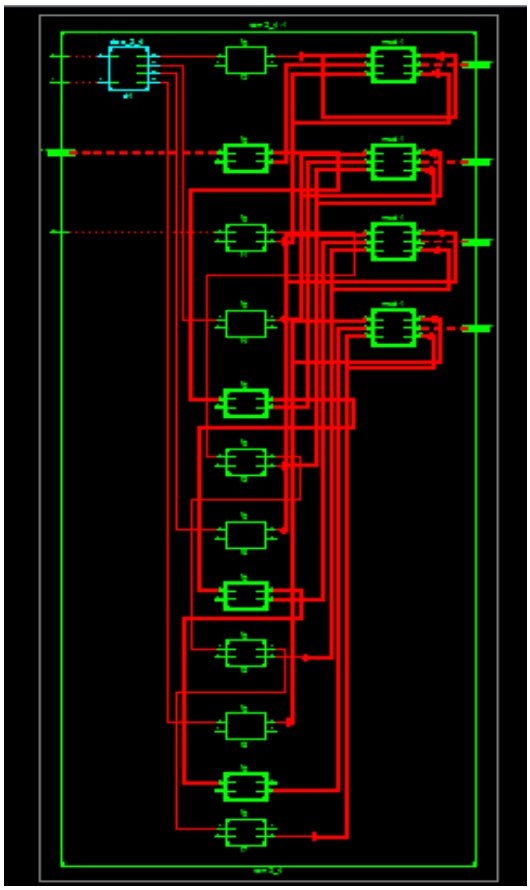

Fig. 3.3 Technology Schematic 4.3 .

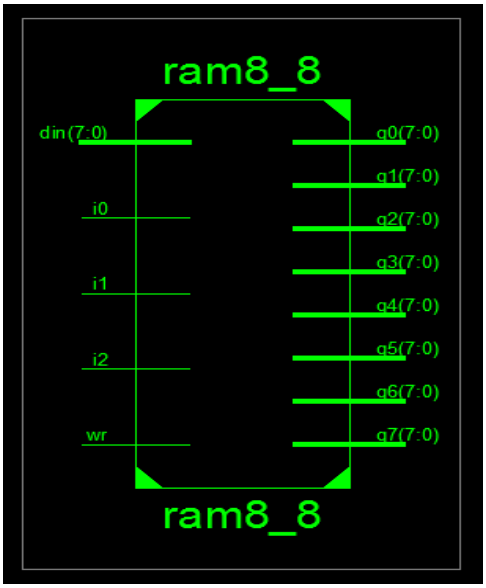

Fig. 3.4 RTL schematic RAM 8_8.

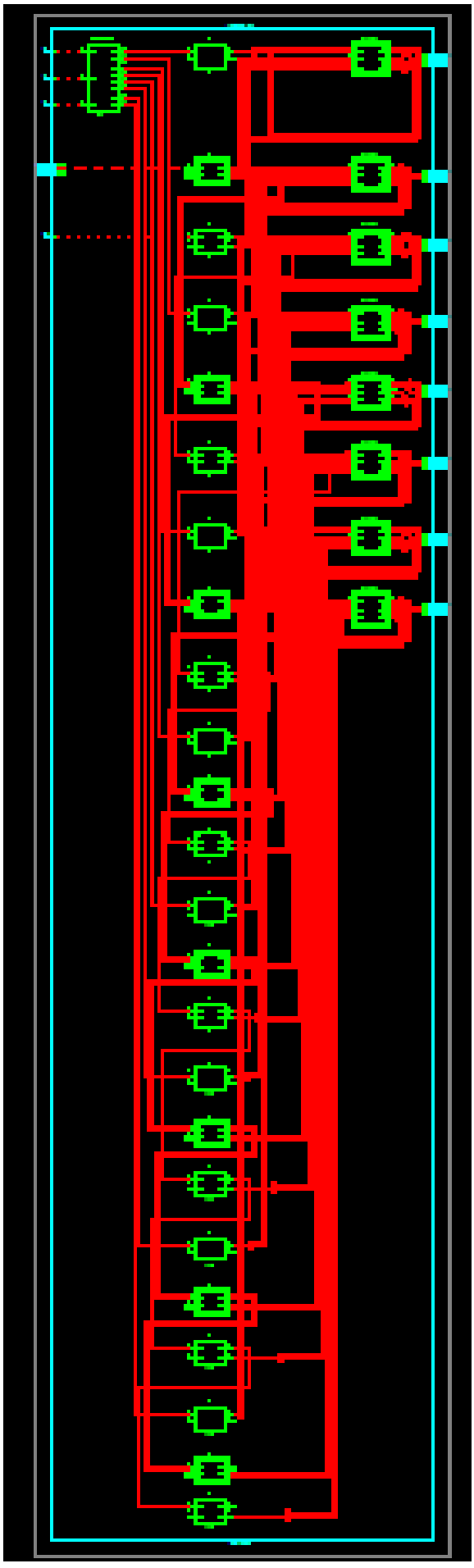

Fig.: 3.5 Technology Schematic Ram_4_16.

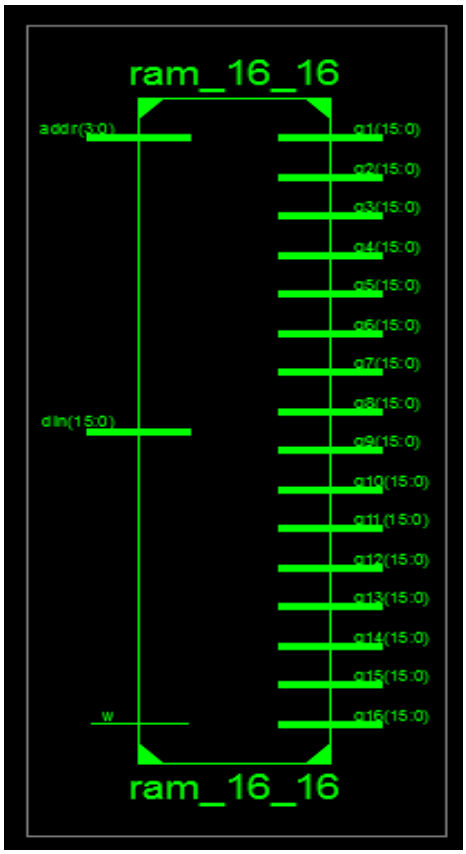

Fig. 3.6 RTL Schematic ram _16_16.

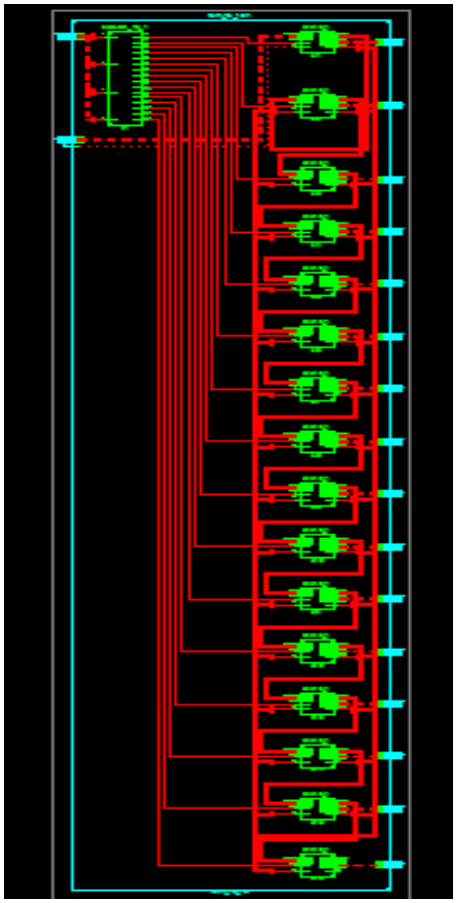

Fig. 3.7 Technology Schematic ram_16_16.

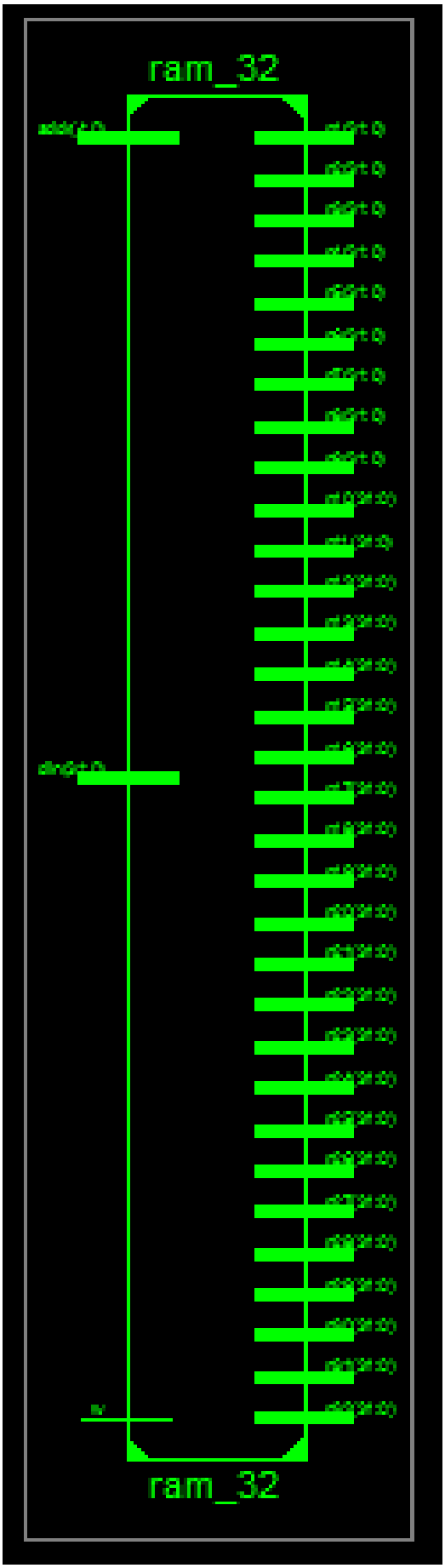

Fig. 3.8 RTL Schematic ram_32.

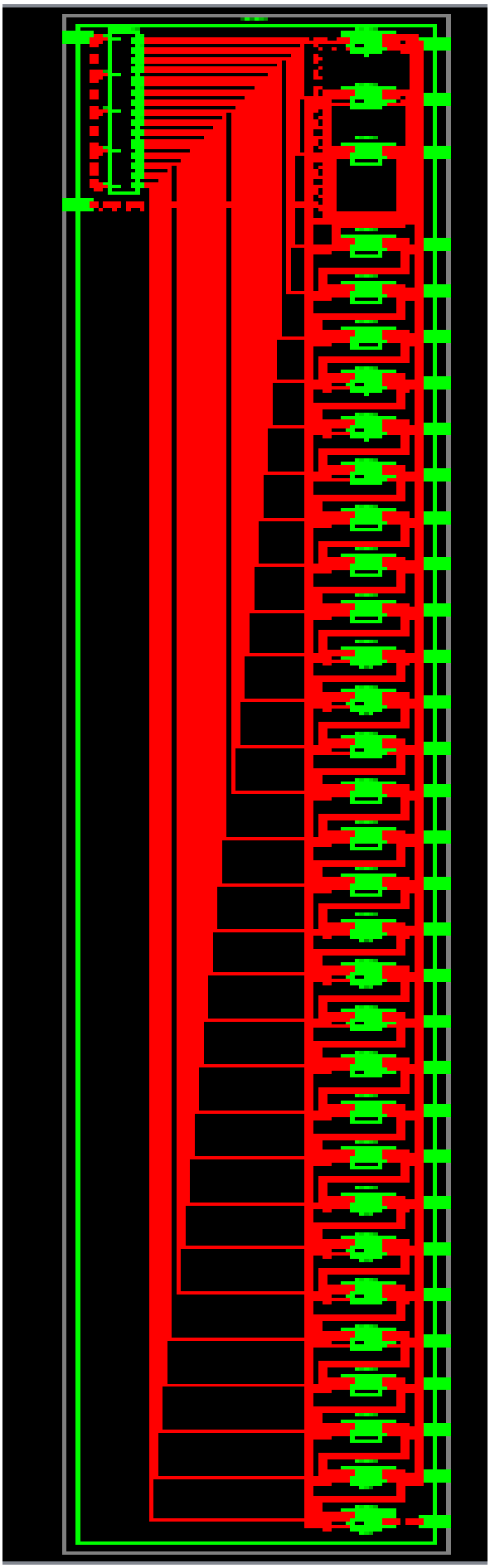

Fig. 3.9 Technology Schematic ram_32.

IV. SYNTHESIS AND OUTCOME

Simulation of the proposed work has done on Xilinx ISE HDL simulation platform the outcome of the test bench of the proposed system has give in figure below.

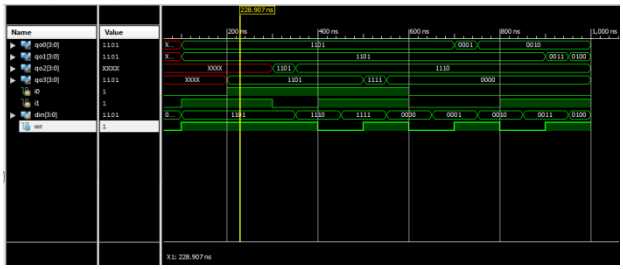

Fig.: 4.1 Ram 4 output.

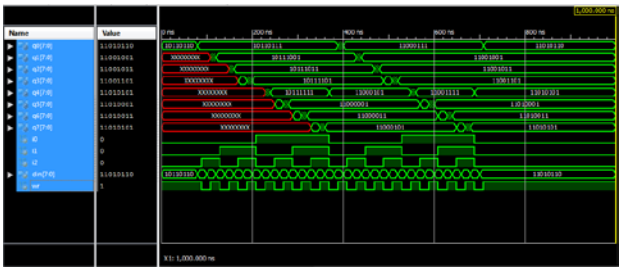

Fig.: 4.2 Ram_8.

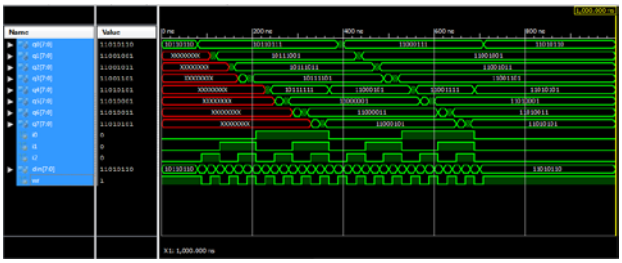

Fig: 4.3 Ram_16.

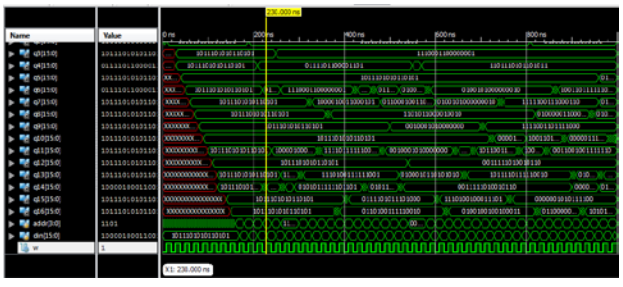

Fig: 4.4 Ram_32.

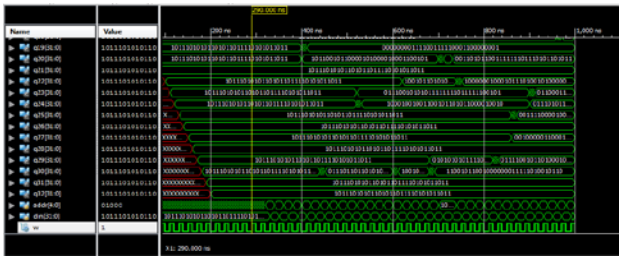

Fig: 4.5 Reversible masterslave dff.

Table 1: Cost Comparison of Equivalent Design of Proposed Circuit

Parameter	***Previous Design with 2X4 Decoder***	***Proposed Design with 4X16 Decoder (For Equivalent Ciruit of Previous Design)***
Delay	9 ns	6.211ns
Quantum Cost	9	9
Garbage Outputs	1	0

V. CONCLUSION

In this research work proposed an efficient Reversible RAM of 32 bit has implimented and synworked on Xilinx ISE HDL presented an efficient reversible/quantum synwork method for the RAM. As compared to the best previously reported method targeting the synwork of symmetric Boolean functions, our method uses simpler gates (resulting in technologically preferable circuit speci¬fications) and requires significantly less garbage bits. compared our designs to those presented previously and found that our circuits are smaller. presented reversible implementations for some well known symmetric benchmark functions whose reversible circuits were never reported before.

REFERENCES

[1] A. Majumder, P. L. Singh, N. Mishra, A. J. Mondal and B. Chowdhury, "A novel delay & Quantum Cost efficient reversible realization of $2^i \times j$ Random Access Memory," 2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), Bangalore, 2015, pp. 1-6.

[2] N. Pandey, N. Dadhich and M. Z. Talha, "Realization of 2:4 reversible decoder and its applications," 2014 International Conference on Signal Processing and Integrated Networks (SPIN), Noida, 2014, pp. 349-353.

[3] I. V. Anand and A. Kamaraj, "Design of combinational logic circuits for low power reversible logic circuits in quantum cellular automata," International Conference on Information Communication and Embedded Systems (ICICES2014), Chennai, 2014, pp. 1-6.

[4] D. Kunalan, C. L. Cheong, C. F. Chau and A. B. Ghazali, "Design of a 4-bit adder using reversible logic in quantum-dot cellular automata (QCA)," 2014 IEEE International Conference on Semiconductor Electronics (ICSE2014), Kuala Lumpur, 2014, pp. 60-63.

[5] N. J. Lisa and H. M. Hasan Babu, "A compact realization of a reversible quantum n-to-2n decoder," 2013 IEEE 4th International Conference on Electronics Information and Emergency Communication, Beijing, 2013, pp. 90-93.

[6] M. Shamsujjoha and H. M. H. Babu, "A Low Power Fault Tolerant Reversible Decoder Using MOS Transistors," 2013 26th International Conference on VLSI Design and 2013 12th International Conference on Embedded Systems, Pune, 2013, pp. 368-373.

[7] R. Wille, R. Drechsler, C. Osewold and A. Garcia-Ortiz, "Automatic design of low-power encoders using reversible circuit synwork," 2012 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, 2012, pp. 1036-1041.

[8] R.Landauer, “Irreversibility and heat generation in the computational process”, IBM Journal of Researh. Dev. 5, 183-191, 1961.

[9] C.H.Bennett, R.Landauer, “The fundamentals physical limits of computation”.

[10] Axelsen, H. B., Gluck, R., De Vos, A., and Thomsen, M. K. MicroPower: Towards low-power microprocessors with reversible computing. ERCIM News 79, 1 (2009), 20-21].

[11] C.H.Bennett, “Logical reversibility of computation”, IBM Journal of Research. Devel. 17, 525-532, 1973.

[12] Tommaso Toffoli, "Reversible Computing,' Automata, Languages and Programming, 7th Colloquium of Lecture Notes in Computer Science, vol. 85, pp. 632-644, 1980.

[13] E. Fredkin, T.Toffoli, “Conservative logic”, Int. J. Theor. Physics 21, 219-253,1982.

[14] A Peres, “Reversible logic and quantum computers”, Phys. Rev. A, Gen. Phys. 32, 6, 3266-3276, 1985.

[15] P. Picton, “Multi-valued sequential logic design using fredkin gates” MVL i. 1,241-251, 1996.

[16] J.Smolin, D.Divincenzo, “Five 2-bit quantum gates are sufficient to implement quantum Fredkin gate”, Phys. Rev. A 53, 2855-2856, 1996.