# Fault Tolerant FPGA Track Circuit For Railways Using Fuzzy Logic

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Abstract-In railway transportation, specific track circuits are used to guarantee that a specific track section is free for circulation of railway vehicles. Common track circuits consist of two signaling subsystems physically placed at two certain points of the rail track delimiting then a track section The main proposals for track circuits can be found in how to identify the presence of a vehicle in a certain section, the type of transmitted signals, and the way the measuring circuit is coupled to the railway tracks. In some of them train presence is basically detected by comparing the received signal amplitude with a certain threshold. The transmitted signals are captured and then analyzed to determine the train positions since the closer the train, the lower the received amplitude at the measuring system. Sometimes, the correlation with the transmitted signal is searched to increase confidence in the detection. furthermore, this system must be periodically calibrated since empty-track features can change according to the state of tracks, weather conditions, etc. Other systems encode the emitted signal, so the receiver can correlate the reception with this code and compare its value with a determined threshold. This encoding should be immune to any system noise. This work proposes a novel track circuit based on the encoding of the electrical transmissions with Kasami codes. Track circuit emitters send signals coded with a known sequence that can be identified by the corresponding receivers using correlation techniques; these processes increase immunity to noise and changes in environmental conditions. To increase the fault tolerant transmission reliability we use fuzzy logic control. An appropriate selection of orthogonal sequences for encoding, as well as different carrier frequencies for transmissions, allow simultaneous emissions and receptions without cross interference.

# Index Terms-Field-programmable gate array (FPGA) implementation, Kasami code-division multi-access, rail track circuit, railway traffic control.

## I. INTRODUCTION

In railway transportation, specific track circuits are used to guarantee that a specific track section is free for circulation of railway vehicles. Common track circuits consist of two signaling subsystems physically placed at two certain points of the rail track delimiting then a track section; most of the track circuits have an electrical emitter at one end and an electrical receiver at the other one. Whether a railway vehicle is inside a certain track section, their axles will electrically connect both rails, which will avoid any emitted signal to reach the receiver end; this fact is somehow detected by the track circuit, which will classify this section as occupied. Each track section is isolated from adjoining sections by using electrical filters or isolation sections to avoid signal propagation among different track sections.

Furthermore, the extended use of electrical trains, together with the current control technologies of electrical engines, has forced an evolution in the research and design of track circuits. This evolution has several guidelines: to deal with noisy environments, to improve reliability under perturbations, and to simplify maintenance operation. The main differences among proposals for track circuits can be found in how to identify the presence of a vehicle in a certain section, the type of transmitted signals, and the way the measuring circuit is coupled to the railway tracks.

Field-Programmable Gate Arrays (FPGAs) are readily available, multi-sourced components which have a proven place in development, small-scale production, and even large-scale production runs. One style of field-programmable gate array uses static RAM to dynamically configure both the function of the logic cells and their interconnections. Current examples of large-scale FPGAs in this style are the Xilinx 3000 and 4000 series the Electrically Reconfigurable Array and the Logic Cell Array devices..In some of them train presence is basically detected by comparing the received signal amplitude with a certain threshold.

Other systems encode the emitted signal, so the receiver can correlate the reception with this code and compare its value with a determined threshold. This encoding should be immune to any system noise source including Gaussian, impulsive, and burst noise, as well as more significant interferences coming from frequency components in traction return currents. Furthermore, the root mean square (RMS) voltage of signals measured in the track can be analyzed, therefore, if the RMS is high but the correlation value is low, there is an error in the measurement. Some other solutions use sinusoidal tones coupled to tracks with circuits tuned at specific frequencies to discriminate among different emitters and receivers. These are complex methods since the tuning process has to include track parameters, which are often a function of the track state (rails and ballast), weather, and other environmental conditions.

The transmitted signals are captured and then analyzed to determine the trains position since the closer the train, the lower the received amplitude at the measuring system. Sometimes, the correlation with the transmitted signal is searched to increase confidence in the detection. Furthermore, this system must be periodically calibrated since empty-track features can change according to the state of tracks, weather conditions, etc.

## II. RELATED WORK

Intelligent transport systems (ITS)[1] are advanced applications which, without embodying intelligence as such, aim to provide innovative services relating to different modes of transport and traffic management and enable various users to be better informed and make safer, more coordinated, and 'smarter' use of transport networks. in the field of road transport and for interfaces with other modes of transport defines ITS as systems in which information and communication technologies are applied in the field of road transport, including infrastructure, vehicles and users, and in traffic.

Track circuits allow railway signaling systems [2] to operate semi-automatically, by displaying signals for trains to slow down or stop in the presence of occupied track ahead of them. They help prevent dispatchers and operators from causing accidents, both by informing them of track occupancy and by preventing signals from displaying unsafe indications. A track circuit typically has power applied to each rail and a relay coil wired across them. When no train is present, the relay is energized by the current flowing from the power source through the rails. When a train is present, its axles short (shunt) the rails together; the current to the track relay coil drops, and it is de-energized. Circuits through the relay contacts therefore report whether or not the track is occupied. Modern track is often continuously welded, the joints [3] being welded during installation. This offers many benefits to all but the signaling system, which no longer has natural breaks in the rail to form the block sections. The only method to form discrete blocks in this scenario is to use different audio frequencies (AF) in each block section. To prevent the audio signal from one section passing into an adjacent section, pairs of simple tuned circuit are connected across the rails at the section boundary. The tuned circuit often incorporates the circuit to either apply the transmitted signal to the track or recover the received signal from the other end of the section.

The ground to train transmission system (TVM)is a vital factor in railway safety on high speed lines. It is used to continuously transmit signaling information to the driver in the cab. The ground-based part of the system consists of a compensated UM71-type track circuit including a transmitter, a receiver and timing capacitors, whose characteristics may change because of ageing of track maintenance operations.

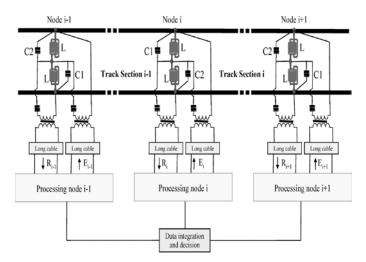


Fig. 1.Global structure of the proposed track circuit.

This can lead to serious defects and even interrupt the TVM. It is therefore important to detect the defects as early as possible to maintain the system safe and variable. In this paper, we propose a diagnosis method based on a local electrical modeling of the track circuit. The TVM carrier signal is simulated, and the parameters of the local model are optimized so that the simulated signal is as close as possible to the real measured one, recorded by an inspection vehicle. It makes it possible both to detect the track circuit defects, and to estimate their graveness.

#### **III. PROBLEM DEFINITION**

More recently, four U.S. Class one railroads started to work towards a unified, interoperable concept. It will consist of a PTC system providing a monitoring, control, and safety overlay above existing train signaling and control systems. This system will communicate with and monitor trains and high-rail vehicles as they move. It will determine their exact position and speed at any time, using specialized software in fault-tolerant network operations centers to monitor multiple simultaneous train operations. Events including conflicts, loss of separation between trains, operation outside established limits and excessive speed will result inimmediate action to avoid potential accidents. This document provides an outline of how train control and railroad communications systems evolved through the years, from early Morse key telegraph to wireless PTC systems, which have to operate 24/7/365 as mission critical, vital railroad signaling systems. Unlike voice mobile radio, PTC requires seamless radio coverage of tracks. Final PTC requirements are still being defined by the main Class One Railroads.

PTC will include state-of-the-art, mission critical, fault tolerant data networks and digital wireless communications systems. Initially, PTC will be deployed as an overlay on existing train control and signaling systems, including track circuits, blocks and track side equipment. In the future, PTC will support the migration to a moving block concept where more trains can be operated over the same section of track. With PTC monitoring and maintaining train separation for safe operations, it will provide in-cab signals to locomotive engineers, and will not require physical block systems or track side signals.

In analog integrated circuits, the recent trend toward miniaturized circuits has given a decisive boost towards low voltage low-power design, widely used in portable system applications. The most efficient way to reduce power consumption is to decrease both the supply voltage and the Stand-by current. Reducing the supply voltage makes it difficult to implement efficient analog circuits, so novel circuit architectures have to be developed. The values of the current sources inside the amplifiers are the main cause of quiescent power dissipation. Adaptive biasing techniques boost the bias current of the input differential pair when large signals are applied, thus, increasing circuit dynamic characteristics without affecting stand-by dissipation [2]. In this paper, we present a novel rail-to-rail fully differential OTA, showing low-voltage low-power characteristics, where DC gain has been enhanced by a suitable technique which increases the output impedance of the operational transconductance amplifier (OTA) input stage through positive feedback.

#### IV. PROBLEM EVALUATION

FPGA programming pins, such as joint test action group (JTAG) pins, may be subject to noise if not pulled up or down by resistors. This noise can either alter or erase the configuration memory. Also, FPGAs with external configuration memory require specific rules for the layout of the connections between the external configuration memory and the FPGA programming pins. To prevent accidental or malicious reconfiguration of CPLDs or external configuration programmable read-only memories (PROMs), the configuration memory should be write-protected by using write security bits. Malicious reconfigurations should be prevented by design and/or by administrative controls. For example, the FPGA design can include error detection circuitry or built-in self-test (BIST) to constantly monitor the health of the FPGA system. Making JTAG connector physically accessible only to the trusted personnel may be one of the administrative measures.

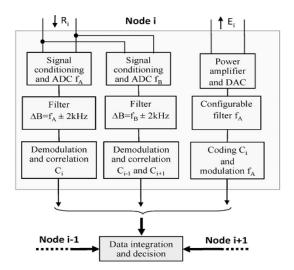


Fig.2.Detailed block diagram of a processing module for a generic node *i* 

Shrinking process geometry and reduced supply voltages in FPGAs have resulted in enormous growth in terms of their computational capability and power efficiency. The growth in FPGA computational capability versus process geometry. FPGAs are about an order of magnitude more capable than

programmable processors and an order of magnitude less capable than full custom VLSI. Furthermore, the gap between FPGAs and microprocessors is widening, as FPGA vendors use increased density to increase the number of logic cells, whereas microprocessor developers often use increased density for caches and reducing die size. The growth in the computational capability of FPGAs for DSP applications as a function of time in billions of 16-bit arithmetic operations per second.

#### Rail track circuit:

The proposal for the track circuit is based on the simultaneous use of frequency-division multiple access and code-division multiple access techniques. Both emitters (Ei) and receivers (Ri) are placed in locations that separate the different track sections to be monitored [3]. Every emitter Ei and receiver Ri is coupled to track using a soft-tuned passive circuit to separate traction current components.

Every emitter Eitransmits through the railway a signal that consists of a binary code ci and binary shift phase-keying (BPSK) modulated by a carrier frequency fA or fB .The selection of carrier frequencies fA and fB is configured in such a way that, if an emitter Ei uses fA, then the next one Ei+1 will use fB, and vice versa. The emission is transmitted in both directions, so it can be detected at any point of the track. The discrimination among different emissions is possible due to the encoding, as well as to the alternative carrier frequencies fA and fB.

Let us define a node i in the railway as a set of an emitter Ei and receiver Ri; then, any pair of consecutive nodes will define a track section. Every node i can work in two different modes (A or B), depending on the frequency used for the trans-mission. For instance, let us suppose that node i is in mode A; then, its transmitting frequency is fA, and their adjacent nodes (i - 1 and i + 1) must be fixed to mode B. Regarding the codes, every node i emits its own code ci and searches at the reception stage for the codes coming from the next nodes i - 1 and i + 1 (sent at fB), as well as its own code ci (sent at fA); this last check is done for safety reasons to verify that node i itself is properly working. On the other hand, if node i were in mode B, emitter i would transmit code ci at a frequency fB, whereas the receiver would search for codes ci-1 and ci+1 at fA, and code ci at fB.

The detection of a train in the track circuit will be carried out by analyzing the amplitude of the correlation output in the reception stage. This amplitude can be processed by different alternatives of thresholds.

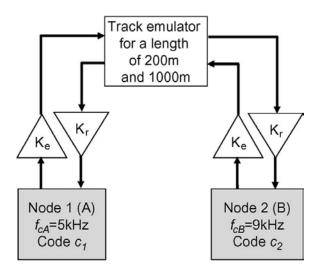


Fig.3.Experimental setup used for validation

Anyway, the shunt resistance presented by the train becomes an important factor when fixing a threshold for the detection of trains. The correlation outputs obtained at node i for the transmission coming from node i +1 are shown in Fig. 4 for the following values of the shunting resistance: 0.1, 1, 2, 3, 5, and 10  $\Omega$ . The system behavior has been simulated for a 1km-long track circuit, with a train placed at 0.5 km from each node. As can be observed, the presence of a train with a shunting resistance below 5  $\Omega$  is provoked to not receive the transmissions between nodes. For higher resistances, the typical maximum values from the correlation function are not attenuated enough, which implies that the transmissions could be detected by nodes.

The emission and reception system is directly coupled to the track by means of two LC resonant circuits. This coupling requires a low quality factor Q since bandwidth is necessary for encoding transmissions (about 20% over the carrier frequency in the modulation)[4]. Furthermore, this makes possible the coupling of the signal emitted by a node i to the receiver in the same node i. This allows a node i to detect its own transmission and check the correct link from the processing module to the coupling point in the track.

As the coupling is less dependent on the resonance frequency and on the global bandwidth than other systems without encoded signals, it provides more reliability and availability. The proposal requires the detection of all the transmissions to consider the track as free, so any fault in the system implies a safe situation since some transmissions will be lost. Finally, the proposal tries to improve previous track circuits, simplifying the coupling elements by enhancing the signal processing. Only the elements improved by the proposal are considered in the succeeding sections, and therefore, those elements common to any track circuit (overvoltage suppressors, protection against surges and transients, etc.) are not described. The proposed track circuit is oriented to train railways, with 25-kV 50-Hz traction supply, although it could be applied to other cases.

# Fault tolerant FPGA:

In recent years the application space of reconfigurable devices has grown to include many platforms with a strong need for fault tolerance. While these systems frequently contain hardware redundancy to allow for continued operation in the presence of operational faults, the need to recover faulty hardware and return it to full functionality quickly and efficiently is great. In addition to providing functional density, FPGAs provide a level of fault tolerance generally not found in mask-programmable devices by including the capability to reconfigure around operational faults in the field. Incremental CAD techniques are described that allow functional recovery of FPGA design configurations in the presence of single or multiple operational faults. If initial recovery attempts through localized swapping fail, an incremental router based on the widely-used Path Finder maze routing algorithm can be applied remotely in an attempt to form connections between newly-allocated logic and interconnect based on the history of the initial design route. If a fault is discovered on a remote embedded system, fault information can be transferred to a computationally-superior reconfiguration server via a network.

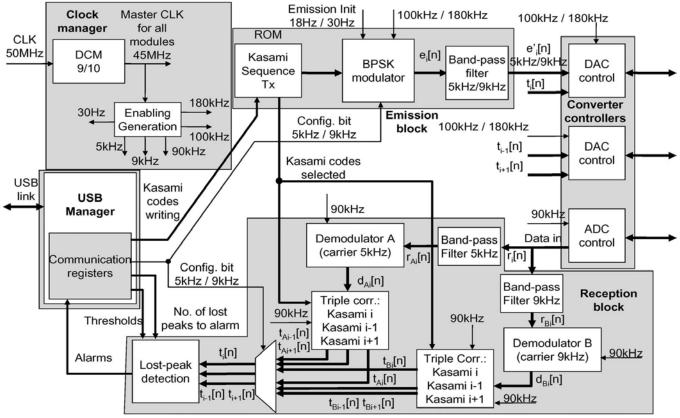


Fig.4. Global block diagram of the hardware implementation inside the FPGA device.

The CLB usually consists of three types of logic modules: D flip-flops, multiplexers and look-up tables (LUTs). Multiplexers and LUTs are typical configurable devices, while D flip-flops are not really configurable, although their asynchronous control signals (reset, clock) are configurable by means of multiplexers. Our approach detects the faults at

the application system level, so it can detect CLB faults or the routing switches and wires faults. However, our fault location algorithm can locate faults only in the CLBs, therefore we presume that the CLBs may be faulty, while the switches and wires are fault-free. For instance, LUT faults are such that any number of the configuration bits could be stuck-at or could have address line faults (functional inputs). In our approach, any number of faulty CLBs can be detected. There are two classes of faults, the first containing faults that are independent and identically distributed (iid), i.e., uniformly distributed faults, where each element fails with independent probability. Secondly, there are non uniform faults (clustering model), which postulate the existence of non-overlapping regions, alternatively known as quadrats or blocks. Fault-detection latency also increases as a result of an off-line approach.

#### Fuzzy control:

The purpose of control is to influence the behavior of a system by changing an input or inputs to that system according to a rule or set of rules that model how the systemoperates. The system being controlled may be mechanical, electrical, chemical or any combination of these.

Classic control theory uses a mathematical model to define a relationship that transforms the desired state (requested) and observed state (measured) of the system into an input or inputs that will alter the future state of that system.

The most common example of a control model is the PID (proportional-integral- derivative) controller. This takes the output of the system and compares it with the desired state of the system.

It adjusts the input value based on the difference between the two values according to the following equation.

$$butput = A.e + B.INT(e)dt + C.de/dt$$

Where, A, B and C are constants, e is the error term, INT(e)dt is the integral of the error over time and de/dt is the change in the error term.

The major drawback of this system is that it usually assumes that the system being modeled in linear or at least behaves in some fashion that is a monotonic function. As the complexity of the system increases it becomes more difficult to formulate that mathematical model Fuzzy control replaces, in the picture above, the role of the mathematical model and replaces it with another that is build from a number of smaller rules that in general only describe a small section of the whole system. The process of inference binding them together to produce the desired outputs.

Most commercial fuzzy products are rule-based systems that receive current information in the feedback loop from the device as it operates and control the operation of a mechanical or other device. A fuzzy logic system has four blocks as shown in Fig.. Crisp input information from the device is converted into fuzzy values for each input fuzzy set with the fuzzification block [5]. The universe of discourse of the input variables determines the required scaling for correct per-unit operation. The scaling is very important because the fuzzy system can be retrofitted with other devices or ranges of operation by just changing the scaling of the input and output.

The decision-making-logic determines how the fuzzy logic operations are performed (Sup-Min inference), and together with the knowledge base determine the outputs of each fuzzy IF-THEN rules. Those are combined and converted to crispy values with the defuzzification block. The output crisp value can be calculated by the center of gravity or the weighted average. Fuzzy Control Fuzzy control, which directly uses fuzzy rules is the most important application in fuzzy theory

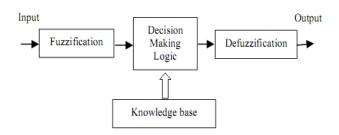


Fig. 5.Block Diagram of Fuzzy logic system

1) Fuzzification (Using membership functions to graphically describe a situation)

2)Rule evaluation (Application of fuzzy rules)3) Defuzzification consider the following classic situation: the inverted pendulum. Here, the problem is to balance a pole on a mobile platform that can move in only two directions, to

the left or to the right. The angle between the platform and the pendulum and the angular velocity of this angle are chosen as the inputs of the system. The speed of the platform is chosen as the corresponding output.

Fuzzy controllers are very simple conceptually. They consist of an input stage, a processing stage, and an output stage. The input stage maps sensor or other inputs, such as switches, thumbwheels, and so on, to the appropriate membership functions and truth values. The processing stage invokes each appropriate rule and generates a result for each, then combines the results of the rules [6]. Finally, the output stage converts the combined result back into a specific control output value.

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# Fig. Resource utilization

The most common shape of membership functions is triangular, although trapezoidal and bell curves are also used, but the shape is generally less important than the number of curves and their placement [7]. From three to seven curves are generally appropriate to cover the required range of an input value, or the "universeofdiscourse" in fuzzy jargon.

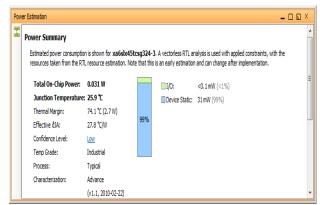


Fig. Power Estimation

Speed Grade: -3 (Timing Summary)

Minimum period: 1.415ns (Maximum Frequency: 706.714MHz)

Minimum input arrival time before clock: 3.421ns Maximum output required time after clock: 5.825ns Maximum combinational path delay: No path found

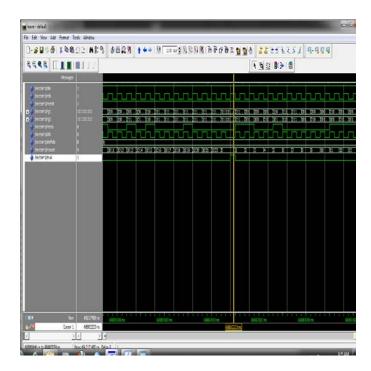


Fig. Correlated Simulation output

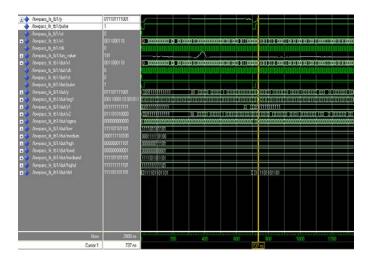


Fig .Simulation output

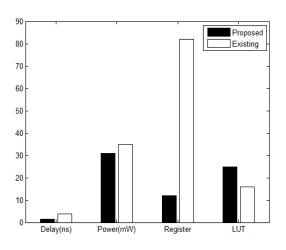


Fig. Comparison of existing and proposed systems

# V. CONCLUSION

A novel track circuit based on the encoding of the electrical transmissions with Kasami codes has been studied. It is possible to achieve satisfactory performances, even for reduced signal-to-noise ratios. To increase the fault tolerant transmission reliability we use fuzzy logic control. The experimental result with two nodes can be emulated with different distances to evaluate the performance of the proposal. Furthermore, the multiple emissions achieved without cross interference among encoded signals allows links to be established between successive track circuits, thus increasing detection reliability and railway safety. The correctness of the results has been checked up to distances of 1000 m, being capable of detecting transmissions coming from adjacent nodes and its own emission to check the correct operation of the node. As future works, the node implementation should be analyzed to provide fault tolerance and reliability and availability evaluations. Furthermore, tests in more realistic environments will be considered, as well as commercial manufacturing issues.

## REFERENCES

- [1] Álvaro Hernández, Juan JesúsGarcía, Ana Jiménez, Juan Carlos García, Felipe Espinosa, Mazo and JesúsUreña. "FPGA-Based Track Circuit for Railways UsingTransmission Encoding" IEEE Transactions on intelligent Transportation Systems, VOL. 13, no. 2, June 2012..
- [2] A. Debiolles, L. Oukhellou, P. Aknin, and T. Denoeux, "Track circuit automatic diagnosis based on a local electrical modeling," in Proc. 7<sup>th</sup> World Congress Railway Res., Montreal, QC, Canada, 2006.

- [3] P. Aknin, L. Oukhellou, F. Vilette. "Track circuit diagnosis based on automatic analysis of measurementrecords," in WCRR 2003, Edinburgh.L.Oukhellou, P.Aknin, A.Debiolles, F.Vilette, "Automatic diagnosis of track circuit in based on local electrical modelingt", Railway Engineering,
- [4] Ambika Prasad Patra, A. P., Kumar, U. and Larsson-Kraik, "Maintenance Decision Support Models for Railway Infrastructure using RAMS & LCC Analysis". Accepted for publication in Proceedings of Reliability and
- [5] Commission Decision 2002/731/EC 30 May 2002 on the technical specification for interoperability relating to "The control-command and signaling subsystem of the trans-European high-speed rail system", Official Journal L 245,12/9/2002.
- [6] Richard Bartoni, ReginaLamedica and Eugenio," FedeliAn Audio Frequency Model of a 2x25 kV Traction Line for High Speed Railway Systems"Proc. of the 5th WSEAS/IASME Int. Conf. on Electric Power Systems, High Voltages, Electric Machines, Tenerife, Spain, December 16-18, 2005 (pp562-567)
- [7] Giuseppe Ferri, Vincenzo Stornelli, and Angelo Celeste, "Integrated Rail-to-Rail Low-Voltage Low-Power Enhanced DC-Gain Fully Differential Operational TransconductanceAmplifier". ETRI Journal, Volume 29, Number 6, December 2007.