# A Survey and Taxonomy on the Leakage Reduction of SRAM

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***Abstract - Volatile memory strategies include Non-Volatile Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) devices. RAM devices in the prior art have been used for temporary data storage, such as during data manipulation, as writing information into, and reading information out of, the device is performed quickly and easily. However, a disadvantage of these devices is that they have short channel effects, such as loss of data, data retention is not good due to that the data may change its state internally, practically the shadow RAM, temporary files are the example of short channel effects. Needless to say, the SRAM is a fundamental component of most digital systems. However, SRAMs suffer from leakage currents thereby reducing the batter retention and also the lifetime. Several leakage reduction mechanisms have been devised so far. The paper presents a survey on the different leakage reduction techniques along with their salient features.***

***Keywords: Static RAM (SRAM), Power Dissipation, Power Gating, Double-Gate MOSFET (DG-MOSFET), sub-threshold, leakage.***

## I. INTRODUCTION

For over three decades there has been a quadrupling of transistor density and a doubling of electrical performance every 2-3 years. With the anticipation of unconstitutionality of Moore's law within a decade, researchers have embarked in exploring alternative technologies by harnessing the properties of channel materials, dielectric materials and gate work-function engineering that would provide us with high performance with nanoscale devices. Due to excellent control over short channel effects (SCEs), and better "ON" current, DG MOSFETs become one of the promising candidates. However, with continuous downscaling of device dimensions as well as aggressive scaling of oxide thickness, lead to exponential increase of leakage components, which leads to a large stand-by power dissipation. Thus leakage power management becomes indispensable in high-end microprocessors for cost effective solution. We will discuss the leakage components in 6-T SRAM cell using DG device. The total leakage in SRAM cell is substantially reduced using DG devices with sleep transistor. We will also discuss the effect of parameter variation in the DG SRAM cell due to independent gate control and advantage of the using independent gate control in DG devices in circuit design.

## II. POWER CONSUMPTION

Power consumption is now the major technical problem facing the semiconductor industry. For a digital circuit, the overall power dissipation, includes two components these are: - dynamic power and static power dissipation.

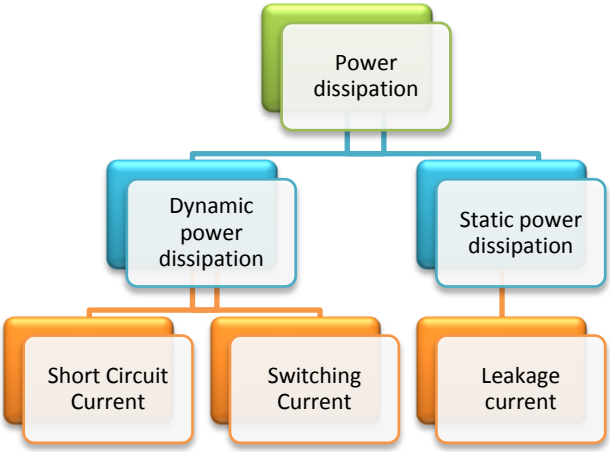


Fig. 2.1 Hierarchy of the Power Dissipation

The hierarchy helps to understand the way by which the power dissipation gets affected by the currents. The dynamic power dissipation is occurs due to the short circuit and switching current whereas the static power dissipation occurs due to the leakage current. Total power dissipation is expressed as-

$$P_{total} = P_{dynamic} + P_{static} \quad (2.1)$$

Where

Pdynamic = dynamic power dissipation.

Pstatic = static power consumption

**Dynamic power**

Dynamic power dissipaton is widely considered to be a repurcussion of the charging and discharging of the MOS capacitance.

The average dynamic power consumption is given by-

$$P_{dynamic} = C_L V_{DD}^2 f \quad (2.2)$$

Where,

$\mathbf{C_L}$ is the switching capacitance,

$\boldsymbol{f}$ is the operating frequency.

$\mathbf{V^2_{dd}}$ is the supply voltage

**Short Circuit Power Dissipation**

The short circuit power dissipation occurs due to the short circuit current that are occurs when the higher voltage in the system gets path directly to the ground is called the short circuit power dissipation. It is expressed as:

$$P_{sc} = I_{mean} V_{dd} \quad (2.3)$$

$$I_{mean} = \frac{1}{T}\int_0^T I(t)dt \quad (2.4)$$

**Switching Power dissipation**

The charging and discharging of capacitance occurs losses the power is known as switching power dissipation.

Static power

The static power consumption can be given as-

$$P_{static} = V_{DD} * I_{static} \quad (2.5)$$

Where,

$t_{avg}$ = Average gate delay,

$t_{dr}$ = Rise time delay and

$t_{df}$ = fall time

## III. LEAKAGE IN SRAM

One of the most important characteristics of ideal CMOS technology is the fact that it doesn't exhibit any magnitude of static power dissipation in steady state. In practical situations though, degraded levels of voltage are fed to gate comprising of CMOS transistors and a subsequent flow of current can be seen from power supply to ground, which is often termed as static biasing current. In Fig. 3.1, depicts the situation in which an inverter is driven by a pass transistor. On analyzing the circuit, we reach to the result that voltage at node A is degraded ($V_{dd}$-$V_{th}$). The inverter input being high ($V_{dd}$-$V_{th}$), the output would be low. Since, the PMOS transistor is weakly ON which results in static biasing current from power supply to ground nodes. Thus static biasing current come into the picture due to the aforesaid conditions. Static currents which flow from $V_{dd}$ to ground, without degrading the inputs is known as leakage power.

With the advent of technology resulting in scaling, supply voltage must be reduced to address dynamic power and issues pertaining to reliability. This in turn needs scaling of the device threshold voltage (Vth) so that a reasonable gate over drive can be maintained. Reduction in Vth, results in the sub-threshold current to increase exponentially.

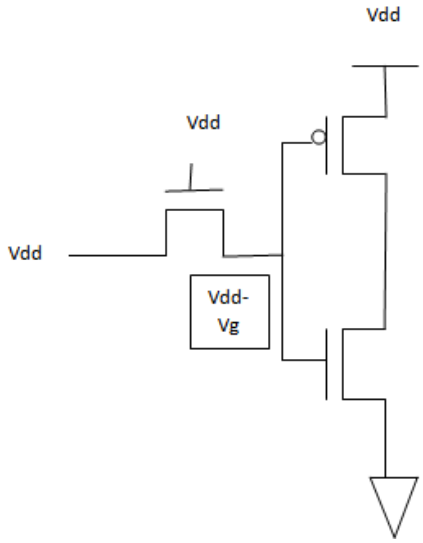


Figure 3.1 Degraded voltage level at the input node of a CMOS inverter results in static biasing power consumption

## IV. LITERATURE REVIEW

Investigation of leakage reduction techniques for a conventional 6T SRAM cell in advanced technologies. The most promising leakage reduction techniques that have been proposed are presented and compared for the 130-nm and 65-nm technology nodes. More specifically, the impact of the evolution of the gate tunneling and substrate currents is studied considering the efficiency of those techniques

King Tsu-Jae et al. described important considerations for the sleep transistor (often called MTCMOS) design and implementation including header and footer switch selection, sleep transistor, gate length and width etc. for area, leakage and efficiency and also investigated various power-on current rush control methods for the sleep transistor implementation in which he realized that the two storage charge method is most effective.

Lourts Deepak A. proposed that a Static Random Access Memory works as to plug two applications first cache memory which make communication between central processing unit and dynamic random access memory. Second is the driving force helps to provide the low power applications. SRAM does not require refresh current and it is portable as compared to DRAM.

Mizumura proposed that characteristics Vth and Ion of driver and load MOSFETs in which SRAM cells is investigated with a new developed SRAM cell array test structure which reported for the first time. The distribution of driver in SRAM cells and load MOSFET characteristics of Vth and Ion of SRAM cells gives report by using new developed SRAM cell array test structure. SRAM cells of

subthreshold humps monitored with algorithm gives occurrence automatically.

Tony Kim et al. said that nowadays CMOS based technologies scale down beyond 90nm or more deep towards submicron level. In this research work, MOSFET are facing the short channel effect problems that are common in integrated circuits as we move towards the submicron region. Parasitic resistance, capacitance are increases as we reduce the channel length.

The first order continuous turf MOSFET scrambling scheme created model proposed by Shayan Md. which assumed all critical parameters precisely at that level maintained the dignity of its position and significant role in the integrated circuits. The factor that helps to read the scaling effect is dimensionless factor denoted by the S.

$$s=\sqrt{2}$$

The forecast through the International Technology Roadmap for Semiconductors provides the details about the features size in nm vary from 2001 to 2016 is 130 to 22 nm respectively. At 45 nm technology the working is conducted right now and the supply voltage for that feature size is 0.6 to 1.0

Sushil Bhushan et al. presented a 4-T SRAM cell for less power and great compactness applications. The fresh cell size is 35.45% slighter than a standard 6-T cell employing identical design rules. In addition it utilizes one pair bit-line and two word-lines.

Sang Phill Parket al. showed MuGFET (Double-Gate (DG) transistors) appeared out as capable devices for Nano measure circuits as they have good scalability than bulk CMOS devices. Double Gate devices together with liberated gates (separate contacts to front and back gates) have lately been advanced.

Poonam et al. studied the Four-Transistor SRAM Cell in which various parameters like Power dissipation and propagation delay are analyzed in 45nm, 65nm and 90nm technology w.r.t supply voltage Vdd and Temperature. The tool used for simulation is TANNER EDA.

Razavipour et al. portrays two SRAM cells in which leakage currents shrinks the static power dissipation. The first cell had a NMOS pass transistors circuit, and the second circuit had PMOS as pass transistors. The total gate leakage of these circuits diminishes as compared to the conventional one.

Then Navakanta Bhatpresented a novel SRAM cell which is similar to behavior of Four-Transistor SRAM cell i.e. PMOS has two high load resistors and to regulate the short circuit current with NMOS switch. After simulating the circuit, the energy consumption becomes lesser as compared to traditional Static RAM cell.

## V. CONCLUSION

This paper embarks on a comprehensive quantitative survey towards the simulation of different leakages predominant. It can be concluded that the SRAM is a fundamental component of most digital systems. However, SRAMs suffer from leakage currents thereby reducing the batter retention and also the lifetime. Several leakage reduction mechanisms have been devised so far. The paper presents a survey on the different leakage reduction techniques along with their salient features.

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