Evaluation of n-bit Serial and Paprallel Linear Feedback Shift Register

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Abstract- Evolution of n-bit linear feedback shift register in very high scale integrated circuit hardware description language (VHDL) and evaluates its performance with respect to logic speed, number of slice and maximum frequency. Structural implementation of linear feedback reversible serial in serial out (SISO), serial in parallel out (SIPO), parallel in serial out (PISO) and parallel in parallel out (PIPO) in VHDL is configurable in terms of different parameter. The target device used for implementation of linear feedback shift register is Xilinx software with Spartan-3 device family. The output waveforms and timing report are also discussed.

Keywords—Serial in Serial Output (SISO), Serial in parallel out (SIPO), Parallel in Serial out (PISO), Parallel in Parallel out (PIPO), Maximum Frequency.

I. INTRODUCTION

A linear feedback shift register is a combination of series of flip flop and XOR or XNOR logic gates. Its output is pseudo randomly cycle through a sequence of binary values after certain number of clock cycle [1]. The repetition of random output depends on the number of stages in the LFSR. Therefore, it is an important component in communication system where, it play important role in various application such as cryptography application, CRC generator and checker circuit, gold code generator, for generation of pseudorandom sequence, for designing encoder and decoder in different communication channels to ensure network security, Design for Test (DFT) and Built in Self-Test design (BIST).

A linear feedback shift register is linear in the sense that its input bit is a linear function (XORing or XNORing) of LFSR previous state [2].

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation for VLSI circuits. The power dissipation during the test mode is 100% more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges. Linear feedback shift registers have multiple uses in digital systems design. Here we have implemented a 32 bit length sequence on FPGA using VHDL with maximum length feedback polynomial to understand the memory utilization and speed requirement. Also, we have presented the comparison of performance analysis based on synthesis and simulation result as well identify the simulation problem for long bit LFSR. The target device we have used Xilinx Spartan 3A and performed simulation and synthesis using Xilinx ISE. The HDLs are VHDL and Verilog. We prefer VHDL for programming because it is widely used.

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flops are driven by a common clock, and all are set or reset simultaneously. In these few lectures, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In – Serial Out, Parallel In - Parallel Out, and bidirectional shift registers. A special form of counter - the shift register counter, is also introduced.

II. DESIGN SYNTHESIS FLOW DIAGRAM

Synthesis is the process that reduces and optimizes the HDL or graphical design logic.

Some third-party synthesis tools are available as a part of the FPGA vendor’s complete development package. Simplicity’s Simplify and Mentor Graphics’ Leonardo Spectrum,Precision RTL and Precision Physical are some examples of third-party synthesis tools.

Xilinx offers ISE Project Foundation, which is a complete development application that includes a synthesis tool [3].

Although some FPGA vendors offer synthesis, they still recommend using a third-party’s synthesis tools. The synthesis tool must be set up prior to actually synthesizing the design. The synthesis process takes this information and the user-defined constraints and produces the output netlist. A constraints file specifies information like the critical signal paths and clock speeds. Synthesis can begin after completing set-up. General synthesis flow for tools involves three steps: creating structural element, optimizing, and mapping. Figure 1 shows a synthesis flow diagram.

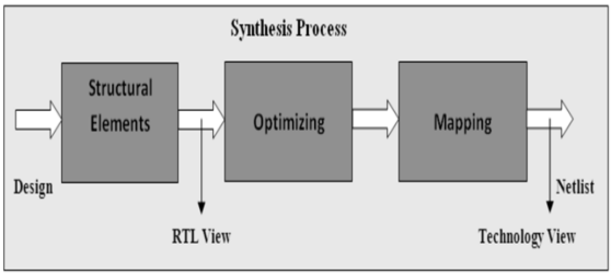

Figure 1: Design Synthesis Flow Diagram

The first step in the synthesis process takes the HDL design and compiles it into structural elements. The next step involves optimizing the design, making it smaller and faster by removing unnecessary logic and allowing signals to arrive at the inputs or output faster. The goal of the optimizing process is the make the design perform better without changing the circuit's functions. The final step in the synthesis process maps or associates the design to the vendor specific architecture [4]. The mapping process takes the design and maps or connects it using the architecture of the specific vendor. This means that the design connects to vendor specific components such as look-up tables and registers. The optimized netlist is the output of the synthesis process. This netlist may be produced in one of several formats. Edif is a general netlist format accepted by most implementation tools, while '.xnf' format is specific to Xilinx and is only recognized by Xilinx's implementation. In addition to the optimized netlist, many synthesis tools like Simplify will produce a netlist for gate-level simulation and other report files. Stimulus applied to this netlist instead of the original HDL design produces the functional-level simulation, which lets the designer verify that the synthesis process hasn't changed the design's functions.

III. PROPOSED METHODOLOGY

This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name Shift Register.A shift register basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches.Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required.

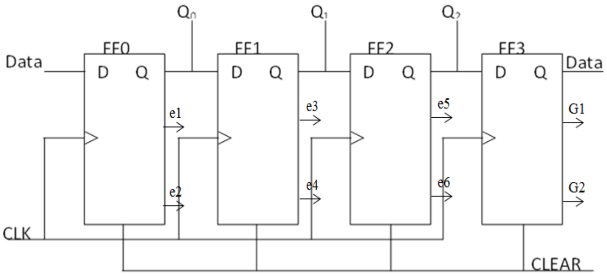

Figure 2: Flow Diagram of Serial in Parallel Output Shift Register

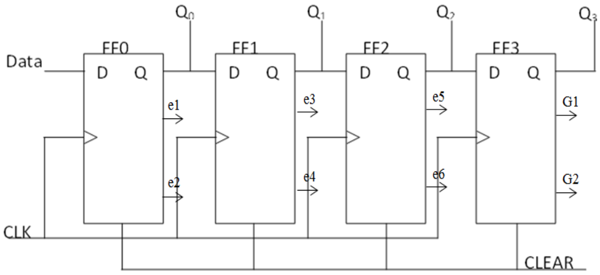

Figure 3: Flow Diagram of Parallel in Serial Output Shift Register

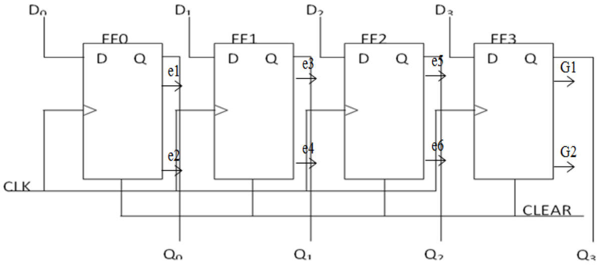

Figure 4: Flow Diagram of Parallel in Parallel Output Shift Register

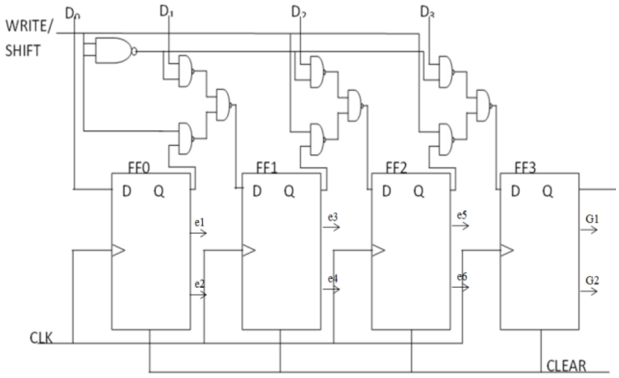

Figure 5: Block Diagram of Reversible Parallel in Serial out Shift Register

Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

IV. SIMULATION RESULT

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE^{TM} (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution. ISE 14.1i Xilinx tools permits greater flexibility for designs which leverage embedded processors. The ISE 14.1i Design suite is accompanied by the release of chip scope Pro^{TM} 14.1i debug and verification software. By the aid of that software we debug the program easily. Also included is the newest release of the chip scope Pro Serial IO Tool kit, providing simplified debugging of high-speed serial IO designs for Virtex-4 FX and Virtex-5 LXT and SXT FPGAs. With the help of this tool we can develop in the area of communication as well as in the area of signal processing and VLSI low power designing. To simplify multi rate DSP and DHT designs with a large number of clocks typically found in wireless and video applications, ISE 14.1i software features breakthrough advancements in place and route and clock algorithm offering up to a 15 percent performance advantage. Xilinx 14.1i Provides the low memory requirement while providing expanded support for Microsoft windows Vista, Microsoft Windows XP x64, and Red Hat Enterprise WS 5.0 32-bit operating systems.

Table 1: Device Utilization Summary of SISO Shift Register

Number of Bits	Number of Slice	Slice Flip Flop	Minimum Period	Minimum input arrival time before clock
Sparten-3				
4-bit	3	6	2.418 ns	3.774ns
8-bit	6	10	2.418 ns	3.892ns
16-bit	10	18	2.418 ns	4.152ns
Vertex-2				
4-bit	3	6	2.102 ns	2.815 ns
8-bit	6	10	2.102 ns	2.907 ns
16-bit	10	18	2.102 ns	3.045 ns
Vertex-2p				
4-bit	3	6	1.343 ns	2.394 ns
8-bit	6	10	1.343 ns	2.474 ns
16-bit	10	18	1.343 ns	2.594 ns

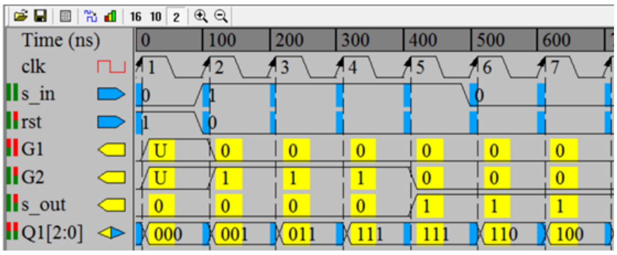

Figure6: Output Waveform of 4-bit Serial in Serial Out Shift Register

Table II: Device Utilization Summary of PISO Shift Register

Number of Bits	Number of Slice	Slice Flip Flop	Minimum Period	Minimum input arrival time before clock
Sparten-3				
4-bit	3	5	2.306 ns	3.744 ns
8-bit	5	10	2.306 ns	3.892 ns
16-bit	9	18	2.306 ns	4.152 ns
Vertex-2				
4-bit	3	5	1.608 ns	2.142 ns
8-bit	5	10	1.608 ns	2.227 ns
16-bit	9	18	1.608 ns	2.329 ns
Vertex-2p				
4-bit	3	5	1.333 ns	2.384 ns
8-bit	5	10	1.333 ns	2.474 ns
16-bit	9	18	1.333 ns	2.594 ns

The VHDL languages were used to design the VLSI architecture modules and are synthesized Spartan-3 (xc3s50-4pq208) device family. It is observed from the table 1 that the 2-bit SISO for number of slice 2, slice flip flop 3 and input output buffer 4, 4-bit SISO for number of slice 3, slice flip flop 5 and input output buffer 6, 8-bit SISO for number of slice 5, slice flip flop 9 and input output buffer 10, 16-bit SISO for number of slice 10, slice flip flop 17 and input output buffer 18 and 32-bit SISO for number of slice 19, slice flip flop 33 and input output buffer 34.

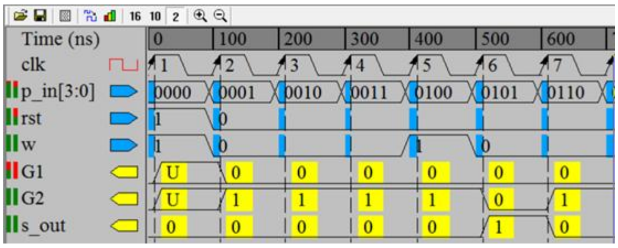

Figure 7: Output Waveform of 4-bit Parallel in Serial out Shift Register

The VHDL languages were used to design the VLSI architecture modules and are synthesized Spartan-3 (xc3s50-4pq208) device family. It is observed from the table III that the 2-bit PISO for number of slice 1, slice flip flop 2 and input output buffer 5, 4-bit PISO for number of slice 2, slice flip flop 4 and input output buffer 7, 8-bit PISO for number of slice 5, slice flip flop 9 and input output buffer 11, 16-bit PISO for number of slice 9, slice flip flop 17 and input output buffer 19 and 32-bit PISO for number of slice 18, slice flip flop 34 and input output buffer 35.

The VHDL languages were used to design the VLSI architecture modules and are synthesized Spartan-3 (xc3s50-4pq208) device family. It is observed from the table 2that the 2-bit SIPO for number of slice 2, slice flip flop 3 and input output buffer 4, 4-bit SIPO for number of slice 3, slice flip flop 5 and input output buffer 6, 8-bit SIPO for number of slice 5, slice flip flop 9 and input output buffer 10, 16-bit SIPO for number of slice 10, slice flip flop 17 and input output buffer 18 and 32-bit SIPO for number of slice 19, slice flip flop 33 and input output buffer 34.

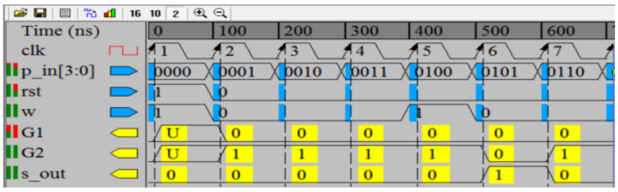

Figure 7: Output Waveform of 4-bit Serial in Parallel out Shift Register

The VHDL languages were used to design the VLSI architecture modules and are synthesized Spartan-3 (xc3s50-4pq208) device family. It is observed from the table IV that the 2-bit PISO for number of slice 1, slice flip flop 2 and input output buffer 5, 4-bit PIPO for number of slice 2, slice flip flop 4 and input output buffer 9, 8-bit PIPO for number of slice 5, slice flip flop 8 and input output buffer 17, 16-bit PIPO for number of slice 9, slice flip flop 16 and input output buffer 33 and 32-bit PIPO for number of slice 18, slice flip flop 32 and input output buffer 65.

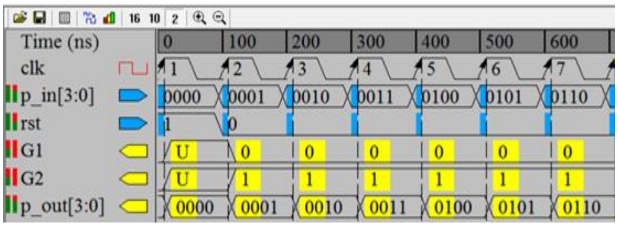

Figure 8: Output Waveform of 4-bit Parallel in Parallel Out Shift Register

V. CONCLUSION

In this paper, we have discussed the VHDL implementation of configurable linear feedback shift register by number of slice, number of flip flop, input output bounded, minimum period, arrival time before max input clock, arrival time after max input clock and maximum frequency. The proposed shift register is 37.5% improvement of number of slice, 30.67% improvement of slice flip flop, 14.61% improvement of arrival time before max input clock and 32.88% improvement of minimum period. Its means that the proposed linear feedback shift registers is high speed compared to previous design.

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