

Common-Mode Voltage Elimination For Z-Source H-Bridge Cascaded Multilevel Inverter with Induction Motor Drives

B. Dinesh¹, F. X. Edwin Deepak²

¹PG Scholar PSNACET, ²Assistant Professor, PSNACET

Abstract-A Z-source five-level inverter topology with common-mode voltage (CMV) elimination for induction motor drive is proposed in this paper. It has only one dc source and different voltage levels are generated by using this voltage source along with floating capacitors charged to asymmetrical voltage levels. This can eliminate the common mode voltage (CMV) in the current through the Z-source inductors as well as the voltage across the Z-source capacitors. For the system parameters, the proposed control technique produces better voltage boost across the Z-source capacitor, DC-link, and AC output voltage than the traditional PWM. The pulse width modulation (PWM) scheme employed in this topology balances the capacitor voltages at the required levels at any power factor and modulation index while eliminating the CMV. The inverter has good fault-tolerant capability as it can be operated in three or two-level mode with CMV elimination, in case of any fault in the H-bridges. Extensive simulation is done to validate the PWM technique for CMV elimination and balancing of the capacitor voltages. The experimental results demonstrate that the proposed topology can be considered for industrial drive applications.

Keywords: Common-Mode Voltage (CMV), Z-source Network, H-Bridge Five-level Inverter, Induction Motor Drive.

I. INTRODUCTION

Multilevel inverters are widely used in high power applications such as large induction motor drives. Multilevel inverter obtains the desired output voltage from several levels of input DC voltage sources. By increasing the number of input DC voltage sources, the inverter output voltage increases. The multilevel inverters have some advantages such as lower semiconductor voltage stress, improved harmonic performance, low Electro Magnetic Interference (EMI) and lower switching losses. Multilevel inverters output voltage is limited to the input DC sources voltage summation. It requires an intermediate DC -DC converter is for the buck or boost operation of MLI output voltage and also occurring of short circuit can destroy multilevel inverters.

In this paper multilevel inverter based Z-source is proposed which can solve above mentioned problems. The Z-source inverter utilizes impedance network between the DC source and the inverter circuit to achieve buck-boost operation. It employs shoot-through state control to boost the input dc voltage of inverter switches when both switches in the same phase. The Z-Source inverters have advantages such as lower cost, reliable, lower complexity and higher efficiency.

The ac output voltage can be of fixed or variable frequency. It can be achieved either by controlled turn-on and turn-off devices or by forced commutated thyristors depending on applications. The output voltage waveforms of an optimal inverter must be sinusoidal. The voltage waveforms of rational inverters are non-sinusoidal and contain certain harmonics. The output frequency of an inverter has been determined by the rate at which the semiconductor devices are switched on and off by the control circuit and can provide ac output of adjustable frequency. The dc input to the inverter might be a battery, fuel cell, solar cells and other dc sources.

A single phase cascaded H-bridge five levels Z-Source inverter is proposed for renewable energy systems and it employs Z network between the DC source and inverter circuitry to achieve boost operation. The output voltage inverter will be controlled using modulation index and shoot through state control.

Cascaded Z-Source performance parameters have been analyzed for cascaded Z-Source MLI. The performances of the these techniques are compared for single phase 5-level Z-Source cascaded multilevel inverter. The PWM scheme used effectively balances the capacitor voltages at the required levels, irrespective of power factor at any modulation index. A number of such schemes have been reported in the literature.

II. SYSTEM MODEL

Proposed Z Source Inverter Operation:

The basic Z-source inverter topology, which consists of inductors (L_1 and L_2) and capacitors (C_1 and C_2) connected in X shape to couple the inverter to the DC voltage source. The Z-source inverter can produce any desired AC output voltage regardless of the DC input voltage. Because of this special structure, the Z-source inverter has an additional switching state, the load terminals are shorted through both the upper and lower switching devices of any phase leg, which called the shoot-through (ST) state besides the eight traditional non-shoot through (NST) states.

The Z-source inverter has two operating modes: non shoot-through mode and shoot-through mode, as shown in Fig.3(a),3(b). During the shoot-through switching state, the diode is reverse biased. The input DC source is detached from the load and the two capacitors discharge energy to the inductors and to the load. During the non-shoot-through switching state the input diode turns ON and the DC input voltage source as well as the inductors transfer energy to the load and charge the capacitors, as a result the DC link voltage get boosted.

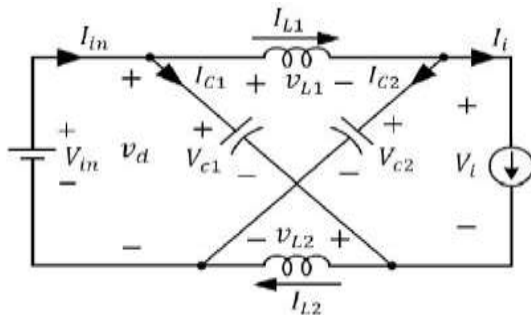


Fig.1 (a). Non-shoot-through state

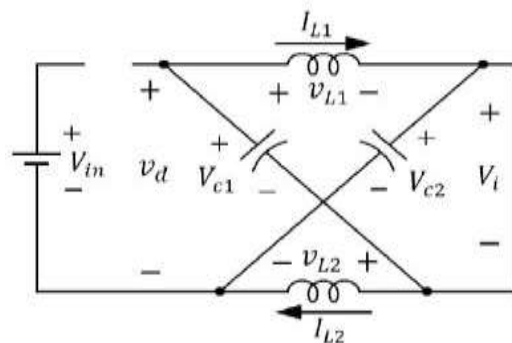


Fig.1 (b). Shoot-through state

Common Mode Voltage:

At the PWM inverter output, instantaneous summation of all the three phase voltages is non zero, an average voltage in a neutral point w.r.t ground create so called common mode voltage.

$$V_{CM} = \frac{(V_{A0} + V_{B0} + V_{C0})}{3} \quad (1)$$

In which V_{an} , V_{bn} and V_{cn} are the phase voltages generated by the PWM inverter. The common mode voltage is the access of amplitude equal to the DC bus voltage and the frequency equal to the inverter switching frequency. Pole voltages will be commonly delivered to all the capacitors C_1, C_2, C_3 respectively. Hence, a better solution is to eliminate the CMVs from the source itself. The proposed inverter structure facilitates elimination of the CMV, by selecting the inverter switching states that make the CMVs zero, for the generation of different voltage space vectors. The PWM scheme to eliminate CMVs is explained in the succeeding discussions.

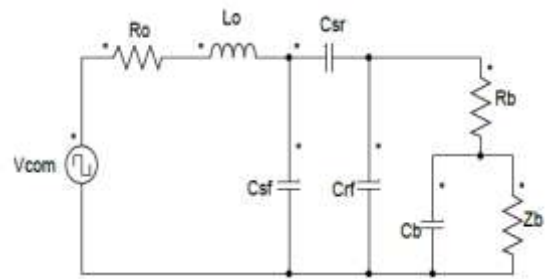


Fig. 2 Common mode equivalent circuit

Space Vector Pulse Width Modulation:

The SVM technique can be easily extended to all multilevel inverters. The Fig.5 shows space vectors for the proposed two, three and five-level inverters. These vector diagrams are common for all type of multilevel inverters. In other words, Fig.5(c) is valid for five-level cascaded inverter. The adjacent three vectors can arrange desired voltage vector by computing the duty cycle (T_j, T_{j+1} , and T_{j+2}) for each vector

$$V^* = \frac{(T_j V_j + T_{j+1} V_{j+1} + T_{j+2} V_{j+2})}{T} \quad (2)$$

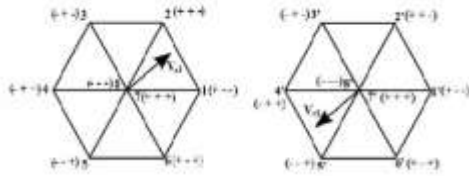


Fig.3. Individual space vector references

The proposed topology and the PWM technique for eliminating the CMVs and balancing of the capacitor voltages are validated by extensive simulation at different modulation indices and operating power factors. The same inverter is operated using normal SVPWM without common-mode elimination scheme also, for comparison. Fig.3 shows waveforms pertaining to the inverter operation without common-mode elimination scheme at a modulation index. Effective elimination of the CMV is evident from the bottom trace of this figure. Similar sets of waveforms for the operation of the inverter at a modulation index of 0.4, without and with implementation of the CMV elimination scheme respectively. A comparison of the waveforms of CMVs in these figures reveals the effectiveness of the proposed topology and the PWM technique in eliminating the CMVs as explained in the previous sections of the proposed topology. The space vector diagram is given above can arrange the switching states from various voltage levels. The arrangement of five-level inverter topology has been implemented and designed by the above references.

III. PREVIOUS WORK

The conventional system is designed with five-level inverter topology which facilitates the elimination of CMVs, by employing a capacitor voltage balancing (CVBPWM)-based switching scheme. It requires only one dc source, and capacitors charged to asymmetric voltages are used for creating a multilevel voltages profile in the output. The PWM scheme used effectively balances the capacitor voltages at the required levels. The design of the PWM generation is made using the capacitor voltage balancing which takes a complexity in triggering sequence.

IV. PROPOSED METHODOLOGY

Implementation of Proposed System:

The proposed system is designed with Z-source inverter can boost dc input voltage with no requirement of dc-dc boost converter or step up transformer, hence overcoming output voltage reduction of conventional voltage source inverter as well as lower its cost. It consists of 2 identical inductors and 2 identical capacitors which are composed to form a unique impedance network to avoid short circuit when the devices are in shoot-through mode, a diode is used to block reverse current, and a three phase bridge in conventional inverter. In three-phase Z-source inverter, one additional control parameter is used namely the Boost Factor (BF), which modifies the AC output voltage equation. The experimental results of the proposed topology is more efficient than the conventional topology.

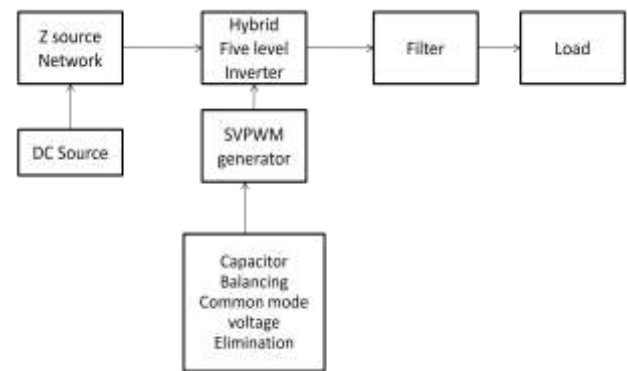


Fig.4. Proposed Block diagram of z-source H-bridge five-level inverter with CMV elimination

The power circuit diagram of the proposed hybrid five-level inverter topology is given in Fig.5. It has only one dc source (V_s) common to all the three phases and three capacitors per phase ($CA1, CA2, CA3; CB1, CB2, CB3; CC1, CC2, CC3$), which are charged to different voltage levels. The ratio of the dc voltage source to the different capacitor voltages in each phase is kept at $V_s: V_{CX1} : V_{CX2} : V_{CX3} = 8 : 4 : 2 : 1$, where $X = A, B$ or C . The presence of two H-bridges (HB-1 and HB-2) in each phase facilitates multiple ways of combining the capacitor voltages with the dc source voltage. By combining the dc bus voltage with the capacitor voltages, this configuration can generate 12 pole voltage levels in each phase with respect to the negative terminal of the dc source (O). They are 0, 1V, 2V, 3V, 4V, 5V, 6V, 7V, 8V, 9V, 10V, and 11V. Out of these, seven voltage levels (1V, 2V, 3V, 4V, 5V, 6V, and 7V) have redundancies in their methods of generation, which can be utilized for balancing the capacitor voltages at any instant, irrespective of

modulation index and operating power factor, as described later in this paper.

The voltage levels 0 and 8V do not affect the capacitor voltages. The last three levels (i.e., 9V, 10V, and 11V) do not have redundancies for balancing the voltages across the capacitors involved, at any instant. Hence, while using these voltage levels, the voltages across the capacitors involved will have to be balanced in an average sense in a cycle, which imposes limits on the operating power factor and the modulation index. For drive applications, it should be able to balance the capacitor voltages at any operating frequency (or operating voltages) under steady-state and transient conditions of sudden acceleration or load change. Hence, in this work, only the first nine voltage levels are used for realizing a multilevel inverter for drive

applications. Since the capacitors are bypassed while generating the voltage levels of 8V and 0V, their voltages are not affected.

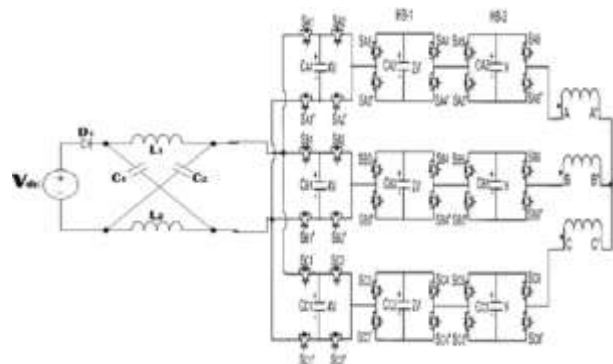


Fig .5.Proposed circuit diagram of z-source H-bridge five-level inverter with CMV elimination

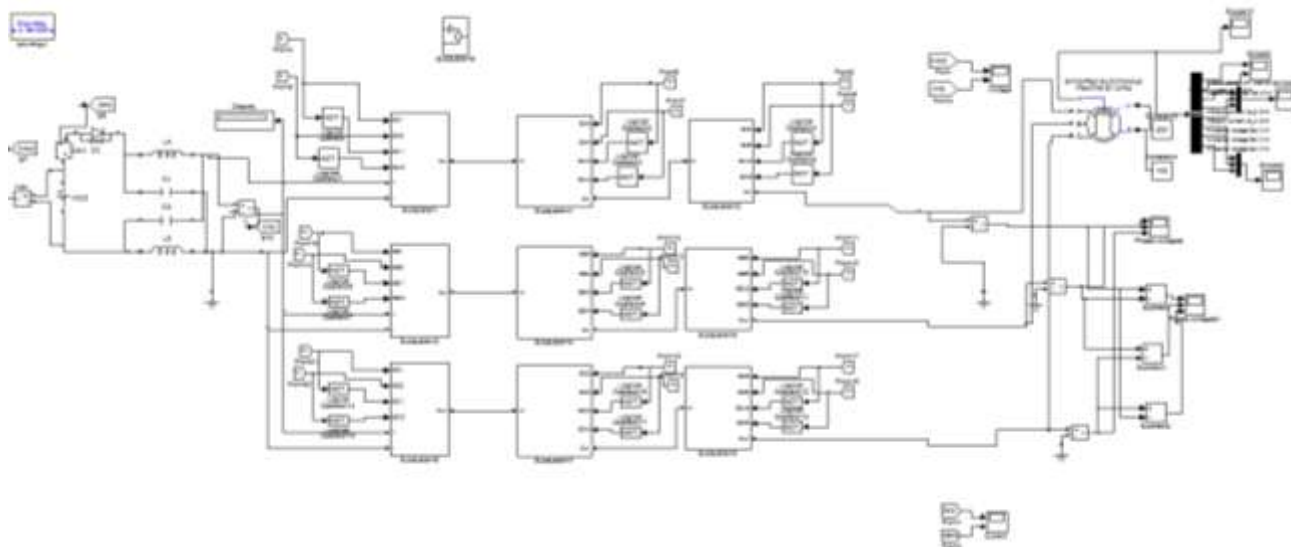


Fig.6. simulation diagram for proposed z-source five level inverter

The capacitor voltages are used for generating the remaining seven voltage levels, and their voltages are balanced by utilizing the redundancies that exists for realizing these voltage levels. For example, the voltage level 7V can be generated in four different ways. These four methods of generation of 7V and the charging or discharging effects on capacitors involved, for the marked direction of the current, are depicted in Fig.4. The effects on the capacitors will be opposite when the direction of the current reverses. It can be seen that's all the capacitors involved in the generation of this voltage. level can be charged or discharged in any direction of the load current by properly selecting the method of generation and the voltage across them can be kept balanced. Hence, the

capacitor voltages can be balanced irrespective of the power factor and modulation index and gives very efficient values in the output.

V. SIMULATION DIAGRAM AND RESULTS

The simulation diagram for proposed z-source five level inverter is shown in fig.6. The simulations are implemented with modulation index 0.8, input voltage of 100V, capacitor value is 2200 μ F and inductor value of 300mH. The z-source boosted voltage is 240V. The idea approached in this simulation is to perform common mode voltage elimination with help of SVPWM scheme that eliminates the common mode voltage and results zero

voltage at the end. It also performs capacitor voltage balancing by balancing the capacitors C1,C2,C3 which is connected across the voltage. The output current results are also performed in this below simulation by using PWM. In this simulation diagram an induction motor is connected for implementing its speed, torque, rotor angle, electrical power, motor voltage and current. The experimental verification of the proposed topology is carried out on an induction motor under transient and steady-state operating conditions. The performance of the inverter-fed drive is tested for different modulation indices covering an entire speed range, including the over modulation region. The experimental results confirm the potential of the proposed inverter topology to be considered for industrial drive applications.

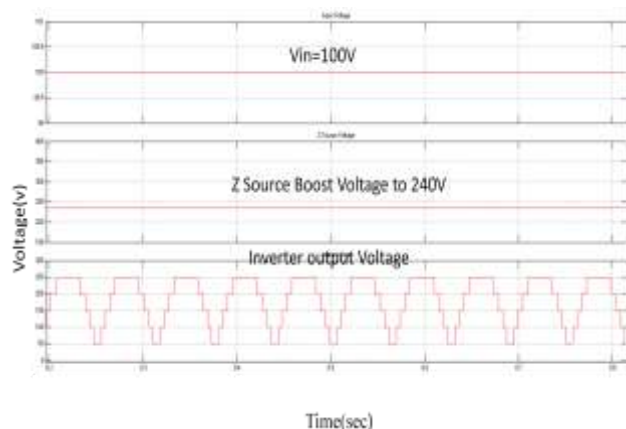


Fig 7: Input voltage, z-source boost voltage and inverter output voltage waveform with filter

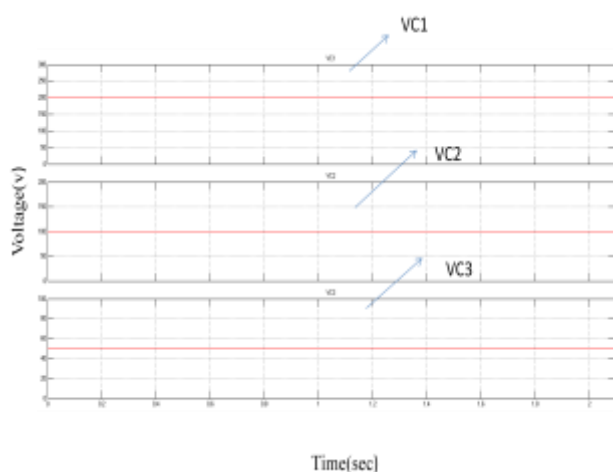


Fig 8: waveforms for Voltage across the capacitors C1,C2 and C3

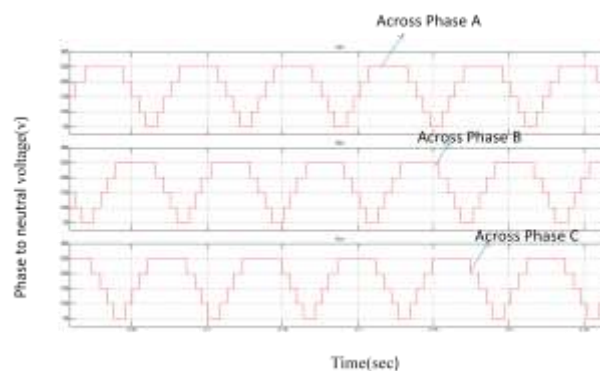


Fig 9 : Phase to neutral voltage waveform with elimination of CMV

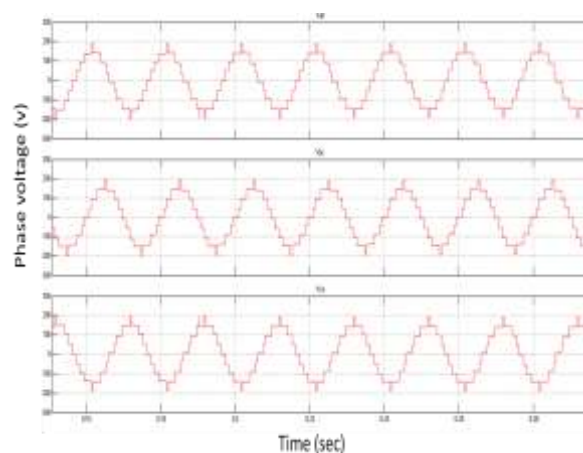


Fig 10 : phase to phase voltage waveform with elimination of CMV

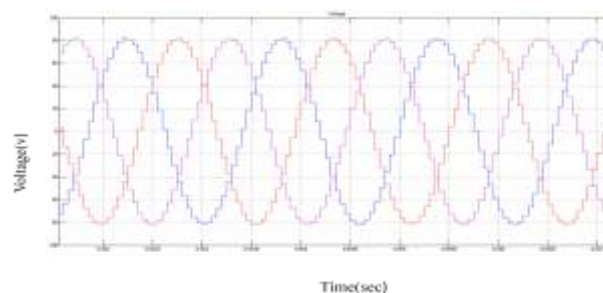


Fig 11 : Output voltage waveform for Induction motor with respect to Time

Advantages Of Z-Source Inverter Over Conventional Inverter:

- It has unique feature that it can boost the output voltage by introducing shoot through operation mode

- Z-source inverter is cheaper and simpler compared to traditional inverter
- Z –source inverter can increase inverter conversion efficiency by 1%
- Inverter motor conversion efficiency by 1 to 15% over conventional inverter
- It also reduces SDP by 15% which also leads to cost reduction
- The existing inverter suffer the shoot through reliability problem

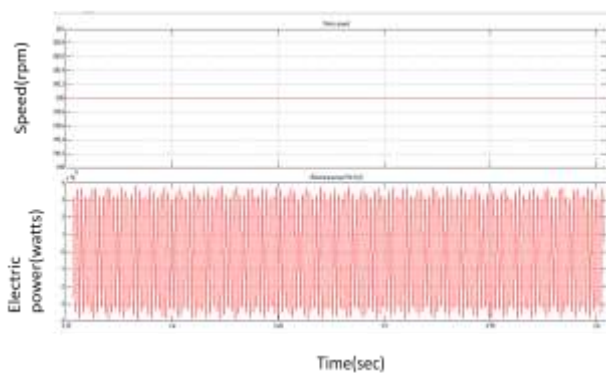


Fig 12 : waveforms for rotor speed and electrical power Vs Time

VI. CONCLUSION

In the project, the common mode voltage that occurred between the terminals was eliminated in five level Z-source cascaded multilevel inverter and using SVPWM, a pure 5 level sinusoidal wave was obtained. The Z-Source utilizes shoot-through state to boost the input dc voltage of inverter switches. The performances of the proposed SVPWM techniques have been evaluated using MATLAB.

From the results, it is found that SVPWM technique provides a higher RMS value of the output voltage and higher voltage gain. Topology and modulation-method is selected based upon the application. SVPWM technique have been implemented and tested in Induction motor drive in the hardware. The proposed Z source multilevel inverters can be connected to Z source inverter based DC/DC converters and its integration with suitable rectifier circuits and necessary modulation strategies is left to future investigations.

VII. FUTURE SCOPE

The Z-source inverter can boost–buck voltage minimizes component count, increase efficiency and reduce cost. The proposed paper will be implemented in hardware experiments by using induction motor drives and also can get some reliability and outputs like boosted voltage and higher efficiency by using Z-source network.

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