Comparative Study and Analysis of Various Full Adders

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Abstract—In this paper, we discuss the various logic style of the CMOS ADDER along with the functional representation to implement the required Boolean logic in circuit. With this we able to understand the different design factors which have direct impact on the speed of the circuits such as the length of transistor, delay in circuit path, capacitance. The two important and the diverging parameter of designing are power consumption and speed; therefore a better way to compute the performance of the circuit is the Power Product delay. Another important parameter of the circuit is its driving abilities to be taken into consideration due to its cascading structure in which the output of one circuit is feed as the input to another circuit. However, if required driving abilities are not obtained then this arises the need of additional buffer which in turn boost the power dissipation of the circuit.

Keywords - CMOS Transistors, Full Adder, driving abilities.

I. INTRODUCTION

With the increasing development of technology and the area of integrated circuit result in evaluating the novel method for designing the high performance circuit. In today's world the important factor taken into consideration for designing the IC is small area requirement, low power consumption, less propagation delay. The applicable area for the IC uses the arithmetic logic circuit for evaluations. In designing any arithmetic circuit the basic unit is the full adder or the binary adder circuit. Thus we understand that the binary addition is the basic arithmetic operation of any logic circuit such as microprocessors, digital signal processors (DSP) and application-specific integrated circuits (ASIC) etc. So a better performance of this circuit results in the better performance of overall circuit. The judging parameters for performance of any circuit are the low power consumption and high speed of operation. In this paper we discuss the optimal design of the full adder circuit for the small scale applications.

II. FUNDAMENTALS

In this section we illustrate the architecture of the full adder circuit. This circuit consists of 3 input lines, namely A,B, Cin and has 2 outputs as Sum (represent the addition of inputs A and B)and Cout.

The output of full adder can be represented as:

Sum = A xor B xorCin

Carry = AB + BCin + CinA.

There are several logic styles are in existence for designing the full adder circuits. There are different flaw and benefits present in different style. Primitive design of full adder used only single style for complete fabrication of circuit. An example of such design style is the CMOS static full adder [2]. These adders used the pull up and pull down transistors with the better power for driving abilities and complete swing output.

III. FULL ADDER TOPOLOGIES

This part deal with the adder family, some of the members of this family are as follows:

- Ripple Carry Adder
- Carry Save Adder
- Carry Look-Ahead Adder
- Carry Increment adder
- Carry Skip Adder
- Carry Bypass Adder
- Carry Select Adder

A. *Ripple Carry Adder (RCA)*

The ripple adder circuit is fabricated by connecting the full adder in a series combination. Each full adder is responsible for addition of respective bits of augends and addend. The carry generated from the previous stage is forwarded to the next stage input carry (cin). However, this simple design ripple carry adder can be used to add number of any bit length, but it is not convenient for performing the addition of larger bit length numbers. One major flaw of this circuit is

that the propagation delay of the circuit increases with the increase in bit length, because the stage of propagation forthe generated carry from the least significant bit to the most significant bit increases. This increase in time can be represented by equation 1 :

$$t = (n-1)t_c + t_s \qquad \text{Eq (1)}$$

in above expression ts represent the delay for evaluating the addition in last stage and tc represent the carry generation delay of circuit. This delay in ripple carry adder is directly proportional to the number of bits, thus with the increasing number of bits; increases the delay which decreases the performance of the circuit. The benefit of this adder is its low consumption of power and low development area of the circuit. The systematic representation of this circuit is shown in figure 1.

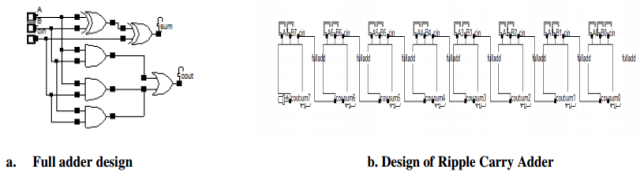


Figure 1 Schematic of RCA

B. *Carry Save Adder (CSaA)*

This circuit [11][12] decreases thenumbers of digit of the addition from 3 to 2. Thus the latency of the circuit is the 3 gate latency instead of depending on the number of the bits. The design architecture of this circuit consist of the n number of adder circuit each of which is responsible for evaluating the only addition of the corresponding bit of the three numbers and carry The final sum is obtained by performing the single position shift left operation of the carry sequence and placing a 0 to the MSB position of the obtained sum and add this evaluated sequence with the ripple carry adder to get n+1 bit number. All the input of the concerned stage is connected to full adder of that stage only without having any carry propagation connection in between them. All these different stages of adder are arranged in a binary tree structure and have logarithmic delay to the number of input, instead of depending on the number of bits of the input. The applicable area for these carry save adder is in high speed digital signal processing , multiplier structure and others .The also used in array multipliers to speed up its propagation of carry generation in array The systematic representation of the carry save adder is in the figure 2.

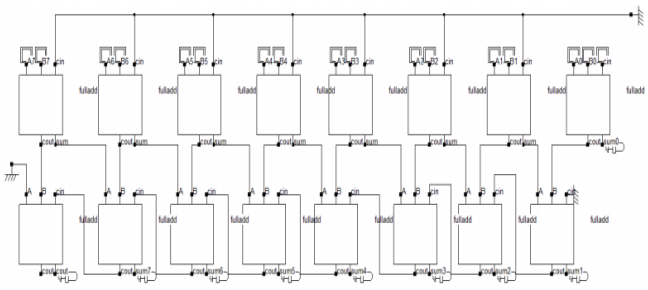


Figure 2 Schematic of CSA

C. *Carry Look-Ahead Adder*

This look-ahead carry adder is designed to decrease the delay introduced by the ripple effect of the carry generation. The delay which is present in the parallel adder, due to the propagation of generated carry is eliminated by this circuit. The working principle of this circuit is it compares the lower order bit of augends and addend if a carry is generated for higher order bits. This circuit decreases the delay introduced by carry propagation by decreasing the number of gate through which the carry propagate. These look-ahead carry adder first compare for each digit position that they are going to propagate the carry coming from the right, and by aggregate all these evaluated group to deduct rapidly whether that group are going to propagate the carry or not. By doing this the starts carry propagation slowly like in the ripple carry adder in each section of the 4 bit adder, but after this it flows 4 times faster lunge form one section of 4bit adder to the other section .At last the sections that receive the carry, have slowly propagation of carry among the digits of that group.

Thus look-ahead carry generator consists of three different phases as 1) NO carry generation 2) Carry propagation 3) carry generation, the below represent the functional representation of it.

$$G_i = A_i.Bi \qquad \text{for i=0, 1,2,3Eq (2)}$$

As similar to generation phase the propagation phase can be described as:

$$P_i = A_i \oplus Bi \qquad \text{for i=0,1,2,3 Eq (3)}$$

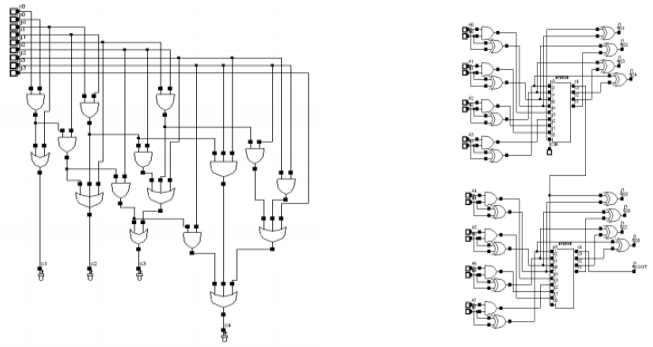
The carry generation at ith stage can be represent by the carry generation at (i-1) stage as shown in euation 4 Ci(out)

$$C_i(cout) = G_i + P_i\, C_{-1} \qquad \text{for i=0,1,2,3 Eq (4)}$$

The obtained sum equation can be represent as :

$S_i = A_i \oplus B_i Ci\text{-}1$ for i=0,1,2,3 Eq (5)

Figure 3 represent the 8 bit look-ahead carry generator by using the two section of the 4 bit carry generator in cascading configuration (Cout of one 4-bit adder section is feed as input to next 4 bit adder section).



(a) Look-Ahead Block (b) 8-bit Look-Ahead Adder

Figure 3 Schematic of CLA

D. Carry Increment Adder (CIA)

The fabrication of this uses two ripple carry adder circuit each of 4 bits. By using the first 4 bit ripple carry adder we add the first 4 bits of the desired number and generate the diversity of the partial sum and the partial carry. The output carry of the first ripple carry adder forwarded to the input carry of the conditional increment block. By this we directly generate the sum of the 4 bits of the number by using the ripple carry adder Theanother RCA circuit also generate the addition of the bits which are forwarded to the conditional increment block regardless of the output of the first RCA circuit. Since the input value of the first RCA circuit is low. The fabrication of this conditional incremental block uses the half adder circuit. As depending on the value of the output carry of the first RCA circuit the operation of conditional increment is defined. The presence of the half adder in the conditional increment block is responsible for the increment operation. Thus the addition output of the second RCA circuit is obtained through the conditional increment block. The systematic representation of carry increment adder is shown in figure 4.

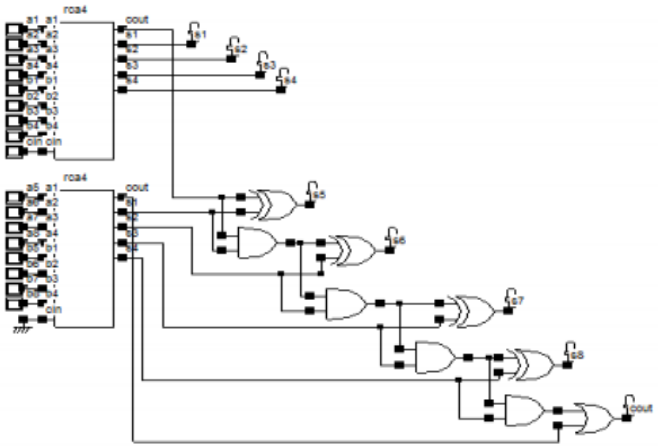


Figure 4 Schematic of Carry Increment Adder

D. *Carry Bypass Adder (CByA)*

In the ripple carry generation circuit each adder has to wait for the input carry before generating the output carry. This flaw can be removed by using an additional bypass adder circuit which speed up the operation of the addition. An input carry ci,0=1 will flows or propagate through all the adder circuit and generate the output carry c0,7=1 only when if all the propagation signal are 1. This exciting idea can be used to speed up the working of the adder circuit.Here we present the conditions which arise the need for propagation of the generated carry Case1: If(BP = P0P1P3P4P5P6P7P8 = 1)this case requires to suddenly forward the generated carry to the next phase by passing it to the additional bypass circuit and this situation don't arise then generate the carry by using the usual path. Case 2If (P0P1P3P4P5P6P7 = 1) then C0,7 = Ci,0 else removed or generate. Thus the architecture of the carry bypass circuit is divided into two phases, each phase bypass or skip the other phase with the help of multiplexer circuit if all the adder of that corresponding phase are propagate.

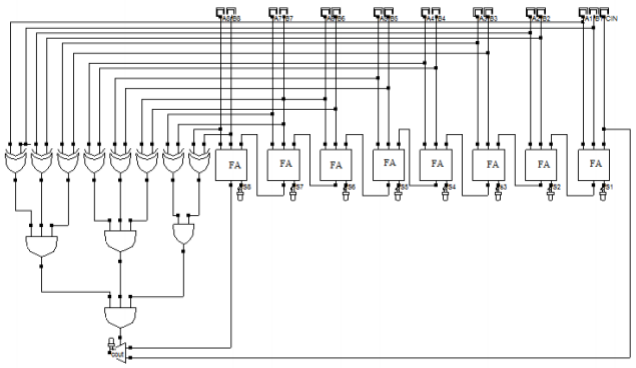


Figure 5 Schematic of Carry Bypass Adder

E. *Carry Select Adder (CSelA)*

The architecture of this circuit is divided into 2 parts and both individual part performing the addition in parallel one for the addition of carry in zero and other addition of carry in one .This CSelA consist of the ripple carry adder and a multiplexer circuit.This circuit even though consider simpler but have the faster speed of the operation.For evaluating the addition by carry select adder we use two ripple carry adder performing addition twice one with the assumption of the carry being zero and other with the assumption of carry being one.

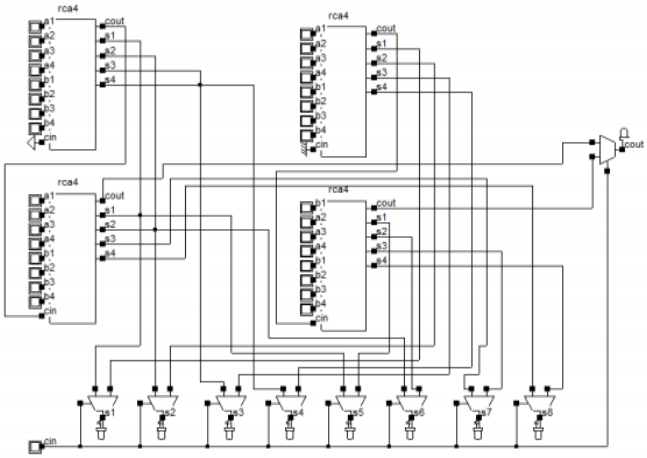


Figure 6 Schematic of Carry Select Adder

By calculating these two results the correct answer for sum and carry is obtained by using the multiplexer circuit only when the value of the correct carry is determined. The systematic representation of the CSA is represented from figure (6). The speed of operation of this circuit increases 30-90% as compared to the ripple carry adder by executing the addition operation in parallel and decreases the carry propagation routes.

IV. Review Of The Various State Of The Full Adder Circuits

In this we discuss the different logic style in order to increase the performance of the circuit and decrease the power consumption of it. This section discussed the eight different logic style of the full adder along with its advantage and disadvantage introduced by the proposed style [9]-[15].Thus the review of all style is presented below along with its systematic diagram representation.

The FA24T is shown in diagram 7(a) [9] and Bridge is shown in figure. 7(b)[10].Full adder circuit is based on CMOS style also called as the bridge style. FA24T consist of the 24 transistor and bridge implementation contains the 26 transistors.In implementation of the FA24T its bridge circuit is used to generate the output carry and other bridge circuit in series is used to obtain the value of sum, while in designing the bridge full adder both sum and carry are generated in parallel manner. The designing architecture of FA24T consists of two transistor less than the bridge full adder thus provide less consumption of power than bridge. But in the FA24T the sum signal has to wait for a period of time till the carry generated, thus its speed of operation is slow compared to the bridge full adder. These FA24T has better driving capabilities than the bridge adder as they consist of the inverter circuit at the output. The benefits which we are obtained from the bridge adder circuit because of its parallel design implementation are increase in performance, symmetric and the robust feature.

The Complementary Pass-transistor Logic (CPL)Full Adder is shown in figure7(c) [11] consists of 18 transistors of NMOS pass transistor logic. Because of this we have lower the value of the capacitance and higher speed of operation. But this also results in a single threshold voltage Vt deficit in the output. Due to this deficit of single threshold voltage in the output the CPL transistor consumed less power than the static CMOS transistor. At the low value of the voltage they decrease the noise margin and cause severe problem in cascading configuration.For this we utilize the CMOs inverter circuit to regain the loss of voltage value and guarantee drivability factor, and used the ineffective PMOS transistors in order to underrate the value of the static current which is present because of the incomplete turnoff the PMOS output inverter of .Because of this introduce overhead the performance of the circuit decreases..

The Double Pass-transistor Logic (DPL) Full is shown in figure7(d) [11] which can be considered as the upgraded version of the CPL transistor and consists of the 24 transistors. To get the complete swing operation by this circuit we introduce the PMOS and the NMOS transistor in parallel in DPL circuit. Because of this parallel configuration the problem of performance degradation and decreases in the noise margin at low voltage level is eliminated in the DPL circuits. But because of the presence of the PMOS batteries caused in increases the value of the input capacitance and decrease in the performance.

Hybrid (HFA)[12] and N-CELL1 (NC1FA)[13] Full Adders, is represented in figure:7(e) and Fig. 7(f) specifically, depends on the operation of low power value of XOR/XNOR circuit [16]. HFA consists of the 26 transistors and have an updating fabrication by utilizing the operation of the XOR/XNOR circuits. In this circuit the maximum latency introduce in the transition from the 01 to 00, which can be decreases by using the two series PMOS transistor and second case of this is when transition from 10 to 11 which also decreases by using two series NMOS transistor.This additional updation increases the speed of the operation of the XOR/XNOR circuit but simultaneously increases the power consumption of the circuit. To generate the sum the HFA uses the additional XOR circuit implemented by using the pass transistors. In this circuit the presence of the output inverters helps in regain the output voltage and improve the driving capabilities of the circuit. In HFA the coutgenerator has the complementary style of the CMOS logic and it has the advantage of using this complementary logic style. Its complete designing parameters are clear from the diagram representations [5].

The designing of the NCELL1 full adder uses the 14 transistor and the low power XOR/ XNOR. These circuits consists of the pass transistor to generate a non full swing sum signal and has the 4 transistor for complete swing of coutsignal, but not have the required driving capabilities. Even though this NCEll 1 has less number of transistors than the full adder cell but have a increased performance compared to the HFA.

Mod2f Full Adder circuit.is shown in diagram7(g) [14], consists of the 14 transistors, and by using the pass transistor based on DCVS they able to produce the complete swing of the XOR/XNOR signal. Thus, as discussed in [13], this is reason for the better performance and the gain in the speed of the circuit in comparison with the circuit present in[16]. To obtained the non complete swing signal of sum they uses the pass transistor arrangements and to generate the complete swing output signal they uses the transmission gate .However, because of the presence of the pass transistor arrangements these circuits will not have the better driving capabilities.

The last member from the family of the full adder is N-10T[15]. One of the major advantages of this family is that it decreases the number of the transistor which in turn decreases the area of the development and increase in the performance of the circuit. But the flaw of this circuit is the lack of presence of driving capabilities and incomplete swing node. Also the presence of the XNOR gate before the inverter and the output of the circuit result in a decreasing voltage level. This loss of voltage will result in various changes in the circuit such as the low noise margin, high problem of power leakage and various severe problems in cascading

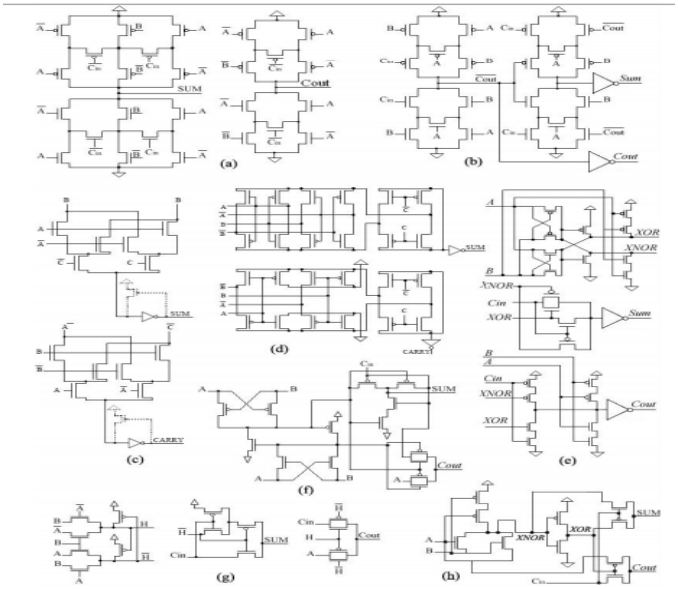


Figure 7. Eight state-of-the-art Full Adder Cells. (a) Bridge. (b) FA24T. (c) CPL. (d) DPL. (e) Hybrid. (f) N-Cell1. (g) Mod2f. (h) N-10T.

V. CONCLUSION

Thus, this paper presents the different logic style for adder circuit and different design factor to improve the performance.As you have seen that different design style has their own advantages and disadvantages of in terms of development area, power consumption, and propagation delay of circuit. And from the study we understand that by reducing these factors we have an increase in performance of the desired circuit.

REFERENCES

[1] G. Eason, B. Noble, and I.N. Sneddon, “On certain integrals of Lipschitz-Hankel type involving products of Bessel functions,” Phil. Trans. Roy. Soc. London, vol. A247, pp. 529-551, April 1955. (*references*)

[2] J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[3] I.S. Jacobs and C.P. Bean, “Fine particles, thin films and exchange anisotropy,” in Magnetism, vol. III, G.T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271-350.

[4] K. Elissa, “Title of paper if known,” unpublished.

[5] R. Nicole, "Title of paper with only first word capitalized," J. Name Stand. Abbrev., in press.

[6] Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, "Electron spectroscopy studies on magneto-optical media and plastic substrate interface," IEEE Transl. J. Magn. Japan, vol. 2, pp. 740-741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].

[7] M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

[8] R. Zimmermann and W. Fichtner, "Low- power logic styles: CMOS versus pass-transistor logic'', IEEE J. Solid- State Circuits, vol. 32, pp. 1079–90, July 1997.

[9] Keivan Navi, Omid Kavehei, MahnoushRuholamini, Amir Sahafi, Shima Mehrabi and NooshinDadkhahi, "Low-Power and High-Performance 1-BitCMOS Full Adder Cell" JOURNAL OF COMPUTERS,VOL. 3, NO. 2, FEBRUARY 2008.

[10] O. Kavehei, M. Rahimi Azghadi, K. Navi, A.P Mirbaha,"Design of Robust and High-Performance 1-bit CMOSFull Adder for Nanometer Design" , IEEE computerSociety Annual Symposium on VLSI, ISVLSI'08,Montpellier, France, April 2008, pp.10-15.

[11] Dimitrios Sourdis, Christian Piguet and Costas Goutis ,Designing CMOS Circuits for Low Power, EuropeanLow-Power Initiative for Electronic System DesignKluwer Academic Publishers, 2004, ISBN: 978-1-4020-7234-5.

[12] C. H. Chang, J. Gu and M. Zhang, "A review of0.18μm full adder performances for tree structuredarithmetic circuits", IEEE Transactions on Very LargeScale Integration (VLSI) Systems, vol. 13, no. 6, pp. 686-695, June 2005.

[13] Arash Shoarinejad Sue Ann Ung, and Wael Badawy,"Low Power Single Bit Full Adder Cells", Can. Jl. OfElectrical and Computer Engineering, vol. 28, no. 1, pp.3-9, Jan. 2003.

[14] S. Goel, Shilpa Gollamudi, Ashok Kumar and MagdyBayoumi, "On the Design of Low-Energy Hybrid CMOS1-Bit Full Adder Cells", 47th IEEE InternationalMidwest Symp. on Circuits and Systems, vol. 2, pp. 209- 211, 2004.

[15] Fartash Vasefi and Z. Abid, "Low Power N-bit Addersand Multiplier Using Lowest Number of Transistors 1-bit Adders", IEEE conference proceeding ofCCECE/CCGEI, Saskatoon, May 2005,pp.1731-1734.

[16] D. Radhakrishnan, "Low-voltage low-power CMOS fulladder", IEE Proceedings-Circuits, Devices and Systems,vol.148, pp. 19 -24, Feb. 2001.