FPGA Simulation of Bit-Count Comparator Based Modified Design of Viterbi Decoder for Burst Error Detection

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Abstract - In the wireless data communication the signals present in the transmission environment interfere with the communicating signals causing an undesired signal reception. This may further cause processing of wrong data. So the transmission error sensitive communication systems are always in need of an efficient encoder and decoder hardware interface that are capable of error detection and correction. Convolution encoder and decoder provide an easy to implement hardware in the same direction. The error handling efficiency of different convolution decoders vary with respect to their hardware designs and implemented algorithm for error detection and correction. Viterbi decoder provides one of the efficient techniques of error detection and correction to the communication systems. It is a Trellis code modulation decoder. There are various hardware implementations of viterbi decoder. A rate 1/3 decoder is a technique that encodes a single bit data in a 3-bit encoded data. This encoded data is decoded to effectively detect and correct single bit error with perfect efficiency. But the effects of burst error are not effectively judged using the technique because of the un-predictability of random effects of the burst error on the transmission data. In the proposed work a modified design of Viterbi decoder is simulated on a field programmable gate array device with the concept of burst error identification. In the proposed design, logical bit count comparator hardware is used to count the number of logic-'1' and logic-'0' and to transfer the information using a single-bit with the transmission data towards the receiver end. At the receiver, the same information is derived from the decoded data to authenticate the absence of the burst error with respect to the encoded data. A comparison of the conventional viterbi decoder simulation result and the proposed design is also presented in this work. The present work shows the simulation result with burst error identification using the proposed concept.

Keywords: Bit-comparator, Burst error, Convolutional Code, Error Correction, Error Detection, FPGA, Trellis Code Modulation, Viterbi Decoder, Viterbi Encoder, VHDL.

I. INTRODUCTION

A Viterbi decoder is based on Trellis Coded Modulation (TCM) Decoding technique. In this technique the data is decoded serially at symbol level. When all the symbols are decoded then the data with the best estimation to the actual data on the basis of hamming distance is traced as the received data. The encoder in a Viterbi design utilizes a convolutional hardware for transmission data generation. This data is transmitted on communication channel after channel modulation. In the present work the design simulations are performed using Xilinx Tool [1] on VHDL language platform. The error effects with a single-bit change in the transmission data are identified by the conventional circuit and are corrected by the implementation algorithm. The cases with the burst error are difficult to identify because of the random changes that are introduced in the data by the burst signal change. So, a pre-calculated bit is also added to the actual data during transmission. The value of this bit is decided on the basis of occurrence of logic-'0 and logic-'1' in the actual data that is to be transmitted.

The pre-calculated bit is again calculated at the receiver end and compared with the actual calculated bit. It the two bits are same then the estimated data at the receiver is accepted by the processing hardware for further processing. Otherwise, the received bits are ignored and the additional hardware of the system can acknowledge the transmitter to re-transmit the same data again. The present paper is organized as follows. Section-2 presents the functional overview of conventional Viterbi Encoder and Decoder using their general block diagram. Section-3 presents the proposed design concept using the block diagrams of the proposed encoder and decoder. Section-4 presents the functional simulation, hardware synthesis and dynamic power simulation results of the proposed designs and the conventional design. Section-5 presents the conclusion based on the proposed work.

II. CONVENTIONAL VITERBI ENCODER-DECODER MODEL

A convolutional Viterbi Encoder with rate p/q generates 'q' bits for 'p' bits of input. In an encoder with rate 1/3 a 3-bit encoded output is generated against each single bit of data

input. The input that is given to the convolutional encoder is a clock synchronized serial data. The realization of a viterbi encoder is performed using a convolutional encoder circuit. Each serial data bit causes a transition in the state of the encoder. Every state transition of the encoder generates a state output. A general block diagram representing the flow of data is shown in Fig-1

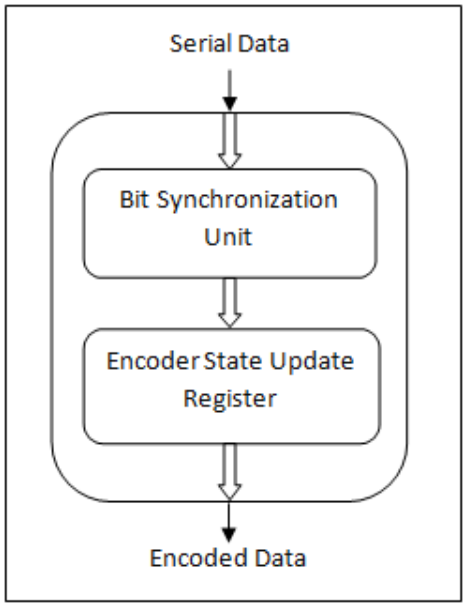

Fig. 1 General Block Diagram of Viterbi Encoder

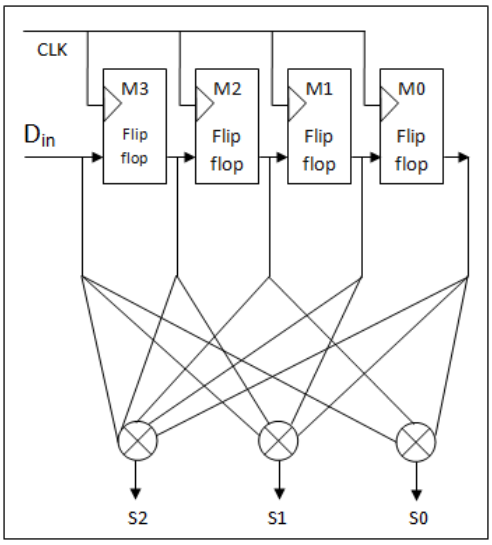

Fig. 2 Functional Diagram of Rate-1/3 Viterbi Decoder with 4-Memory Elements

A functional circuit of state update function of a rate 1/3 viterbi encoder with 4-memory elements is shown in Fig-2. In the state model there are 16-states that can be taken by the memory registers. The output equations of the encoder are realized using XOR logic gate and are represented as follows:

$S0 = D_{in}$ xor M2 xor M0 … (i)

$S1 = D_{in}$ xor M3 xor M1 xor M0 … (ii)

$S2 = D_{in}$ xor M3 xor M2 xor M1 xor M0 … (iii)

Where, D_{in} is the serial input data bit,

M0 M1, M2, M3 are the memory elements.

S0, S1, S2 are output bits.

The encoded data is transmitted towards the receiver for decoding and further processing. The Viterbi decodes the received bits using a serial synchronous hardware circuit. The received data is first arranged in the decoder register by identifying the start and end bits of the data frame and the received symbols. Each symbol is serially decoded. In a rate 1/3 decoder the symbol has 3-bits corresponding to each encoded data bit. These 3-bit information symbols are serially decoded using a clock synchronous logic circuit. A general block diagram of Viterbi Decoder is shown in Fig-2.

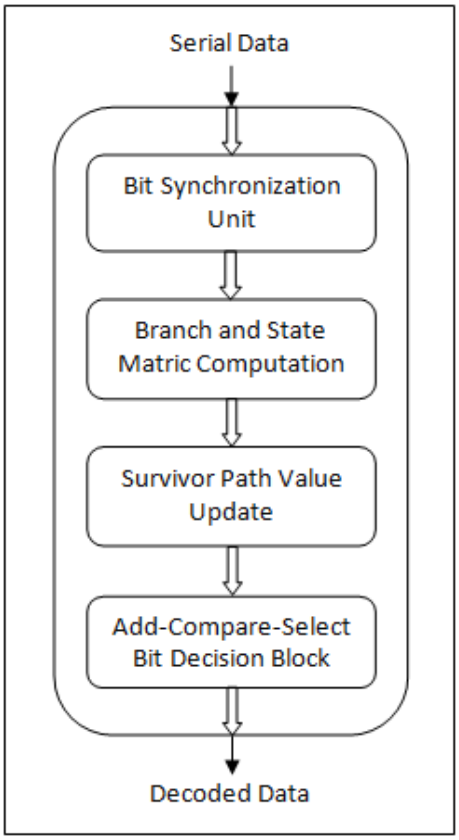

Fig. 3 General Block Diagram of Viterbi Decoder

In a trellis code modulation decoder Branch Metric and State Metric values are updated with every state transition, i.e., with every symbol decoding step. A "branch metric" is the Hamming distance between the actual transmitted symbol and the decoded symbol at the receiver. Branch metric accumulation along a path is called a "path metric". The value of path matric at a state of computation from the initial computation state is called a "state metric". At every state of serial process transition the estimated received symbol is stored in register. When the complete set of symbols is decoded the path metric of all possible data paths are compared for the least value of metric. The path with least metric value is selected as the data path. A trace back is followed to collect the estimated data

III. PREVIOUS WORK

Many modifications in the hardware designs are proposed in previous works. The conventional design implementation of Viterbi Encoder and Decoder is shown in [2] and [3]. A speed optimized field programmable gate array based design implementation is presented in [4] and [5]. A software decision based design for wireless network is shown in [6]. A FPGA base simulation of parity based burst error identification algorithm is proposed in [7]. A register-exchange based design of the Viterbi Decoder for high speed applications is shown in [8]. Low power implementations of Viterbi Decoder based on Adaptive search architectures are presented in [9], [10] and [11]. An implementation of M-algorithm based design of Viterbi Decoder is shown in [12]. Design of an error-resilient algorithm is shown in [13]. Many other designs are also proposed in previous works. In the present work a modified architecture of both encoder and decoder circuits is proposed for burst error identification using rate 1/3 decoder. The proposed designs perform the proposed functionality in addition to the conventional function.

IV. PROPOSED WORK

In this section author should discuss about related research has been done in the same domain or related domains with the name of the researcher and should be mentioned in the references. In a conventional viterbi encoder with rate 1/3 there are 3-bits generated against every single-bit of input data. In proposed work the same function is utilized to encode the data. But, prior to encode the data a fixed length data of 15-bit is considered for simulation of the proposed concept. The 15-bit data is given to a bit-counter block where the count of logic-'1' and logic-'0' is performed. In the next step, the count of logic-'0' and count of logic-'1' is compared. Since there are 15-bits in the actual data so one of the two count values, count of logic-'0' and count of logic-'1', is greater and the other one is smaller. The output of comparator block is logic-high if the count of logic-'1' is more than the count of logic-'0' else the output of comparator logic block is logic-low. The output of the comparator is concatenated with the actual input 15-bit data as MSB-bit. A total of 16-bit data is encoded using the conventional viterbi algorithm using a 4-memory element architecture hardware design. This generates 60-bit data for transmission.

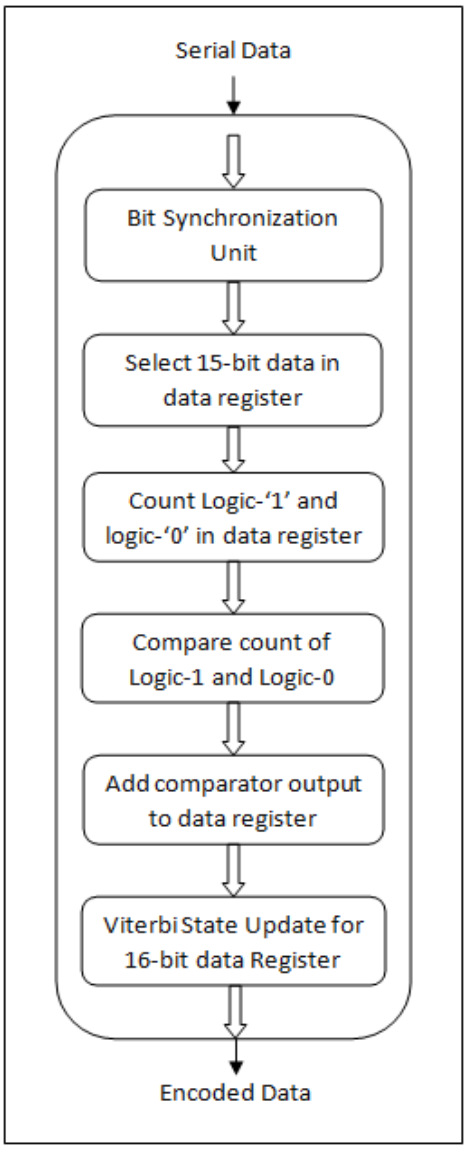

Fig. 4 Block Flow Diagram of Proposed Encoder

The decoder of the proposed design performs the initial decoding of the received data following the same trellis based algorithm.

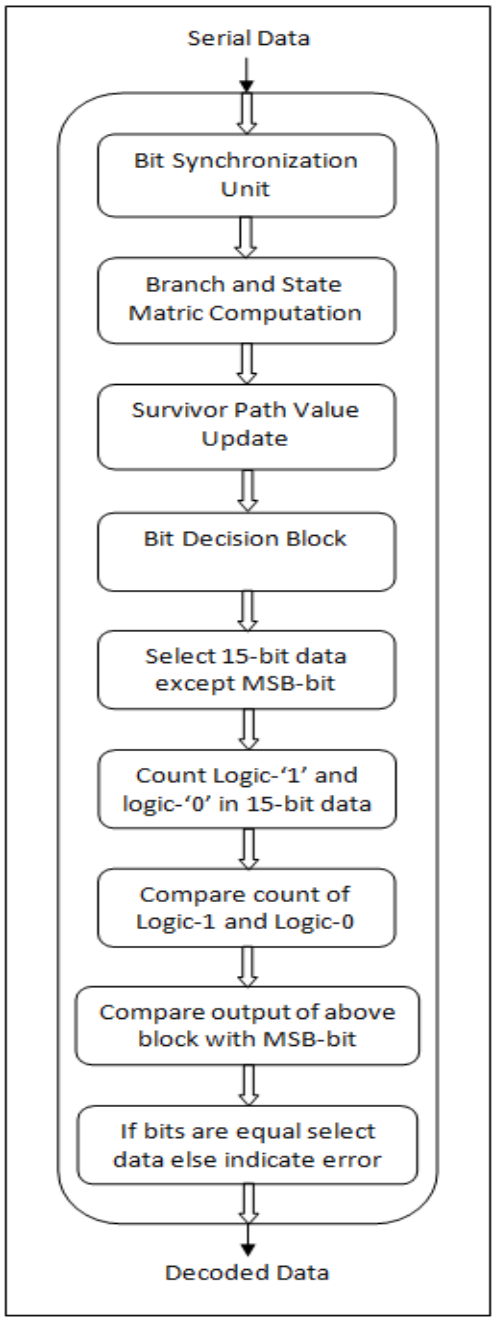

Fig. 5 Block Flow Diagram of Proposed Decoder

When the estimated 16-bit data is generated by the decoder from the received data the first 15-bits of the data are used to generate the count of logic-'0' and logic-'1' in these 15-bits. The 16th (MSB-bit) bit is carried as the first input to the logic bit comparator block. The count of logic-'0' and logic-'1' bits are compared in the count comparator block. The output of comparator block is logic-high if the count of logic-'1' is more than the count of logic-'0' else the output of comparator logic block is logic-low. The output bit of the comparator block is carried as the second input of the bit comparator block. If the two bits are equal in the above block then it indicates that the viterbi decoded data that is corrected by the intermittent hardware is the best estimated data.

V. Simulation/Experimental Results

The conventional and proposed designs of Viterbi Encoder and Viterbi Decoder are simulated using Xilinx ISim Tool and the design entry platform is Very High Speed IC Hardware Description Language (VHDL). The simulation is performed on various input vectors to verify the effectiveness of the proposed algorithm. The waveform result of the simulation of the proposed viterbi encoder is shown in Fig-6. The simulation input (binary) and the output (octal) vectors are 100111001010101 and 76205050216454615670 respectively. The waveform result of the simulation of the proposed viterbi decoder for the conditions: (i) without any error introduced in the input data, and (ii) with single-bit error detection and correction, are shown in Fig-7 and Fig-8 respectively. In these figures, each octal symbol represents the received 3-bit encoded symbol against each single bit encoded data. In these waveforms the decoder data input vectors (octal) are 76205050216454615670 and 76205050216454615670 respectively.

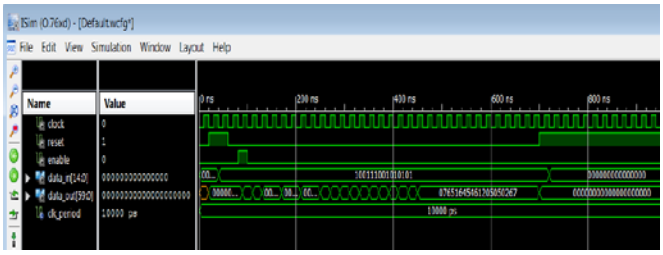

Fig. 6 Simulation Waveform of Proposed Viterbi Encoder

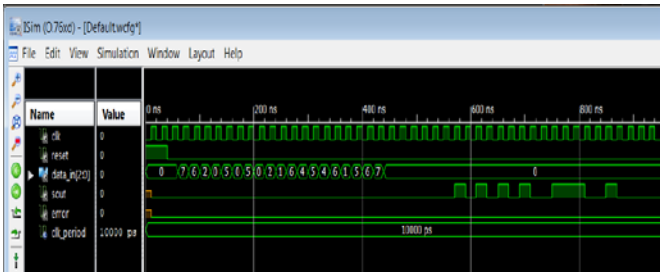

Fig. 7 Simulation Waveform Diagram of Proposed Viterbi Decoder without error

The waveform result of the simulation of the proposed viterbi decoder in Fig-9 and Fig-10 respectively represent the conditions: (i) with burst error effect in received appended bit after comparison of 1's and 0's (Fig-9), and (ii) with burst error effect in data bits (Fig-10). In these waveforms the decoder data input vectors (octal) are 76205050216454663317 and 76205050200000015670 respectively.

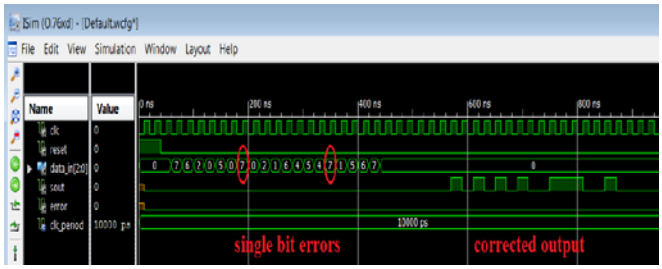

Fig. 8 Simulation Waveform Diagram of Proposed Decoder with error detection and correction

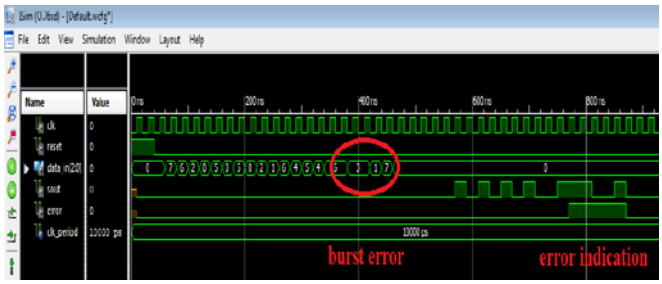

Fig. 9 Simulation Waveform Diagram of Error identification using Proposed Decoder with burst error effect in received appended bit after comparison of 1's and 0's

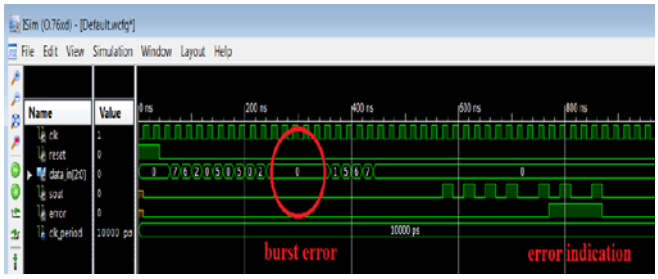

Fig. 10 Simulation Waveform Diagram of Error identification using Proposed Decoder with burst error effect in data bits

Xilinx Spartan 3E FPGA is used in the present work to perform software based hardware synthesis of the conventional and the proposed Viterbi Encoder-Decoder designs. The hardware utilization summary of the conventional and proposed designs is presented in Table-1 and Table-2 respectively.

TABLE 1. CONVENTIONAL DESIGN HARDWARE UTILIZATION

Hardware Resource	Total	Encoder		Decoder	
		Used	%	Used	%
Slices	4656	153	3	437	9
Flipflops	9312	120	1	362	3
LUTs	9312	202	2	623	6

TABLE 2. PROPOSED DESIGN HARDWARE UTILIZATION

Hardware Resource	Total	Encoder		Decoder	
		Used	%	Used	%
Slices	4656	149	3	510	10
Flipflops	9312	115	1	389	4
LUTs	9312	198	2	710	7

VI. CONCLUSION

The proposed work concludes a modified algorithm based on the conventional rate 1/3 Viterbi algorithm for error identification and correction. The present work implements a rate 1/3 Encoder and its corresponding Decoder Viterbi design using a comparator based on number of logic-'1 and logic-'0' bits in a binary data sequence of pre-defined length. In present work the length of sequence is 15-bit. If there is a change in the data during transmission that is affecting the transmitted data in a way that the more number of bit occurrences changes to less number of occurrence in the data frame then it can be identified using the proposed algorithm. But the present work has a limitation that those transmission effects that are changing the received data in a way that the count of the logic bit which was more in the transmitted data is more in received data also then such errors cannot be identified using the proposed work.

VII. FUTURE SCOPES

This opens a new field of research for work in order to improve this work and also to improve the burst error identification ability of the Viterbi rate 1/3 decoder from its conventional capability of identifying and correcting single-bit error. Since the hardware overhead using the proposed concept is very small with respect to the conventional hardware, this concept can be effectively implemented over large data in communication.

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