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DESIGN OF SERIAL ANALYZER FOR IoT DEVICES

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Abstract-One of the major challenges of today's embedded system design is that the debugging, which consumes most of the design point in time and as such there is a demand to reduce the debugging time. The proposed Serial Analyzer is designed to restore the traditional time -consuming debugging and provide a low cost and efficient means to debug the serial communication protocol like UART, I2C, SPI. This paper proposes the debug needs of IoT devices and systems. The proposed Serial Analyzer also acts as a tool that allows numerous serial data to be acquired simultaneously. To acquire different digital waveforms and data a Serial Analyzer is a multi-channel device. The major logic for Serial Analyzer lies on a FPGA board with a powerful embedded processor. A graphical user interface has been build to communicate with the Serial Analyzer. The firmware is built for the processor to interact with GUI and the RTL logic in FPGA. Serial Analyzer is designed and developed to debug, analyze and decode serial protocols in IoT systems.

Keywords: Internet of things (IoT), serial protocols, FPGA, serial analyzer, GUI.

I. INTRODUCTION

One of the major challenges of today's embedded system design is that the debugging, which consumes most of the design point in time and as such there is a demand to reduce the debugging time. The proposed Serial Analyzer is designed to restore the traditional time -consuming debugging and provide a low cost and efficient means to debug the serial communication protocol like UART, SPI, I2C.

The design of Serial Analyzer is use to debug serial communication protocols like UART, SPI, I2C. This tool will assist out designers with debugging their complex embedded systems. The Serial Analyzer comes with 16 channels, multiple trigger options and a easy to use front end GUI. It has the ability to both analyze and decode popular serial protocols.

II. HARDWARE DEVELOPMENT

Serial Analyzer Hardware architecture consists of many blocks as shown in the Figure 2. The Figure shows the major block which are discussed in next sections in details.

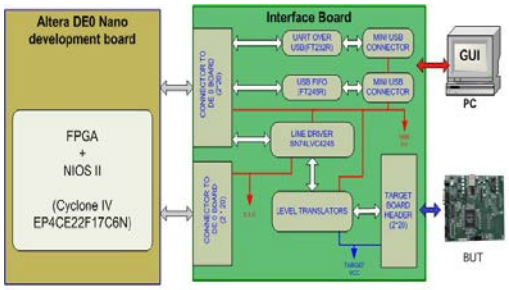

Figure 1. Hardware Architecture

The hardware design of Serial Analyzeris explained into four sub modules as follows

- Processing Module
- USB Module
- Buffer Module
- Power Supply Module

Processing Module: All the logic for Serial Analyzeris centered on Cyclone IV FPGA series from Altera. The crucial part of logic processing takes place in FPGA.The part number for the same is EP4CE22F17C6N.

USB Module: The USB section consists of USB parallel FIFO IC and USB UART IC.

Buffer Module: This section enables the user to connect target boards of different voltage levels (1.2V to 5V).FPGA will be working with 3.3V ,but the target board can work anywhere with in the range of 1.2V to 5V.So there is a need for level translation and buffer for protection and compatibility.

Power Supply Module: The power to hardware unit comes from USB port and target board.

A] SERIAL ANALYZER SCHEMATICS

Capture CIS is an EDA (Electronic Design Automation) tool. It is frequently used to create a schematic design for **PCB (Printed Circuit Board) and FPGA project**. The simple steps involved in schematic design include placing and connecting part, running Design Rules Check, and generating netlist. The tool is also capable of functional and timing simulations for FPGA project, board level simulation for PCB project and analog/mixed signal simulation using PSpice.

Open Capture CIS

From Windows Start Menu, select **Program - Cadence PSD 15.0 – Capture CIS**. You will see Studio Suite Selection dialog box choose PCB Design Studio with Capture CIS.

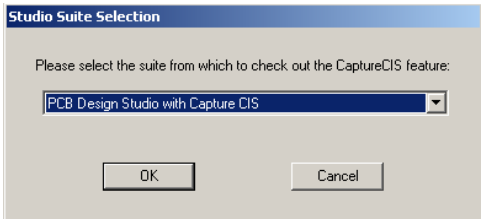

Figure 1. Studio Suite Selection Dialog

Create a new project by going to File > New > Project. Enter project name, select **schematic** project type and enter location you want the project to be saved as shown in figure 4.

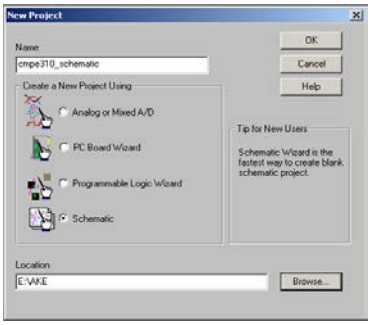

Figure 4. New Project Dialog

Capture CIS will create new schematic for PCB project and you will see your project workspace as shown in figure 5.

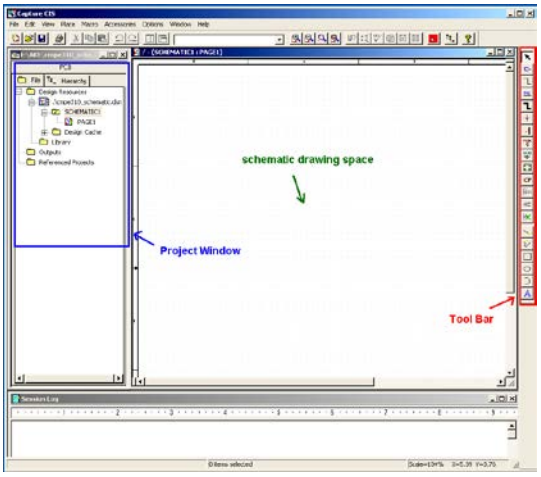

Figure 5. Schematic Project Workspace

Placing Part-You can place the circuit components of your board by click on CIS main menu; **Place - Part** (make sure the schematic window is the active window). Figure 5 shows the Place Part Dialog Box; you can search for a part through libraries by typing on Part textbox. You can select one particular library to be listed/searched or select multiple libraries at a time. Some part has multiple packages on the same chip (ex. 74LS10 has 3 packages of 3-input NAND gate), Capture CIS will automatically place all packages on the same chip before place a new chip (ex. you will see the instance of part as U1A, U1B for the package A and B of instance U1). Highlight the part you want to place on schematic and click OK. Click on the schematic work space to place the part, you can place same part multiple times, press ESC to end the command. Figure 6 shows the example of placing parts on the schematic.

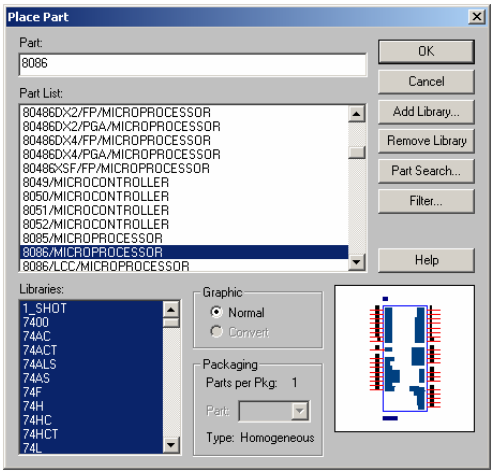

Figure 6 Place Part Dialog

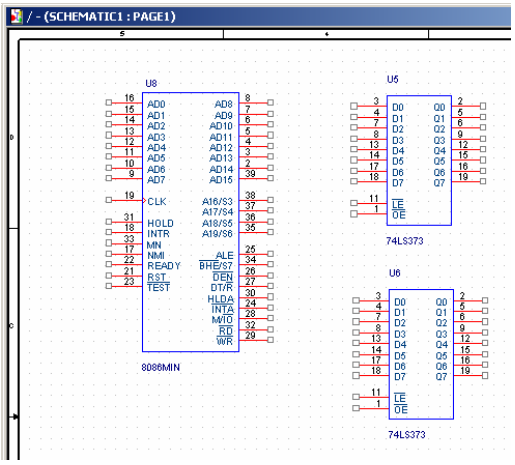

Figure 7. Place part example

Placing Power Source-To place power source on the schematic, simply go to **Place - Power** on the main menu. Select **CAPSYM** library and then use either **VCC or GND** for your power sources as shown in Figure 8. Click OK and then click on the schematic to place power source.

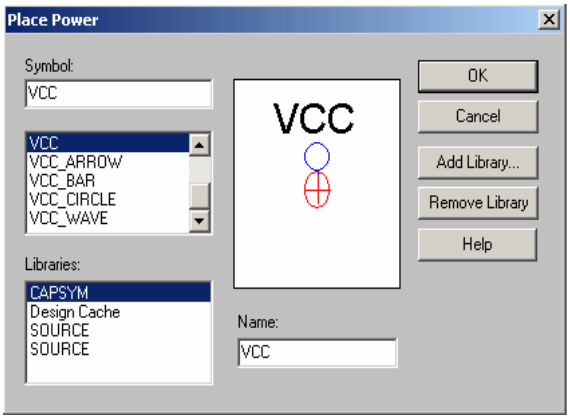

Figure 8. Place Power Source

On-Page Connection: Connect parts on the same page

Place Wire: The easiest way to connect part is to use a wire. Go to **Place - Wire** and then click once on the starting point of the connection. Move the mouse to the destination point (you might need to click along the way to make a 90 degree turn). Make sure you do not cross the wire to existing connections; Capture CIS will give you a warning (**red dot with sign**) whenever 2 nets are about to be connected. Double click to end the wire.

Off-Page Connection: Connect parts between pages- Capture CIS provides an off-page connector for this task. To create off-page connector, go to **Place - Off-Page Connector** on the main menu. Use either **OFFPAGELEFT-L or OFFPAGELEFT-R** from **CAPSYM** library, change a name of connector to the name you like as shown in Figure 9. You can place off-page connectors anywhere on the schematic and then connect a net to the off-page connector.

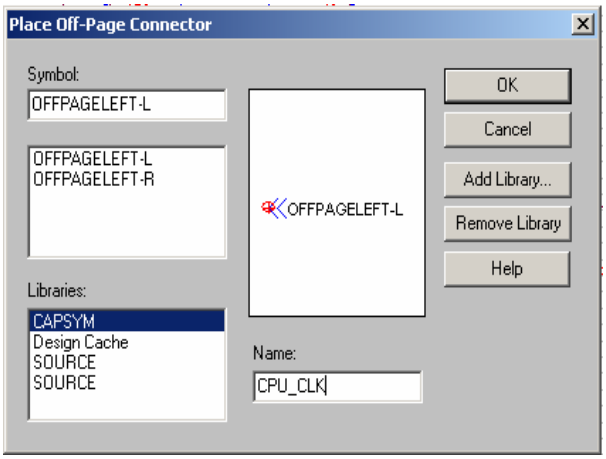

Figure 9. Place Off-Page Connector

No Connection

Capture CIS will complain if there are input pins of the part with no connection when you run Design Rules Check (does not complain for output pins). It is a **good practice to mark these no connection pins** including outputs so that you do not forget to connect some important pins on your design.

To place a no connect mark, go to **Place - No Connect** and then click on the pin that has no connection.

Design Rules Check (DRC)-Running **DRC** help verify your design by checking for open connection, floating off-page connector and so on. However, it is not a magical tool. It does not know if you make a wrong connection on your design such as connect the wrong bus to the wrong pin or connect VDD supply to GND pin.

To run DRC, click on schematic folder on the project window and then go to **Tool-Design Rules Check**. Check on "**View Output**" option on the bottom of the dialog to see the report after DRC run (Figure 10). You can modify other options but for most of the time, default options work very well. Now, click OK button, sit and relax. Take a look at the DRC report and fix errors if there are any.

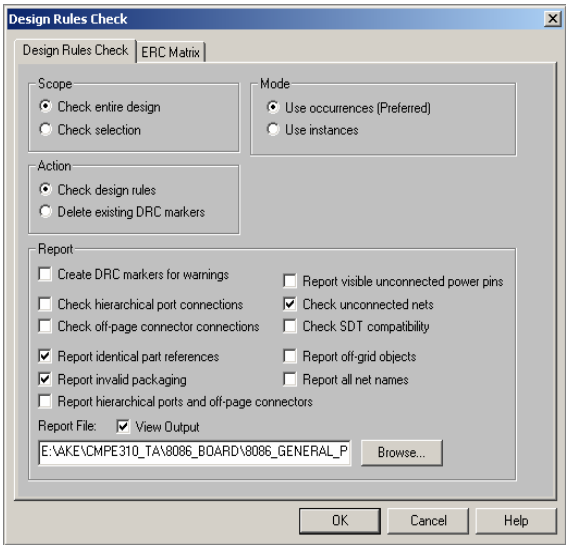

Figure 10. Design Rules Check

Creating Netlist-To import your design into PCB design tool, you will need to generate a netlist of your design. First, click on the schematic folder on the project window and go to **Tool - Create Netlist**. You will see the Create Netlist dialog box as shown in Figure 11. Click on "Layout" tab and then type the location and file name to be saved on Netlist File textbox, use "**.MNL**" extension for your output file. Click OK and you will get a **netlist that is compatible with Cadence Layout Plus**, a PCB design tool.

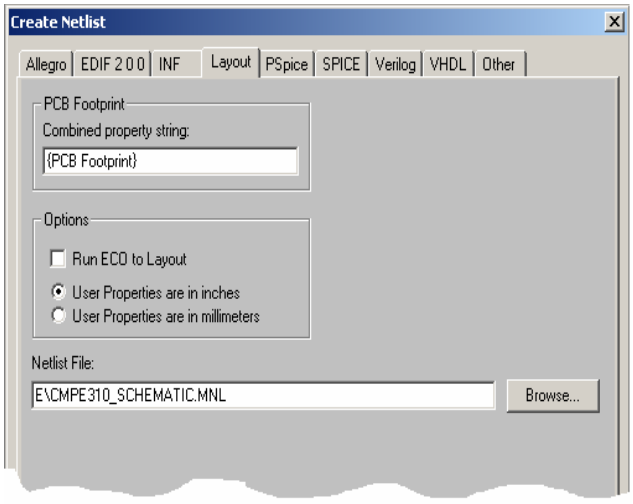

Figure11. Create Netlist

III. CONCLUSION

The design and Implementation of Serial Analyzer is a diverse project which would aid most of the designers to reduce the debugging time and cost .The RTL logic for the Serial Analyzer is based on a FPGA centered around a powerful NIOS II processor. Therefore the project can be extended to include all popular serial protocols like USB, CAN and so on.

Serial Analyzer has been studied to find its potential and necessary trade -offs when used as a logic analyzer. Within the goals of having a complete system based on FPGA to do logic analysis and serial debugging, the entire project has been developed with utmost optimization for speed, memory, RTL logic, power and size.

Apart from additional functionalities when compared to a typical logic analyzer, the Serial Analyzer offers multi trigger options, accurate sampling , user friendly GUI , decoding of serial data line based on protocol and debugging of serial data line .

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