To Improve the Rise Time, Fall Time for Dynamic CMOS Logic with Stack Techniques

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Abstract-There are several techniques that reduce the rise time and fall time. In this dissertation we can use stack techniques that can improve switching response. When we are reducing dynamic CMOS noise then it improves the switching speed of dynamic logic circuit. That means improvement of switching speed is also dependent on the reduction of dynamic logic CMOS noise. Since noise is basically result of charge leakage and charge sharing problem. That means if we can reduced the charge leakage and charge sharing problem then it can reduced the noise of dynamic logic CMOS circuit and it also improves the switching speed of dynamic logic CMOS circuit. Stack transistors has proven to be exceedingly most effective in reducing and minimizing sub threshold leakage or charge leakage in stand by mode of operation of circuit. It has been observed that this technique of using stack transistors saves around 33% in total leakage in 50nm devices.

Keywords: Micro wind 3.0.

I. INTRODUCTION

The switching speed of a CMOS gate is dependent on the time taken to charge and discharge the load capacitance. When we are give input transition either 0 or1 then results in an output transition it give either charges (CL) toward VDD or discharges(CL) toward VSS. Now, we need to define some terms such as Rise, Fall and Delay time

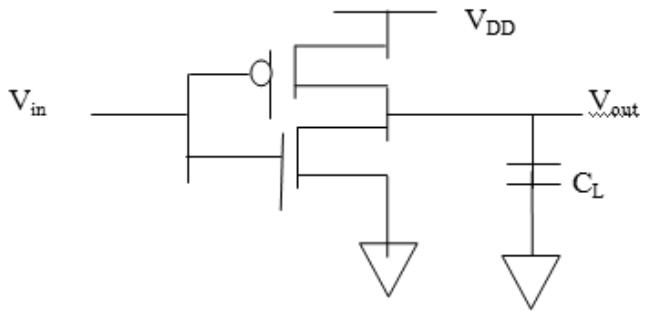

Figure CMOS inverter

For the calculation of rise, fall and delay time of the any CMOC logic circuit we are using computer simulation as well as analytical techniques. Whenever we are using more complex CMOS logic circuit then we are considering appropriate transistor model for the simulation of Dynamic CMOS logic circuits.

- Switching speed: Time taken by wave form to reach charge and discharge of load capacitance ($C_{L)}$.
- Rise time t_r : Time taken by wave form to reach from 10% to 90% of its steady state value.
- Fall time t_f : Time taken by wave form to reach from 90% to 10% of steady state value.
- Delay time t_d : time difference between input transition (50%) and 50% output level.

II. PROBLEM'S ANALYZED

In this paper there are certain issues of process variations, timing, noise tolerance, and power which are looked into together for operation optimization [2]. We recommend stack technique to improve following aspects:-

- To improve charge sharing, charge leakage problem in dynamic CMOS circuits.
- Optimize dynamic CMOS circuits with stack technique to enable and improve the rise time, fall time, when we equate them to their initial performances.

III. PREVIOUS WORK

In this section we discussed the previous approaches which are nearly related to our research. Here we analyse previous technique that primarily target for reducing rise time and fall time. These techniques are shown in below. The approaches that are adopted in VLSI design. Hear we are using base case, raising source voltage using keepers, source voltage using NMOS, source voltage using PMOS, Feedback Keeper and Pre-charge internal nodes.

Source voltage using PMOS :-

An influential way for rectified noise tolerance against both internal and external noises is to increase the source voltage of the transistors in the pull-down network. As the gate voltage has to be greater than the addition of the source voltage and the transistor threshold voltage when a transistor is turned ON, higher voltage source directly initiate's to gate turn on voltage. Besides, due to the body effect, transistor threshold voltage is increased when the source voltage rises up. This also aid's to improve gate turn-on voltage.

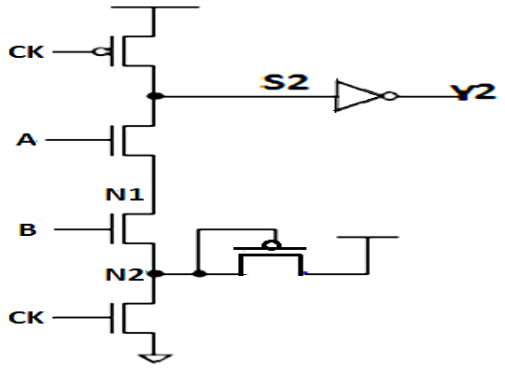

Fig. of source voltage using PMOS

Layout of source voltage using PMOS:-

Firstly, we can draw inverter in DSCH screen. For this we can used 2-PMOS, 3-NMOS, 1-Supply, 1-Ground, 1-Butten, 1-LED, 1-NOT gate and connecting wire that can used to give proper connection . Through this we can design source voltage using PMOS. After the completion of design it save in .MSK format.

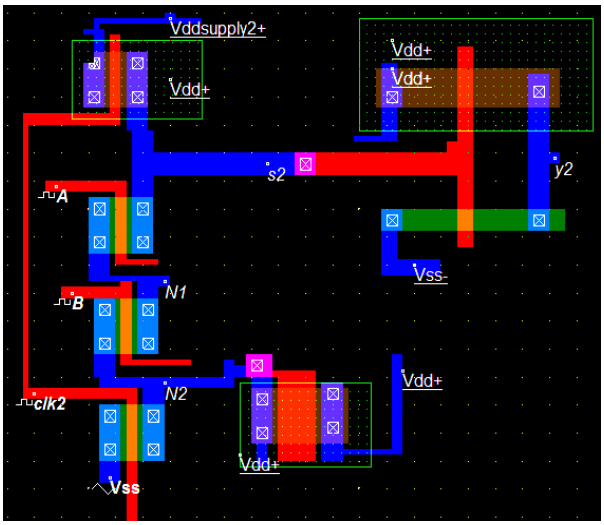

Fig Layout of source voltage using PMOS

Now, we are open Micro wind screen and open saved file. It can generate Lay-out of design circuit, after simulation it can plot graph between:-

- Layout.
- Voltage Vs Time graph.
- Voltage Vs Current graph.
- Frequency and Time graph.

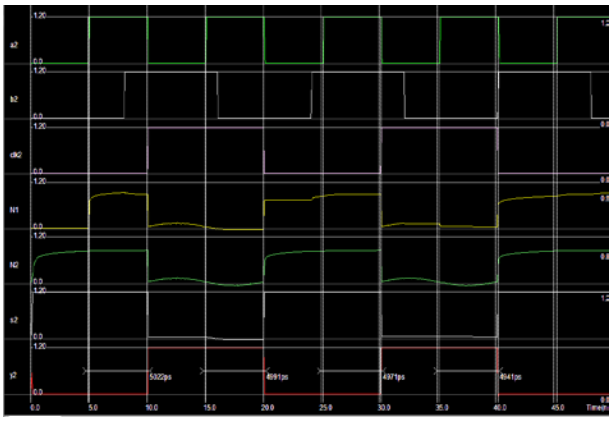

Fig Simulation of source voltage using PMOS

Parametric analysis of source voltage using PMOS:-

Through this table we can give the value of rise time, fall time and output current for source voltage using PMOS. This table also shows that the stack technique improves the Rise time, fall time.

Parametric analysis table:

Parametric analysis table of source voltage using PMOS		
Parameter	Rise time	Fall Time
Value	0.0342	0.0342

Source voltage using NMOS:

An influential way for rectified noise tolerance against both internal and external noises is to increase the source voltage of the transistors in the pull-down network. As the gate voltage has to be greater than the addition of the source voltage and the transistor threshold voltage when a transistor is turned on, higher source voltage directly initiate's to increased gate turn on voltage. Besides, due to the body effect, transistor threshold voltage is increased when the

source voltage rises up. This also aid's to improve gate turn-on voltage.

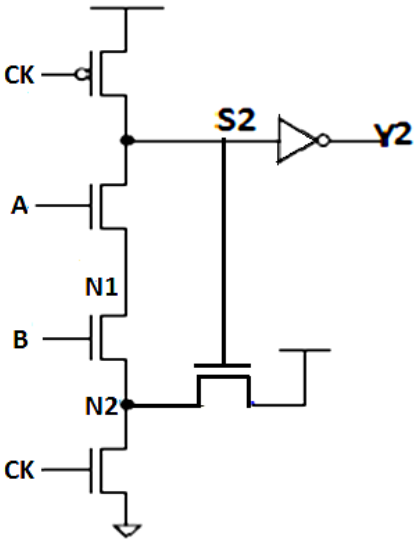

Fig. of source voltage using NMOS

Layout of source voltage using NMOS:- Firstly, we can draw source voltage using NMOS in DSCH screen. For this we can used 1-PMOS, 4-NMOS, 1-Supply, 1-Ground, 1-Butten, 1-LED, 1-NOT gate and connecting wire that can used to give proper connection . Through this we can design source voltage using NMOS. After the completion of design it save in .MSK format.

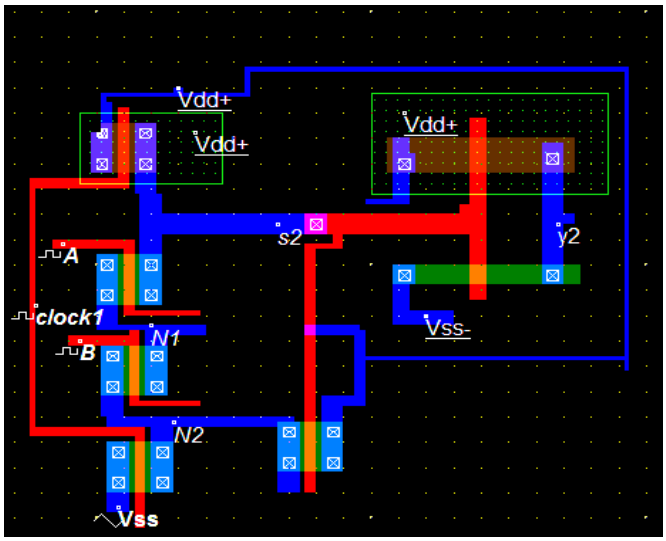

Fig Layout of source voltage with NMOS

Now, we are open Micro wind screen and open saved file. It can generate Lay-out of design circuit, after simulation it can plot graph between:-

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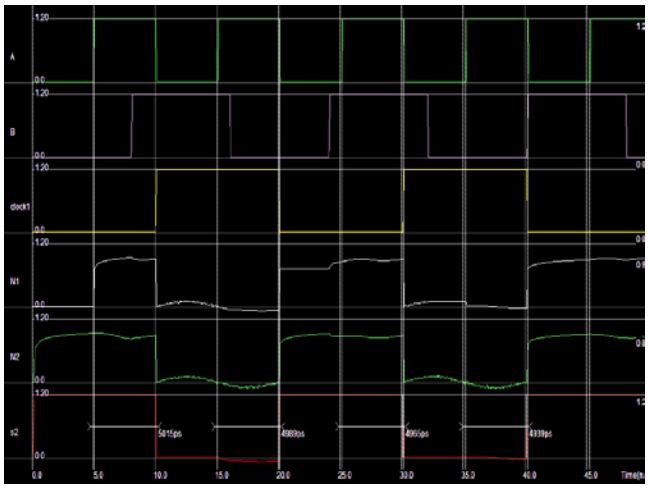

Fig Simulation of source voltage With NMOS

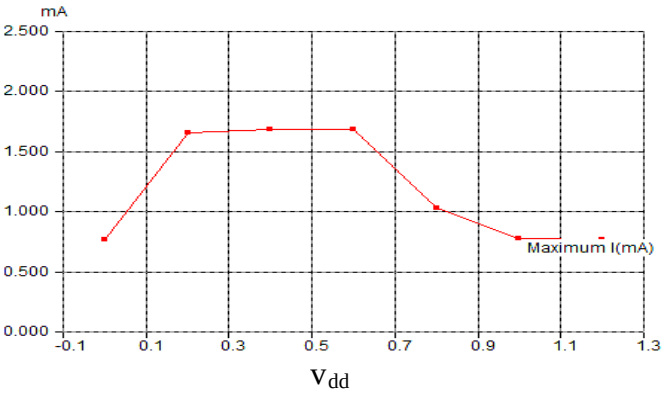

Fig V/I graph of source voltage with NMOS

Parametric analysis table of source voltage using NMOS:-

Through this table we can give the value of rise time, fall time and output current for source voltage using NMOS. This table also shows that the stack technique improves the Rise time, fall time and output current.

Parametric analysis table:

Parametric analysis table of source voltage using NMOS		
Parameter	Rise time	Fall Time
Value	0.75	0.75

Feedback Keeper:

This technique is based on the sleep approach. To maintain logic during sleep mode, the feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

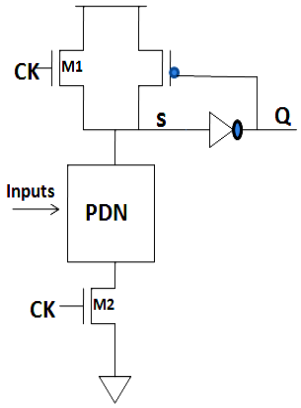

Fig. Feedback keeper

Layout design of feedback keeper logic:-

Firstly, we can design of feedback keeper logic in DSCH screen. For this we can used 1-PMOS, 2-NMOS, 1-Supply, 1-Ground, 1-Butten, 1-LED, 1-NOT gate,1-PDN and connecting wire that can used to give proper connection . Through this we can design of feedback keeper logic. After the completion of design it save in .MSK format.

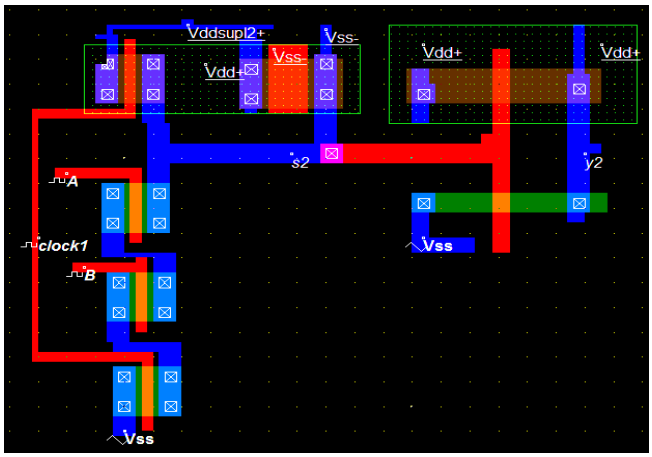

Fig Layout design of feedback keeper logic

Now, we are open Micro wind screen and open saved file. It can generate Lay-out of design circuit, after simulation it can plot graph between:-

- Layout.
- Voltage Vs Time graph.
- Voltage Vs Current graph.
- Frequency and Time graph.

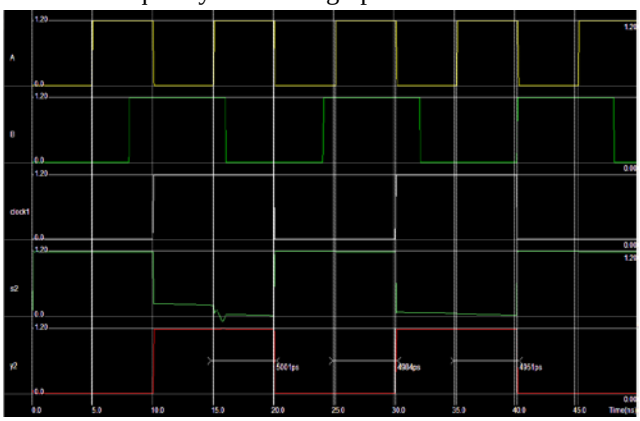

Fig Simulation of Layout design of feedback keeper logic

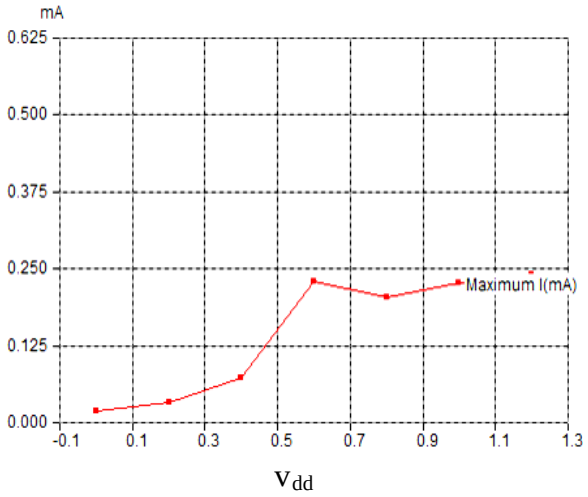

Fig V/I graph of feedback keeper

Parametric analysis table of feedback keeper:-

Through this table we can give the value of rise time, fall time and output current for feedback keeper. This table also shows that the stack technique improves the Rise time, fall time and output current.

Parametric analysis table:

Parametric analysis table of feed back keeper		
Parameter	Rise time	Fall Time
Value	2.605	3.453

Pre-charge internal nodes:

A simple yet effective way to prevent the charge sharing problem is to pre-charge the internal nodes in the pull-down network along with pre-charging the dynamic node S . An example dynamic 2-input AND gate using this technique is illustrated in Fig.4.5.1When all internal nodes are pre-charged, this technique is able to eliminate the charge sharing problem at the cost of using a large number of pre-charge transistors and the increased load capacitance on the clock net. Finally, it is noted that techniques based on pre-charging internal nodes alone are not very effective against external noises.

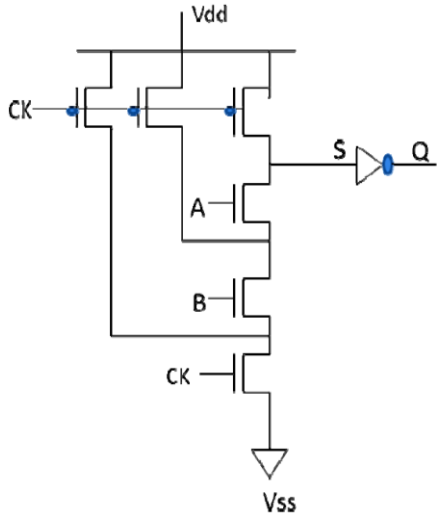

Fig. Pre-charging internal nodes

Layout design of Pre-charging internal nodes logic:-

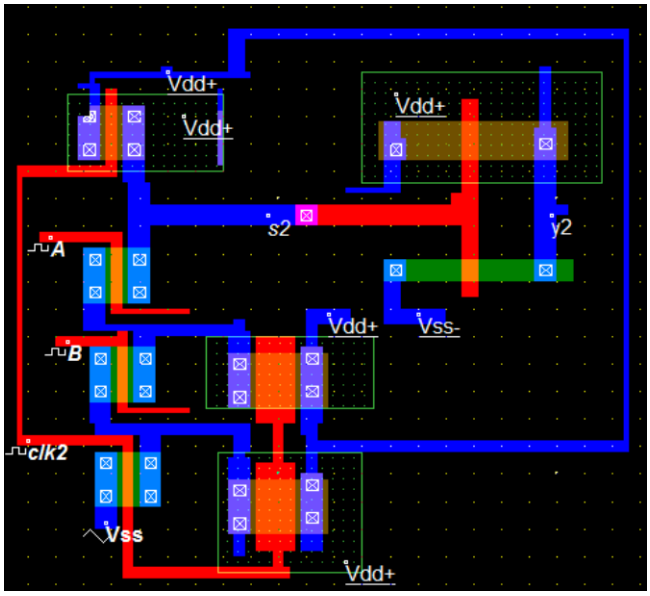

Fig Layout design of pre-charging internal nodes

Firstly, we can design Pre-charging internal nodes logic in DSCH screen. For this we can used 3-PMOS, 3-NMOS, 1-Supply, 1-Ground, 1-Butten, 1-LED, 1-NOT gate,1-PDN and connecting wire that can used to give proper connection. Through this we can design of Pre-charging internal nodes logic. After the completion of design it save in .MSK format.

Now, we are open Micro wind screen and open saved file. It can generate Lay-out of design circuit, after simulation it can plot graph between:-

- Layout.
- Voltage Vs Time graph.
- Voltage Vs Current graph.
- Frequency and Time graph.

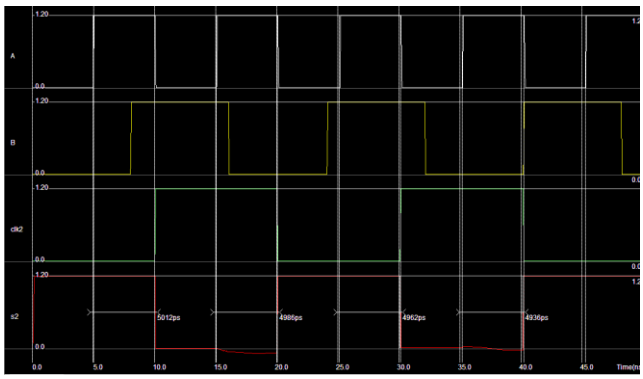

Fig Simulation of pre-charging internal nodes

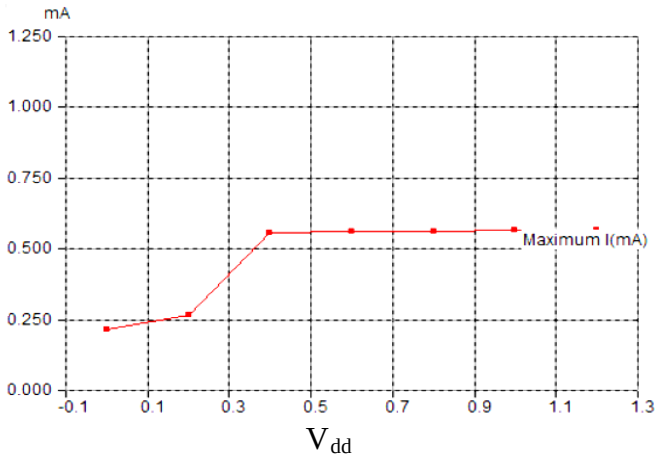

Fig V/I graph of pre-charging internal nodes

Parametric analysis table of pre-charging internal nodes:-

Through this table we can give the value of rise time, fall time and output current for pre-charging internal nodes. This table also shows that the stack technique improves the Rise time, fall time and output current.

Parametric analysis table:

IV. PROPOSED METHODOLOGY

In stack technique, 1-MOS transistor is divided into two half size transistors. When these MOS transistors are turned off together, it induces reverse bias between them which results in the reduction of sub threshold leakage power. However, with increase in the number of transistors overall propagation delay of the circuit increases [12]. Using CMOS technology is basically for consuming less power. In this design criterion it focuses on sub threshold leakage power consumption and it also focuses on body biasing effect and stack effect. One of the main contributors for the static power consumption is sub threshold leakage current which is shown in the Figure i.e. the drain to source current when the gate voltage is smaller than the threshold voltage (Vt). As the technology feature size shrink sub current is increases exponentially as the decrease of threshold voltage. Stacking transistor can reduce sub-threshold leakage. So it is called stacked effect. Where two or more stack transistors are turning off together, then result can reduce.

In complex dynamic logic gates with large pull-down network, charge sharing between the dynamic node and the internal nodes in the pull-down network often results in forged gate switching. A simple yet efficient way to avoid the charge leakage problem is to use stack of transistors in the pull-down network. An example dynamic 2-input AND gate using this technique is illustrated in Fig. In this width of stack of transistors is less than

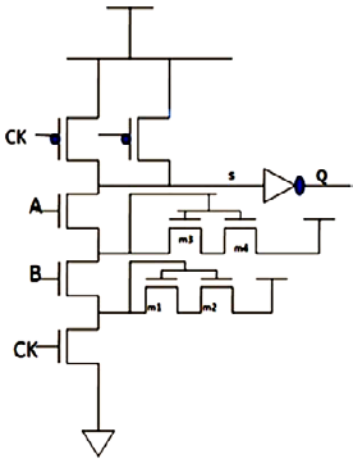

Fig of Proposed stack method

width of other transistors , Like if we take width of other transistors as W, than the width of stacked transistors to be taken as w/2. After implementing this design on software we found that found output current is more and delays found is less.

Parametric analysis table of per charging internal node		
Parameter	Rise time	Fall Time
Value	0.74	0.74

Layout of propose stack method :-

Firstly, we can draw propose stack circuit in DSCH screen. For this we can used 2-PMOS, 7-NMOS, 1-Supply, 1-Ground, 1-Butten, 1-LED, and connecting wire that can used to give proper connection . Through this we can design propose stack circuit. After the completion of design it save in .MSK format.

Now, we are open Micro wind screen and open saved file. It can generate Lay-out of design circuit, after simulation it can plot graph between :-

- Layout.
- Voltage Vs Time graph.
- Voltage Vs Current graph.
- Frequency and Time graph.

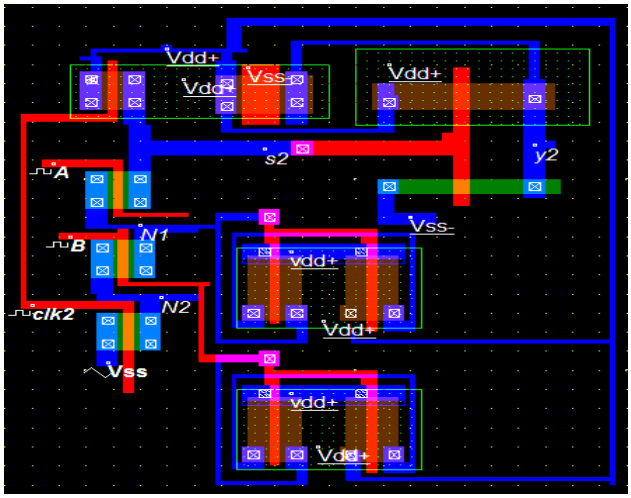

Fig Layout of propose stack method

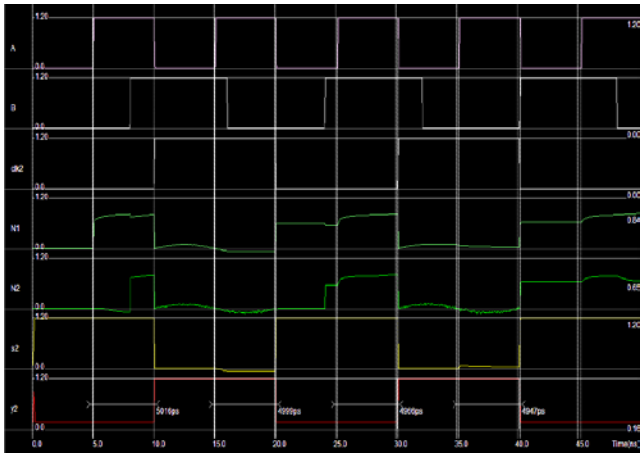

Fig Simulation of Propose stack method

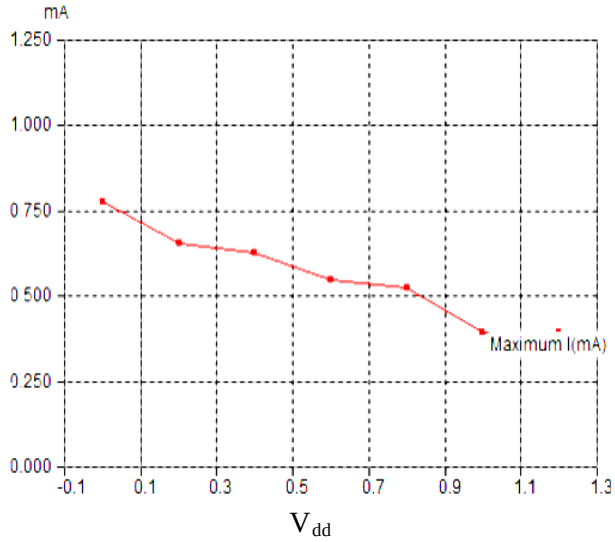

Fig V/I graph of propose stack method

Parametric analysis table of propose stack:-

For the solution of this problem we can used a technique that is called Stack technique. Through this we can improve the Switching speed or response of design circuitry. This technique is also used to reduce leakage current that can improve static power also. Through this table we can give the value of rise time, fall time and output current. This table also shows that the stack technique improves the Rise time, fall time and output current.

Parametric analysis table

Parametric analysis table of propose stack method		
Parameter	Rise time	Fall Time
Value	0.0312	0.0317

V. EXPERIMENTAL RESULT

After implementing certain methods, we have found that stack method has proven to be decreasing rise time and fall time, further it has found that delay is also reduced compared to other techniques.

Comparative result analysis:

As we have compared different techniques of decreasing elements malfunctioning circuits like noise, charge leakage, charge sharing & delay. The comparison is shown in table. The comparison has clearly proved that proposed logic has proven advanced than other ones.

Comparative Parametric analysis table:

In this table we are giving rise time, fall time and output current values for all previous approaches and proposed stack technique. Through this table we compare all values of rise time, fall time and output current and says whose technique is best all of them.

Cell	Rise Time	Fall Time
Source volt with NMOS	0.75	0.75
Source volt with PMOS	0.0342	0.0342
Feedback Keeper	2.605	3.453
Pre-charging internal node	0.74	0.74
Proposed stack logic	0.0312	0.0317

VI. CONCLUSION

Noise or any unwanted signal when enters in a system malfunctions the system, there are various types of noise mainly Thermal noise, Flicker noise ,Voltage transition , etc. All these noises adversely affects the system, there could be certain measures , with the help of which we can decrease noise to a certain extent. Major factor which causes noise are charge leakage and charge sharing problems , thus by using stack transistors we can minimize charge leakage and charge sharing problem and hence minimize noise. The most commonly used dielectric is silicon–di-oxide ,But if we uses high K dielectric material we can minimize noise because the conventional silicon-di-oxide film is too thin e.g. 2nm, to minimize the tunneling current. Thus a slight modification could be done that is The Equivalent Oxide Thickness (EOT) is an essential terminology in high-k field, which indicates how thick a silicon oxide layer would need to be in order to produce the same effect as the high-k material being used. Because the conventional SiO2 film is so thin (e.g. 2

nm) to minimize the tunnelling current and the out diffusion of boron from the gate. If we deposit high-k dielectric materials directly on silicon it results in a very poor interface, and which even has a large amount of defects. A critical solution of this form of a thin SiO2 layer 0.5-0.7nm before deposition of high-k oxide layer with this a high-quality interface between high-k oxides and silicon is restored. The degree to which Noise occurs within a circuit can to a great degree determine the reliability of a circuit. Designers should be versed in knowing about Noise, predicting the occurrences of Noise, and limiting the frequency of Noisy outputs. Ways of limiting Noise include using only one clock, using faster flip-flops, and decrease the asynchronous input frequency, and use synchronization hardware. These steps may easy be get by designers to increase the reliability of a circuit.

- Charge sharing & charge leakage problem is minimized.
- Output current has been enhanced.
- Delay has been reduced that means improve switching response.

VII. FUTURE SCOPE

In this method we can improve the rise time, fall time. In future we are having a target to improve fan-out and power dissipation So in future we can develop a new method that can overcome this problem.

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