Robust Designing of Multiplexer and Ripple Carry Adder using NAND Gate

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Abstract: ***Power consumption technique occupies the major role in designing the VLSI circuit design. Since, there are concerns in power, delay and area. There is no appropriate method/ technique to overcome such limitation, so the best technique needs to be implemented. Thus the two low power digital circuits 4*1 multiplexer and 4-bit ripple carry adder among NAND gate, NAND gate has been designed with Multi Threshold CMOS (MTCMOS) technique. MTCMOS technique offers low leakage and high performance operation by utilizing high speed. Power consumption is calculated individually as Static power and Dynamic power. Static and Dynamic power is compared using 4*1 multiplexer and 4-bit ripple carry adder. The layout design and simulation is done with the help of Micro wind and DSCH tool.***

Keywords: MTCMOS, Ripple carry adder, Multiplexer, Static power, Low leakage, Dynamic power.

I. INTRODUCTION

Power consumption is one of the top major problems in VLSI circuit design. By means of CMOS as the main technology, currently focus on low power is not only because of the recent increasing demands of mobile functions. Power consumption has been the major problem even before the mobile occasion. Ideas on the device level to the architectural level many researchers have proposed many ideas, to solve the power consumption difficulty. Designers are required to desire techniques, in view of the fact that there is no general way to avoid tradeoffs among Power, delay and area.

Mechanisms of power dissipation are typically divided into two types: Static power consumption and Dynamic power consumption [2]. Dynamic power consumption takes place while the circuit is

ready, i.e. the circuit is performing some task on some information. Dynamic power consumption, for the most part caused by the current flow from the charging and discharging of capacitances.

Static power consumption becomes an issue when the circuit is unmoving or in a power down mode. Static dissipation due to sub threshold conduction through OFF transistors channeling current through gate oxide, leakage through reverse-biased diodes, disputation current in measured circuits [2]. Complementary metal-oxide semiconductor (CMOS) technology improvement brings the Performance development and new challenges in VLSI circuit design such as process variation and increasing transistor leakage.

Takes more and more quantity in modern VLSI technology as semiconductor devices are getting lesser and lesser. The following figures show the development of the leakage power in terms invention process. High-performance VLSI design is increasingly necessary with the development of CMOS technology [2].

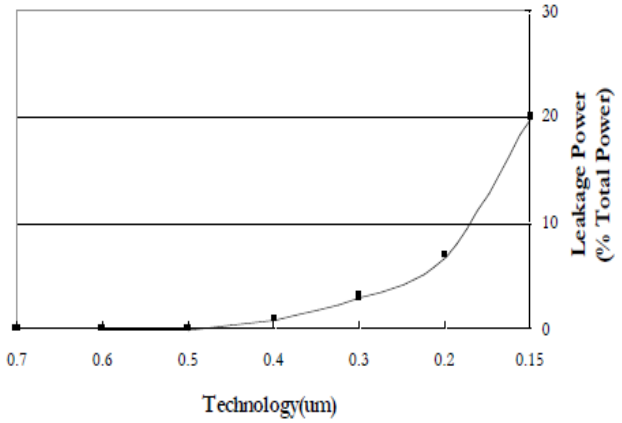

Fig 1.Trend of Leakage Power vs. Technology

The Sub threshold leakage power increase when the leakage power in the given circuit. When the Supply voltage and threshold voltage scales down feature size of Technology also scales down. If Sub threshold voltage increases the power consumption will also be high. To overcome this drawback in this paper we introduce a Multi threshold CMOS technique. These MTCMOS technique is more effective compared to previous

approaches.

II. SYSTEM MODEL

MTCMOS at a high speed with comparatively small power dissipation as compared to usual CMOS [4]. Multi threshold CMOS (MTCMOS) technique has low V_t transistors for logic cells and low leakage, high V_t device as sleep transistors.

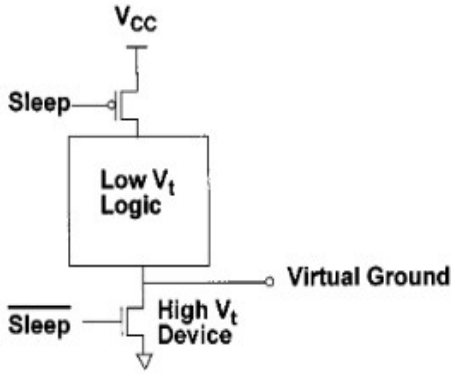

Fig2. MTCMOS Circuit

In MTCMOS technique, transistors of low threshold voltage develop into severed from power supply in whole circuit by using high threshold sleep transistor from the top to bottom. The transistor consist low threshold voltage is used to design low v_t logic as shown in figure2. The sleep transistors are held in reserve by the sleep transistor. This technique during the active mode, the sleep transistor of high voltage v_t is goes to turned on, evaluating both high threshold voltage transistor to turn on and supply a virtual power and low threshold logic to the ground. When the circuit in sleep mode, sleep transistor is available forcing both high Vt transistor to finish and disconnect power lines from the low Vt logic. The transistors of high threshold voltage are used to separate the low v_t logic. The MTCMOS technique, a sleep transistor is further between the real ground and circuit ground named virtual ground [4]. The MTCMOS technique has turn into very popular and there has been important examine towards optimizing its benefits. A well-liked low leakage circuit technique is the Multi threshold Voltage CMOS (MTCMOS).The multi threshold CMOS technique contains two main qualities. First, it works on "active" and "sleep" operational modes are related with MTCMOS technology. Second, two dissimilar types of threshold voltage values are used in support of N channel and P channel MOSFET in a distinct chip. This technique is mainly based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line through disconnect sleep transistors of high threshold voltage (high-Vt). Power gating is another name of MTCMOS technique. The transistors has a low threshold voltage are used to separate the low Vt logic. MTCMOS technology has approach out as a capable another to construct logic gates operating.

ADVANTAGE OF MTCMOS

i. To reduce leakage power.

ii. Lower power consumption

iii. High speed compared to the previous approach.

RIPPLE CARRY ADDER:

An n-bit Ripple Carry Adder (RCA) is a simple flowing of n full adders as shown in Figure 3. In the RCA, the carry bit ripples from one stage of the adder sequence to the next.

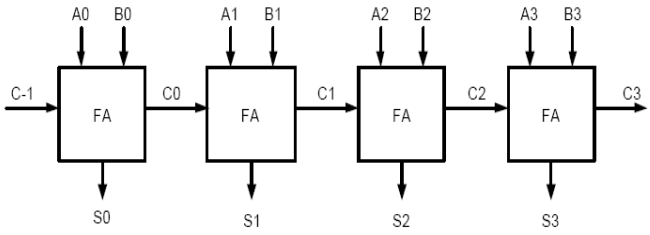

Fig.3. Ripple carry adder architecture

The worst-case delay of the RCA is when a carry signal shift ripples from first to last all stages of adder chain from the least significant bit to the most significant bit, which is estimated by:

$$t= (n-1)\, t_C+t_S$$

Where t_C is the delay through the carry stage of a full adder, and t_S is the delay to calculate the sum of the last stage. The ripple carry adder delay is

linearly proportional to n, the n number of bits; for that reason the performance of the RCA is restricted when n develops bigger. The main advantages of the RCA are lower power consumption as well as a compact layout giving smaller chip area.

MULTIPLEXER

A multiplexer is a combinatorial circuit that is given a certain quantity (usually a power of two) data inputs.

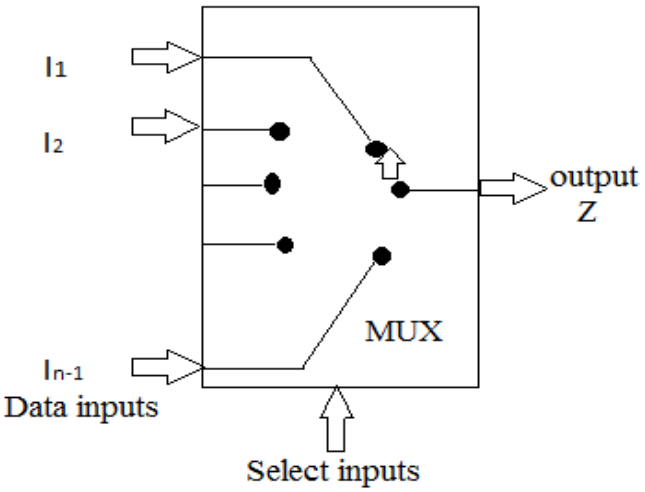

Fig.4. Functional Diagram of MUX

The multiplexer has a 2^n, and n address inputs used as a binary number to select one of the data inputs. The multiplexer contains a single output, which has the similar value as the chosen data input.

III. PREVIOUS WORK

In the previous approaches all work to reduce power consumption in JK master slave flip-flop and 4*1 multiplexer using 2input NAND gate. In that NAND gate using sleepy stack leakage reduction technique with reverse body bias (RBB) and dual threshold CMOS (DTCMOS) to achieve maximum possible static power reduction with optimized results in terms of output waveform and also attained dynamic power consumption and delay. During the active mode sleep switches S_1 and S_2 have been kept ON and in the idle state this sleep switches have been kept OFF to cut off the path of supply to the ground.

Below RBB and DTCMOS techniques are explained.

REVERSE BODY BIAS (RBB)

Reverse body biasing (RBB) is one of the most widely used methods to reduce sub threshold leakage. However, the increasing RBB increases drain-induced barrier lowering (DIBL) and substrate doping density, which leads to an increasing of band-to-band tunnelling leakage. At the same time, increasing of RBB will increase VTH, causing short channel effect in ultra-small technology, which results in an increase of gate tunnelling leakage [5].

To monitor the leakage current components, ISUBTH, IBTBT, and gate induced drain leakage (IGIDL) currents, are generated from a test device and convert the difference of ISUBTH and IBTBT current into voltage signals assuming the gate tunnelling leakage is not as large as the other two leakage components [5].

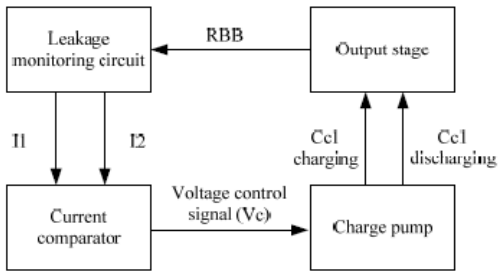

Fig.5. Block Diagram of Optimal RBB Generating System

The converted voltage called “Vc” goes to the charge pump. In this charge pump to charge and discharge the capacitor. The capacitor of the voltage is fed back to the leakage monitoring circuit through the output stage in the Figure 4 to control the body bias voltage of the test device to reduce the total leakage and to form a closed loop.

This closed loop is necessary to build the scheme adaptive and to maintain the optimal body bias status continuously.

A most favourable RBB is accomplished and maintained in the steady state if the two leakage currents become equal [5].

DUAL THRESHOLD CMOS (DTCMOS)

Data signals traverse integrated circuits through different paths of logic gates whereas the start- and endpoints of these paths are marked by sequential elements like registers. The maximum frequency to clock the registers is determined by the path with the longest propagation delay, called critical path. Thus, it is possible to trade off delay for leakage in all previous, non-critical paths. Such an attempt is exploited by the Dual Threshold CMOS (DTCMOS) design technique [6].

DRAWBACKS

The following are the drawbacks of DTCMOS and RBB:

Vth variation cannot be always success at low voltage supplies.

i. Increasing the number of critical paths will sometimes hurt circuit performance.

ii. Increase PN junction reverse leakage.

iii. Scaling down technology aggravate short channel effects and weaken the Vth modulation capability.

IV. PROPOSED METHODOLOGY

In our proposed work we have designed two digital circuits 4*1 MUX and 4bit ripple carry adder with low power NAND gate. In this NAND gate we have used MTCMOS technique which works better than the existing techniques where power efficient is low. The MTCMOS is a very effective technique is to reduce the leakage power of circuits. The MTCMOS technology gives low leakage and high performance operation by operating high speed. In this logic circuit 4*1 MUX and 4-bit ripple adder power is compared and Static and Dynamic power is calculated separately.

4-BIT RIPPLE CARRY ADDER USING NAND GATE

Multiple full adders can be connected with the carry output of one adder connected to the carry input of the next adder. Both a half adder and a full adder use a least significant bit with the carry input together to zero.

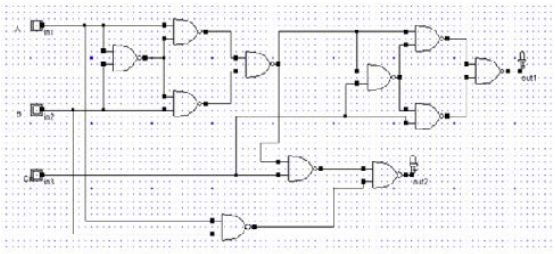

Fig.6. RCA using NAND gate

Having a carry input for the least significant bit is valuable for connecting small adders to make more adders or for making an adder. To add an n-bit number full adder circuits can be cascaded in parallel n number of full adder circuits are used for an n-bit equivalent adder.A ripple carry adder is a logic circuit in which each full adder is carried. It is called as ripple carry adder because each carry bit is rippled into the next stage Below a 4-Bit ripple carry adder have been designed with NAND gate is shown as figure 6,

Below the Truth table of Ripple carry adder is shown.

Input Bit for Number		Carry Input(C/CI)	Sum bit Output(S)	Carry Bit output(Co)
A	B			
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth table of Ripple carry adder

4*1 MULTIPLEXER USING NAND GATE

A multiplexer (MUX) is an electronic device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2'' input is used to select which input line to send to the output. To increase the amount of data multiplexers are mainly used which is also called as data selector.

Figure 7 4*1 Multiplexer using NAND gate circuit is shown below.

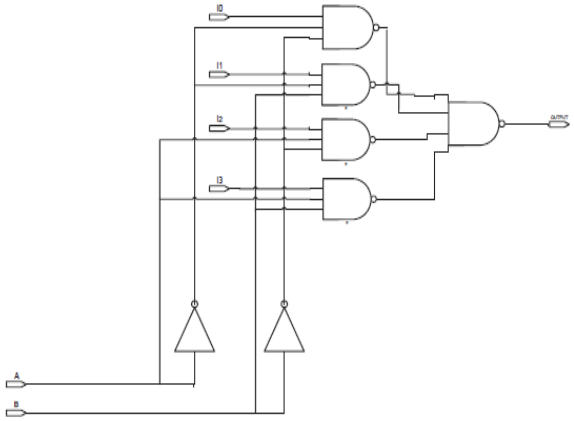

Fig.7. Multiplexer Using NAND Gate

A 4*1 multiplexer has 4 input lines (D0, D1, D2, and D3), two select inputs (S0& S1), and one output line Y. Below the Truth table for a 4*1 multiplexer is shown.

S_1	S_0	D_3	D_2	D_1	D_0	Y
0	0	X	X	X	0	0

0	0	X	X	X	1	1
0	1	X	X	0	X	0
0	1	X	X	1	X	1
1	0	X	0	X	X	0
1	0	X	1	X	X	1
1	1	0	X	X	X	0
1	1	1	X	X	X	1

Table 2: Truth table of 4*1 multiplexer

The proposed system illustrates application of power saving MTCMOS technique on 4:1 MUX using NAND gate structural design. NAND using MUX contains three NAND gate and one inverter only. We have applied MTCMOS technique on 4*1 multiplexer and 4-bit ripple carry adder.

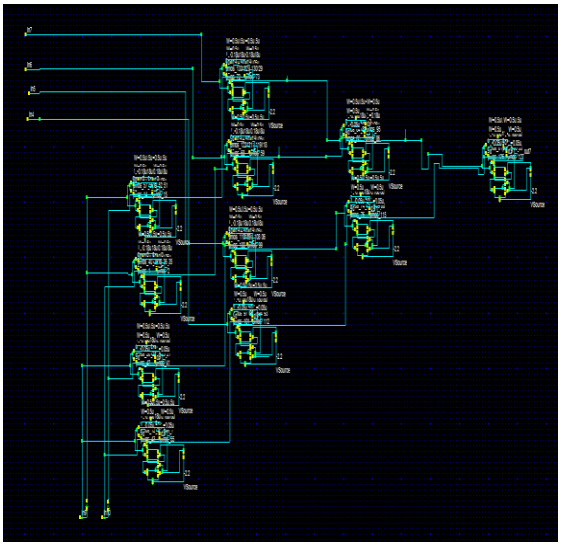

Fig 7: Schematic Diagram of 4*1 MUX with MTCMOS

The MTCMOS is a very effective technique is to reduce the leakage power of given circuits. The multi threshold voltage CMOS technique is basically for reducing leakage power and sub threshold voltage. The circuit design & circuit logic verification here we apply DSCH (Digital schematic), for CMOS layout verification & power computation of the circuit we use a MWND (Microwind) tool.

The Dynamic circuit of 4*1 MUX with MTCMOS technique is shown below.

The Static circuit of 4*1 MUX with MTCMOS technique is shown below.

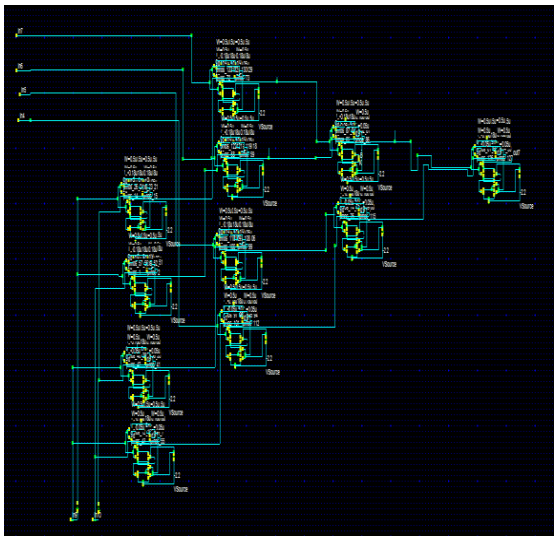

Fig 8: Schematic diagram of 4*1 MUX with MTCMOS

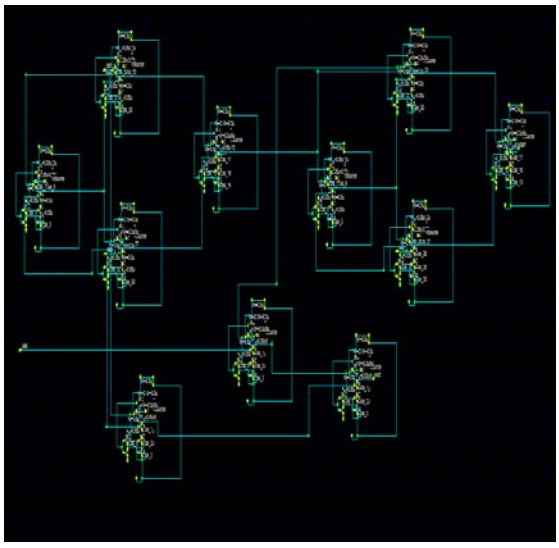

Fig 7: Schematic Diagram of 4-bit Ripple Carry Adder with MTCMOS

The application of power saving MTCMOS technique is used by 4bit ripple carry adder. The multi threshold voltage CMOS technique is basically for reducing leakage power and sub threshold voltage. The circuit design & circuit logic verification here we apply DSCH (Digital schematic), for CMOS layout verification & power computation of the circuit we use a MWND (Microwind) tool.

The Dynamic circuit of 4-bit Ripple Carry Adder with MTCMOS technique is shown below

The Static circuit of 4-bit Ripple Carry Adder with

MTCMOS technique is shown below.

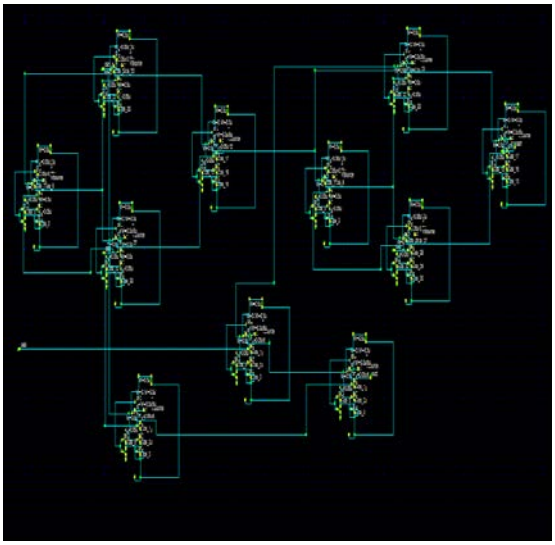

Fig 8: Schematic diagram of 4-bit Ripple Carry Adder with MTCMOS

V. SIMULATION

The circuits of NAND gate based on 4*1 Multiplexer and 4-bit ripple carry adder were designed in CMOS technology. On each of these circuits the one leakage reduction technique, MTCMOS have been implemented. The delay, dynamic power and static power are calculated on Microwind and Dsch tools.

Fig.11 and 12 is the output waveform of 4-bit Ripple Carry Adder with multi threshold CMOS technique. By analysis this output we get power dissipation and delay.

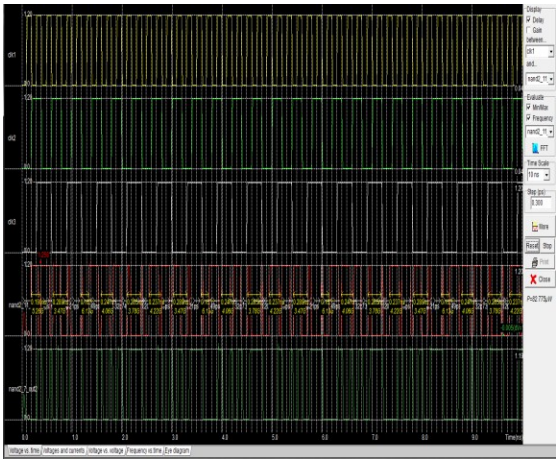

Fig.11: Output waveform of 4-bit Ripple Carry Adder (Dynamic power)

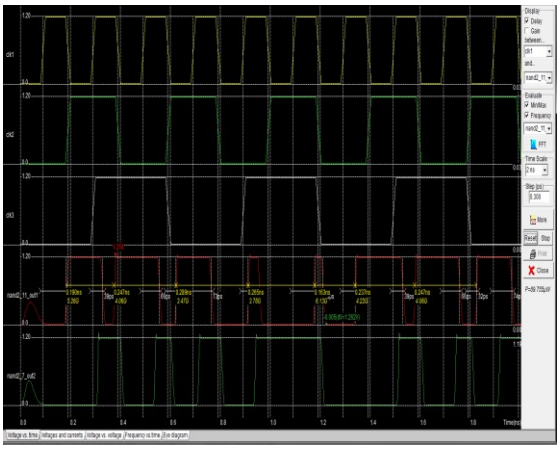

Fig.12: Output waveform of 4-bit Ripple Carry Adder (Static power)

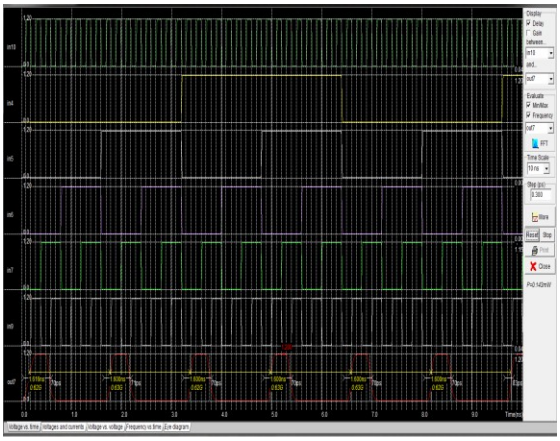

Fig.11: Output waveform of 4*1 Multiplexer (Dynamic power)

Fig.11 and 12 is the output waveform of 4*1 Multiplexer with multi threshold CMOS technique. By analysis this output we get power dissipation and delay.

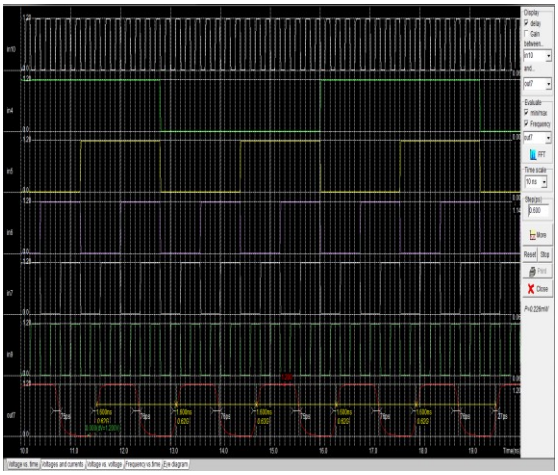

Fig.12: Output waveform of 4*1 Multiplexer (Static power)

In Table 3, the performance of designed adder and multiplexer was analyzed and compared with the different parameter. And the comparison of the static power, dynamic power and delay for 4-bit adder and 4*1 multiplexer circuits. Table3. Below represents the above result graphically.

CMOS logic	Static power	Dynamic power	Delay
4-bit RCA	83.34µw	99.69µw	0.125ns
4*1 MUX	0.143mw	0.244mw	1.616ns

Table 2: Comparison of 4-bit adder and 4*1 multiplexer

VI. CONCLUSION

In this paper, the effect of optimization of leakage power is observed by application Multi threshold CMOS on two different structures such as 4-bit ripple carry adder and 4*1 multiplexer using CMOS NAND gate has been measured. Using this technique, effective at ultra low supply voltages is potential for high speed circuits. We are achieving static power reduction maximum up to 59.30% in 4*1 multiplexer and 99.74% in 4-bit ripple carry adder but with 55.54% and 4.67% increment in delay in multiplexer and ripple carry adder respectively. Dynamic power consumption has been reduced up to 34.32% and 13.59% in multiplexer and ripple carry adder respectively.

VII. FUTURE SCOPE

The proposed technique consumes less power and high speed compared to previous techniques. As the future work, we are going to do the advanced research and accuracy improvement of the Multi threshold CMOS technique.

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