Performance Analysis of 5-level H-bridge Multilevel Inverter

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Abstract - This paper presents with the simulation and testing of 5-level H-bridge multilevel inverter. This paper presents 5level inverter with harmonics reduction along with the reduction in number of switches. . In this paper modeling and evaluation of 5-level PWM inverter is carried out & also a evaluation with conventional 2-level inverter is made. The percentage (%) total harmonic distortion is intended for 5-level inverter. The harmonic reduction is achieved by PWM method. The functionality confirmation of the 5-level inverter is done using MATLAB. The result of simulation is confirmed by experimentation.

Keywords: Cascaded multilevel inverter, 5-level inverter ,modulation techniques.

I. INTRODUCTION

The voltage source inverters generate an output voltage or a current with levels either 0 or +Vdc or –Vdc. They are recognized as the two-level inverter. To gain a quality output voltage or a current waveform with a minimum number of ripple substances, they require high switching frequency along with various pulse-width modulation (PWM) techniques. In upper level power and upper level voltage applications, these two-level inverters, have some restrictions in operating at high frequency mainly due to switching losses and constraints of device ratings. The major shortcomings of conventional 2-level inverters are Large dv/dt and di/dt ratings of switches, Static and dynamic voltage sharing difficulty among devices, Switching frequency, Switches must have very low turn-on and turn-off times for high power applications due to very high switching frequencies. Top order harmonics contents have been recognised, and large common mode voltages have been generated across industrial motor phases. furthermore, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series-parallel combinations that are necessary to obtain potential of usage high voltages and current.

The multilevel inverters have drawn wonderful interest in the power industry. They propose a new set of description that are well suited for the reactive power compensation. It may be easier to produce a upper level-power, upper level-voltage inverter with the multilevel structure. Increasing the number of voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating. The exclusive structure of multilevel voltage source inverters allows them to reach upper level voltages with low harmonics without the use of transformers or series connected harmonized switching devices. As the voltage levels increases, the harmonic substance of the output voltage waveform decreases appreciably.[2]

Multi-level inverters with the pulse width modulation techniques are gaining more meaning due to the fact that the lower order harmonics in the output waveform can be eliminated without any increase in the higher order harmonics, unlike the 2-level PWM inverters. The high level output voltage can be achieved with multi-level PWM inverters without using transformers or series connected switching devices. In this thesis modeling and evaluation of 5-level PWM inverter is carried out & also a evaluation with conventional 2-level inverter is made.

II. SYSTEM MODEL

In this section firing scheme is shown below and power stage firing scheme will be discussed and model is shown in last section . [1]

In this section the proposed control scheme is explained. It is developed in a manner that it can be applied to all topologies of multilevel inverters.[1]. For a given inverter, let the number of levels in the phase voltage be N_{Level}. A voltage source inverter allows multilevel operation if N_{Level}

N_{Level} is considered to be odd. Also, number of positive levels in an N_{Level} waveform will be: $N = (N_{Level} - 1) / 2$

The modulating signal, f_{ref} (t), is sinusoidal waveform with amplitude A_{ref} and angular frequency $\dot{A}_{ref}$. There should be 2N carrier signals which are all triangular for sinusoidal PWM and are constants for low frequency schemes like SHE. These carriers have the angular frequency $\dot{A}_{car}$ and peak-to-peak amplitude A_{car}. Carrier signals upper the zero

reference are designated as $f +_{car},j$ (t) and those below the zero reference are designated as $f -_{car},j(t)$, { j = 1 to N }. Carrier signals are disposed such that they occupy contiguous bands and zero reference is placed in the middle . Accordingly following quantities can be defined:

Frequency modulation index, $P = \dot{A}_{car} / \dot{A}_{ref}$

'P'dictates the switching frequency of the power switches and the harmonic profile of the output waveform. Amplitude modulation index, $M = A_{ref} / (N A_{car})$

'M'dictates the number of levels in the output waveform and its peak value.

At every moment, each carrier is compared with the modulating signal. For all carrier signals upper the zero reference each evaluation gives '1' if the modulating signal is greater than carrier and '0' otherwise. For all carrier signals below the zero reference , each comparison gives '0' if the modulating signal's greater than the

$$f +_{out},j(t) = 1, \text{ for } f_{ref}(t) > f +_{car},j(t)$$

$$= 0, \text{ otherwise} \quad (1)$$

$$f -_{out},j(t) = 0, \text{ for } f_{ref}(t) < f -_{car},j(t)$$

$$= -1, \text{ otherwise} \quad (2)$$

The results so obtained are added, there by synthesising a signal called as aggregate signal as designated as $f_{agg}(t)$. That is

$$f_{agg}(t) = \sum \{f +_{out},j(t) + f -_{out},j(t)\}$$

In this model there are three stage for analysis of description given below.

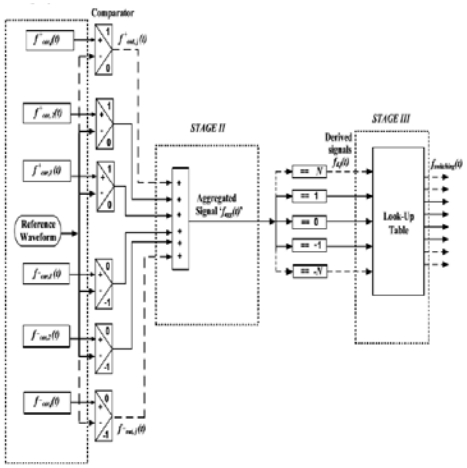
(a) Stage I: appropriate selection of carriers and reference enables the proposed scheme to incorporate required modulation strategy[1].(discussed in section 3)

(b) Stage II: appropriate manipulations with the aggregated flexibility to implement charge balance control in input DC sources. An example of such manipulation is demonstrated in Section 4.

(c) Stage III: look-table can be formulated based on the topology and hence the scheme is applicable to all multilevel topologies

In this paper simulations are shown and the analysis of the output voltage and current waveform have been done by performing the FFT analysis to draw the conclusion for the most superior type of multilevel inverter. The waveforms are analysed in terms of the output voltage magnitude and THD for the input DC voltage. Firstly the normal inverter is modeled then cascaded 5 level and OTC CHB inverter is modeled [3]and simulated. Then their A three-phase CMI topology is basically composed of three similar to phase legs of the series-chain of H-bridge converters, which can possibly produce dissimilar output voltage waveforms and offers the potential for AC system phase-balancing, this topology consists of series power conversion cells, the voltage and power level may be with no trouble scaled. The dc link supply for each full bridge converter is provided individually, The converter topology is based on the series connection of single-phase inverters with separate dc sources. In chapter 5 Fig. shows the Simulink model for five-level cascaded inverter. The resulting output ac voltage swings from $-2V_{dc}$ to $+2V_{dc}$ with five-level. The staircase waveform is nearly sinusoidal, even without filtering. Then it consist of Load voltage THD analysis, Load current THD analysis OTCHB model and output waveform Voltage THD analysis.[4][6]

Comparison will be done using MATLAB software on the basis of following aspects: (1)The Total Harmonics Distortion of output voltage(2).Number of main switching devices required.(3)Number of diodes, capacitors required(4)Wave shape of the output voltage.



2.1 firing scheme

III. PREVIOUS WORK

(Shailendra jain at etl.)In The control techniques can be broadly classified as PWM (e.g. sinusoidal, space vector and sigma-delta) and stepped (e.g. selective harmonic elimination (SHE)). As for space-vector PWM is

concerned, when the number of output level is more than five, the scheme becomes very complicated and so the carrier based PWM methods is more feasible in multilevel inverters. In this section, a generalized control strategy is developed using carrier-based modulation methods and S H E method. A brief description of these schemes is made first.[1][2]

3.3.1 Multicarrier Sine wave

PWM Multilevel carrier based PWM methods have multiple carriers which can be triangular waves or sawtooth waves. Thus, by using these combinations, many multilevel carrier-based PWM methods can be find. [5] [1]

Carrier- based modulation schemes are basically categorised as:

level-shift PWM (LSPWM), phase-shifted PWM (PSPWM) and hybrid (H). They are briefly described below.

A. Level-Shift PWM

(i) Alternative phase opposition disposition (APOD): As the name suggests, the carrier waveforms are so disposed that carriers are alternatively phase displaced from each other by 180 degrees. Carrier and reference waveforms for five level inverter are as in Fig. 3.1(a).

(ii) Phase disposition (PD): In this scheme, all the carriers are in phase. Carrier and reference waveforms for a five level output waveform are as in Fig.3.1(b).

(iii) Phase opposition dispositions (POD): In this scheme, the carriers are all in phase above and below the zero reference, with a phase shift of 180 degrees between those above and below zero reference. Carrier and reference waveforms for a five level output waveform are as in Fig. 3.1(c).

B. Phase Shifted PWM

In this scheme, the carriers have same amplitude and all of them are appropriately phase shifted.

C. Hybrid (H)

This scheme combines level-shifted and phase-shifted techniques as in Fig. 3.1(d).

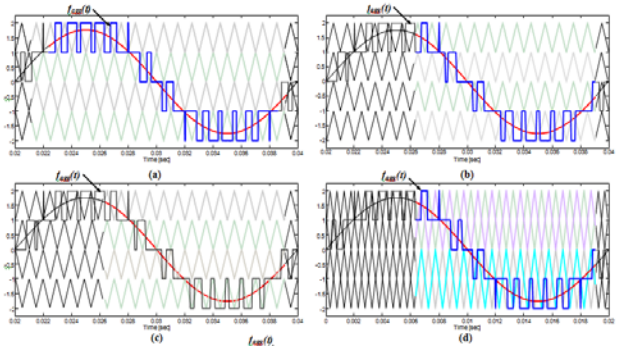


Fig. 3.1 Multilevel PWM and Multistepped Modulation Schemes (a)APOD (b)PD (c)POD (d)Hybrid

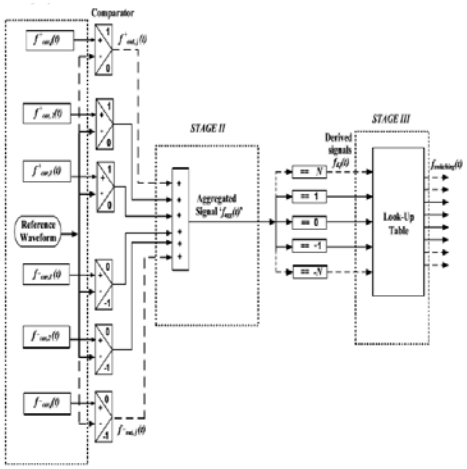


Fig. 3.2 Firing scheme

IV. PROPOSED METHODOLOGY

On the basis of previous section work discuss modeling of different types of 5-level multilevel inverters

4.1 Introduction

In this chapter the modeling of the conventional H-Bridge and the transistor clamped H-Bridge inverter is done in the cascaded configuration which is the most popular topology out of the available configurations of the multilevel inverters. In the first part of this chapter the single cells each of the conventional H-Bridge as well as the transistor clamped H-Bridge is modeled and simulated for the same rating of the input DC voltage source and the IGBT of the same rating are used as the conducting switches. These two types of H-Bridges are compared in the no. of switching devices used, the number of level the output voltage so formed etc. And in the second part the two 5-level inverters are modeled and simulated one is made using the conventional H-Bridge and the other is made using transistor clamped H-Bridge and then the comparison is done between

these two different types of 5-level inverters. If we use two cells of conventional H-Bridge we get 5-level in output voltage where as only single cell is needed in case of transistor clamped H-Bridge.[12] Thus if we use two cells of transistor clamped H-Bridge we get a 9-level inverter hence this inverter is also modeled. In the modeling and simulation of all these inverters similar pulse width modulation is used[13].

4.2.1 Modeling of Conventional H-Bridge

For the modeling of the single cell of conventional H-Bridge it requires a DC voltage source and main four conducting switches thus constituting a H-Bridge. The two anti parallel switches conducts for positive half cycle and the other set of anti parallel diodes conduct for the negative half cycle. Fig.4.1 shows the simulink model of the single unit of the conventional H-Bridge and table 4.1 shows the conduction of the various switches at a particular instant of time.

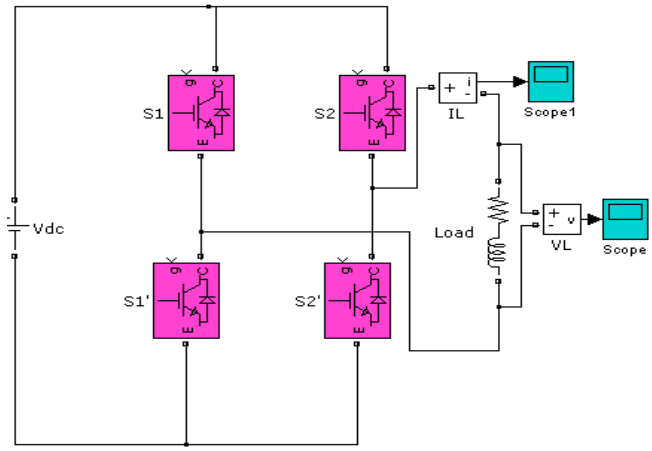


Fig 4.1 Conventional H-Bridge inverter

Table 4.1: Conduction Chart for Conventional H-Bridge inverter

Output-Voltage level	Vdc	0	-Vdc
S1	1	1	0
S2	0	0	1
S1’	0	0	1
S2’	1	0	0

4.3 Modeling of using CHB based 5-level Cascaded Multilevel Inverter

The single unit of the conventional H-Bridge constitutes a 3-level inverter. For the modeling of this type 5-level inverter it requires two cells of conventional H-Bridge. Hence the total number of the switching devices used for this inverter will be twice of that used in the single unit. Now the total number of the main conducting switches will be 8, the voltage sources required will be two. The circuit of the pulse generation will also undergoes a change as now it will require four carrier signals and based on that the number of logical operators needed will also increased. Fig.5.3 shows the simulink model of the 5-level cascaded inverter using the conventional H-Bridge and table 5.3 shows conduction chart for this inverter.

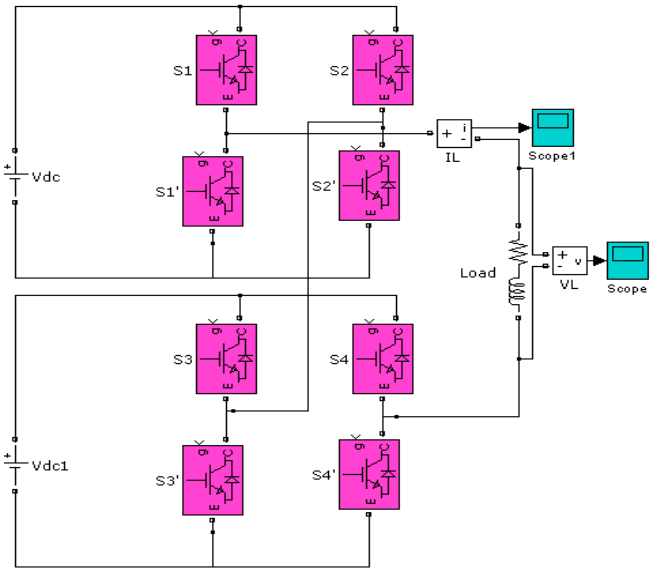


Fig 4.2 CHB based 5-level Cascaded Multilevel Inverter

4.4 Multicarrier Based Sinusoidal Pulse Width Modulation

Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have the controlled output voltage. There are vareity of modulation techniques available. Basically the control technique can be classified as the pulse width modulation which is considered as the most efficient method. This PWM is further divided into various PWM techniques such as single pulse PWM, space vector PWM, multiple pulse PWM, phase displacement control. For this proposed topology we are using the multicarrier based control technique which can be applied to all the topologies of the multilevel inverter. For any given number of levels in the output voltage the number of carrier to be used is given as N-1 Where N is the number of levels in the output voltage. Fig. represents the triangular shape carrier waveform and the sinusoidal reference signal showing the pulse width modulation technique used for the control. Simply a reference signal is taken which is a sinusoidal signal of 50Hz frequency and this reference is compared with the carrier signal which are the triangular wave .The modulation index we are using in this modulation

technique is 0.95.The advantage of this scheme is that it offers the charge balance control in the input DC sources and voltage across the capacitor are also balanced.[10] Fig. shows the voltage across the two capacitors` which are equal in magnitude[7][8].

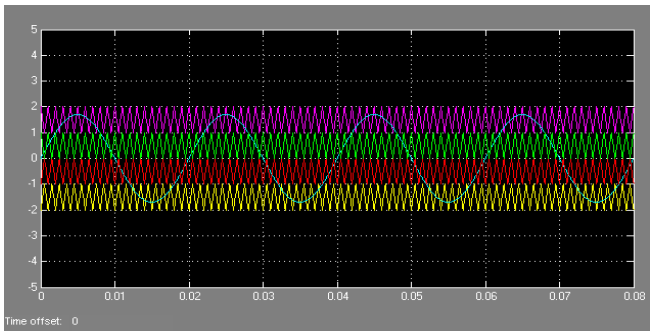


Fig 4.4 Multicarrier based PWM control scheme

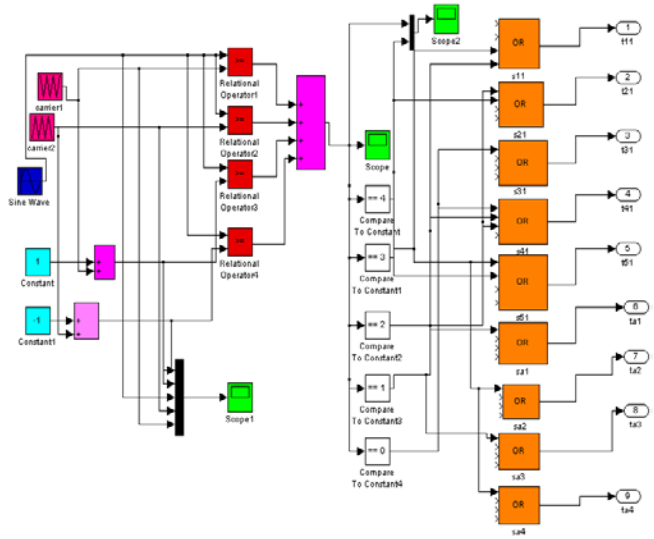


Fig 4.5 Modeling of Sinusoidal Pulse Width Modulation Scheme

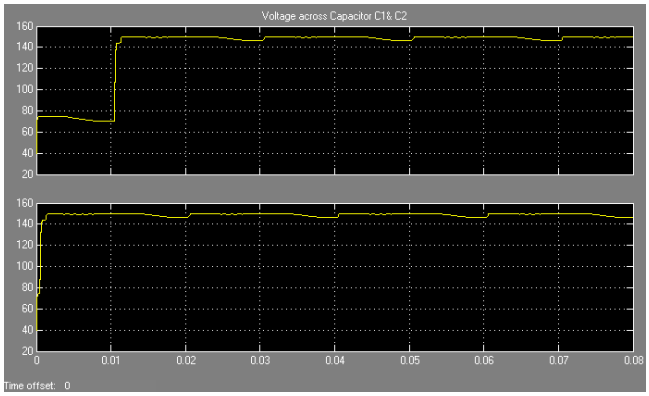


Fig 4.6 Voltage across the Capacitors of TCHB

V. SIMULATION/EXPERIMENTAL RESULTS

5.1 Result Analysis:

In this chapter different types of the cascaded multilevel inverter have been modeled and simulated for the same input DC voltage. The results of the simulations are shown and the analysis of the output voltage and current waveform have been done by performing the FFT analysis to draw the conclusion for the most superior type of multilevel inverter. The waveforms are analysed in terms of the output voltage magnitude and THD for the input DC voltage. Firstly the normal inverter is modeled then cascaded 5 level and OTCHB inverter is modeled and simulated.[9]

5.2 Modeling of Normal inverter

For the modeling of normal inverter, 4 switches are used and controller is designed to provide specific pulses to get the desired output. The two anti parallel switches conducts for positive half cycle and the other set of anti parallel switches conduct for the negative half cycle. Fig.5.1 shows the simulink model of the Normal inverter. In normal inverter there are three different possible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. Tthree-level inverter, a set of two switches is on at any given time. Switching states of the three level inverter are summarized in Table-1

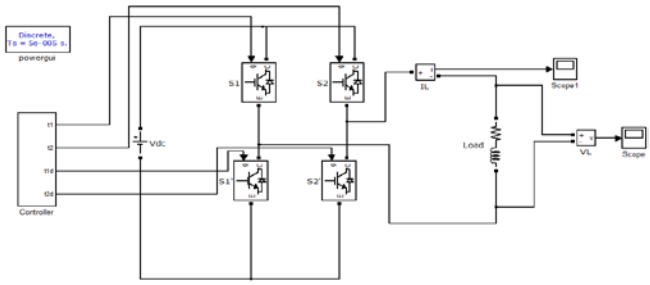


Fig.5.1 simulink model of Normal inverter

Table 1 Switching states in Normal inverter

Switch status	state	Pole voltage
S_1=ON,S_2=ON $S_{1'}$=OFF,$S_{2'}$=OFF	S=+ve	$V_{ao}=V_{dc}$
S_1=OFF,S_2=ON $S_{1'}$=ON,$S_{2'}$=OFF	S=0	$V_{ao}=0$
S_1=OFF,S_2=OFF $S_{1'}$=ON,$S_{2'}$=ON	S=-ve	$V_{ao}=-V_{dc}$

5.3 Control signal waveform

For control signal waveform shown below.

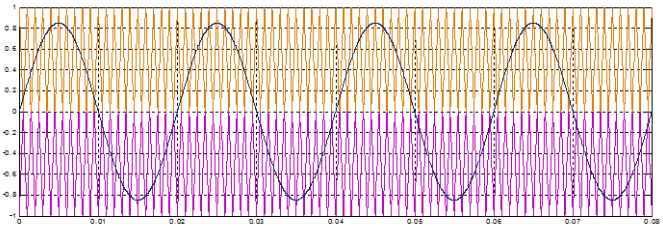


Fig.5.2 control signal waveform

5.4 Pulse analysis for normal inverter

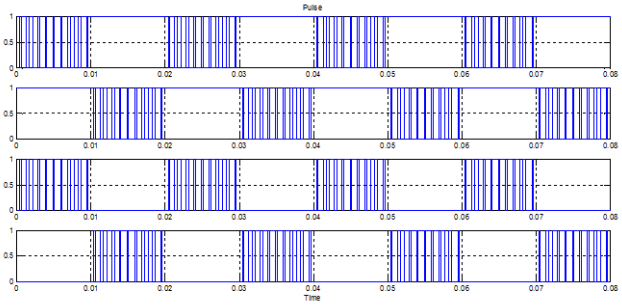


Fig 5.3 shows pulse analysis of the Normal inverter in the balanced condition

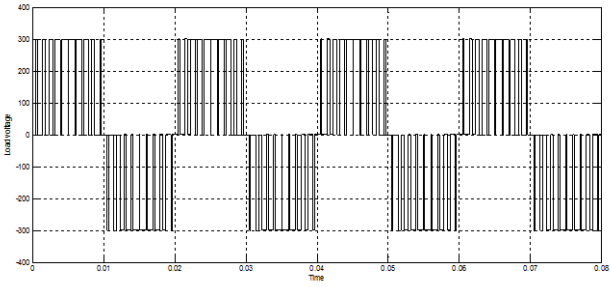
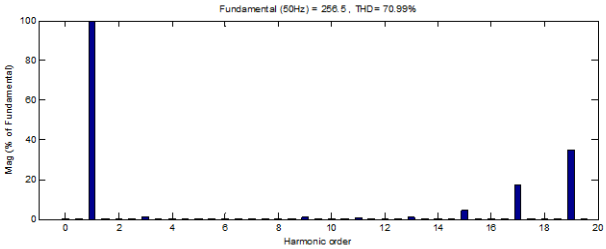


Fig 5.4 shows the load voltage of the Normal inverter in the balanced condition



Total Harmonic Distortion (THD) = 70.99%

0 Hz	(DC) :	0.00%	270.0°
25 Hz		0.00%	248.9°
50 Hz	(Fnd) :	100.00%	0.0°
75 Hz		0.00%	221.0°
100 Hz	(h2) :	0.00%	215.4°
125 Hz		0.00%	208.1°
150 Hz	(h3) :	0.87%	0.0°
175 Hz		0.00%	201.6°
200 Hz	(h4) :	0.00%	200.2°
225 Hz		0.00%	197.8°
250 Hz	(h5) :	0.26%	0.0°
275 Hz		0.00%	195.5°
300 Hz	(h6) :	0.00%	195.1°
325 Hz		0.00%	194.0°
350 Hz	(h7) :	0.33%	0.0°
375 Hz		0.00%	193.0°
400 Hz	(h8) :	0.00%	192.7°
425 Hz		0.00%	192.4°
450 Hz	(h9) :	1.02%	0.0°
475 Hz		0.00%	191.9°
500 Hz	(h10) :	0.00%	191.9°
525 Hz		0.00%	191.6°
550 Hz	(h11) :	0.41%	170.1°
575 Hz		0.00%	191.5°
600 Hz	(h12) :	0.00%	190.8°
625 Hz		0.00%	191.4°
650 Hz	(h13) :	0.87%	0.0°
675 Hz		0.00%	191.4°
700 Hz	(h14) :	0.00%	189.8°
725 Hz		0.00%	191.6°
750 Hz	(h15) :	4.32%	0.0°
775 Hz		0.00%	191.6°
800 Hz	(h16) :	0.00%	188.5°
825 Hz		0.00%	191.8°
850 Hz	(h17) :	17.35%	0.0°
875 Hz		0.00%	191.6°

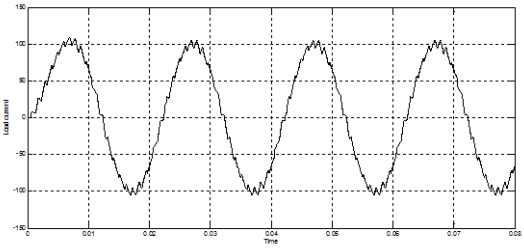
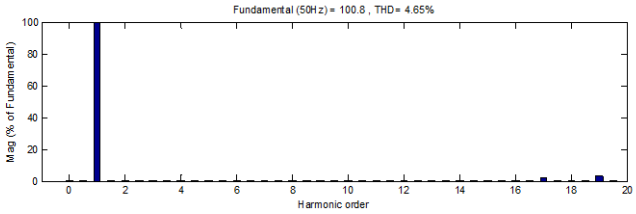


Fig 5.5 Voltage THD analysis and load current waveform



Total Harmonic Distortion (THD) = 4.65%

0 Hz	(DC) :	0.00%	90.0°
25 Hz		0.00%	68.8°
50 Hz	(Fnd) :	100.00%	0.0°
75 Hz		0.00%	41.0°
100 Hz	(h2) :	0.00%	33.4°
125 Hz		0.00%	28.1°
150 Hz	(h3) :	0.43%	0.0°
175 Hz		0.00%	21.6°
200 Hz	(h4) :	0.00%	19.5°
225 Hz		0.00%	17.8°
250 Hz	(h5) :	0.08%	0.0°
275 Hz		0.00%	15.5°
300 Hz	(h6) :	0.00%	14.7°
325 Hz		0.00%	14.0°
350 Hz	(h7) :	0.08%	0.0°
375 Hz		0.00%	13.0°
400 Hz	(h8) :	0.00%	12.6°
425 Hz		0.00%	12.3°
450 Hz	(h9) :	0.18%	0.0°
475 Hz		0.00%	11.9°
500 Hz	(h10) :	0.00%	11.7°
525 Hz		0.00%	11.6°
550 Hz	(h11) :	0.06%	86.4°
575 Hz		0.00%	11.5°
600 Hz	(h12) :	0.00%	11.4°
625 Hz		0.00%	11.4°
650 Hz	(h13) :	0.11%	264.0°
675 Hz		0.00%	11.4°
700 Hz	(h14) :	0.00%	11.5°
725 Hz		0.00%	11.5°
750 Hz	(h15) :	0.46%	261.4°
775 Hz		0.00%	11.7°
800 Hz	(h16) :	0.00%	11.7°
825 Hz		0.00%	11.8°
850 Hz	(h17) :	1.64%	259.0°

Fig 5.6 Current THD analysis

5.5 Cascaded 5 level multilevel inverter model

Since then, the CMI has been utilized in a wide range of applications. The CMI shows superiority in high-power applications, especially shunt and series coupled FACTS controllers. The CMI produce its output almost sinusoidal

voltage waveforms by combining many cut off voltage levels. By addition of more H-bridge converters, the amount of Var can simply bigger without redesign the power stage, and build-in redundancy against shelf H-bridge converter failure can be realized. A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters,[14][15] which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing., The converter topology is based on the series connection of single-phase inverters with separate dc sources Fig.5.7 shows the Simulink model for five-level cascaded inverter. The resulting output ac voltage swings from $-2V_{dc}$ to $+2V_{dc}$ with five-level. The staircase waveform is nearly sinusoidal, even without filtering.[14]

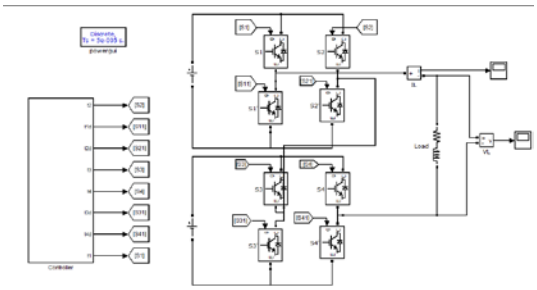


Fig 5.7 Simulink model for five-level cascaded inverter

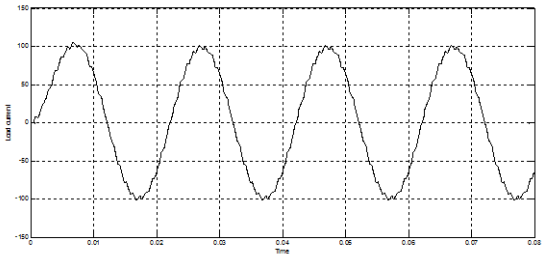


Fig 5.8 Load current waveform

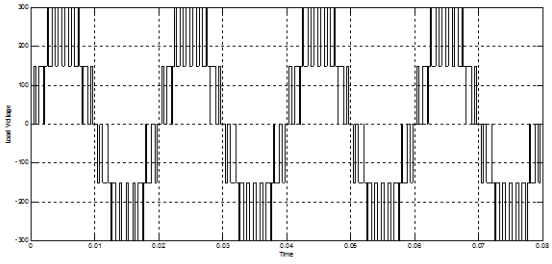
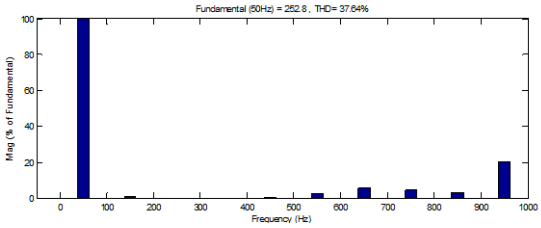


Fig 5.9 Load voltage waveform

5.6 Load voltage THD analysis

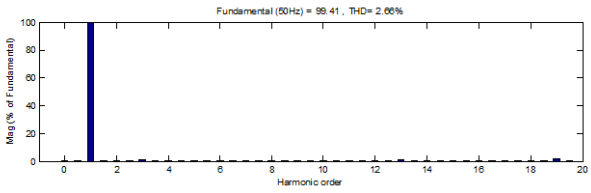


Total Harmonic Distortion (THD) = 37.64%

0 Hz	(DC):	0.00%	270.0°
50 Hz	(Fnd):	100.00%	0.0°
100 Hz	(h2):	0.00%	213.8°
150 Hz	(h3):	1.12%	0.0°
200 Hz	(h4):	0.00%	199.4°
250 Hz	(h5):	0.20%	0.0°
300 Hz	(h6):	0.00%	194.6°
350 Hz	(h7):	0.02%	0.0°
400 Hz	(h8):	0.00%	192.7°
450 Hz	(h9):	0.68%	171.9°
500 Hz	(h10):	0.00%	191.7°
550 Hz	(h11):	2.75%	0.0°
600 Hz	(h12):	0.00%	191.4°
650 Hz	(h13):	5.88%	0.0°
700 Hz	(h14):	0.00%	191.7°
750 Hz	(h15):	4.74%	0.0°
800 Hz	(h16):	0.00%	191.7°
850 Hz	(h17):	3.27%	0.0°
900 Hz	(h18):	0.00%	191.0°
950 Hz	(h19):	20.21%	0.0°

Fig 5.10 Load voltage THD analysis.

5.7 Load current THD analysis



Total Harmonic Distortion (THD) = 2.66%

0 Hz	(DC):	0.00%	90.0°
50 Hz	(Fnd):	100.00%	0.0°
100 Hz	(h2):	0.00%	33.4°
150 Hz	(h3):	0.56%	0.0°
200 Hz	(h4):	0.00%	19.5°
250 Hz	(h5):	0.06%	0.0°
300 Hz	(h6):	0.00%	14.7°
350 Hz	(h7):	0.00%	0.0°
400 Hz	(h8):	0.00%	12.6°
450 Hz	(h9):	0.12%	89.6°
500 Hz	(h10):	0.00%	11.8°
550 Hz	(h11):	0.40%	266.8°
600 Hz	(h12):	0.00%	11.5°
650 Hz	(h13):	0.73%	263.9°
700 Hz	(h14):	0.00%	11.5°
750 Hz	(h15):	0.51%	261.4°
800 Hz	(h16):	0.00%	11.7°
850 Hz	(h17):	0.31%	259.0°
900 Hz	(h18):	0.00%	12.1°
950 Hz	(h19):	1.71%	256.7°

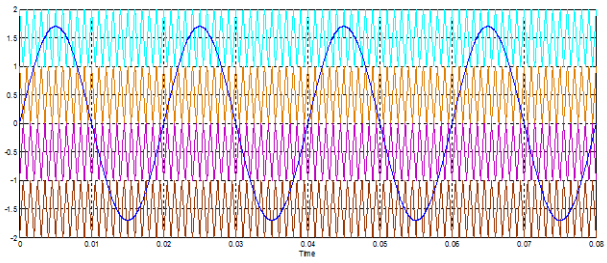


Fig 5.11 Load current THD analysis and current waveform

5.8 OTCHB model and output waveform.

The simulink model and output wave form shown below.This model is compared with above two model for THD analysis.

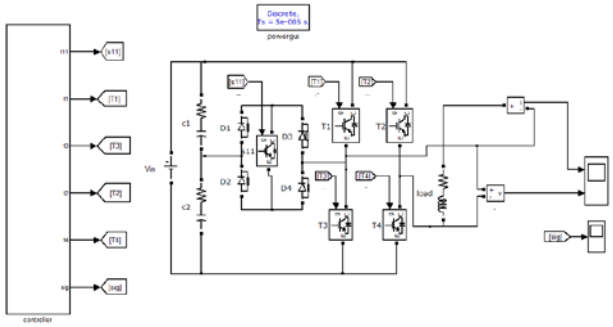


Fig 5.12 Simulink model for OTCHB inverter

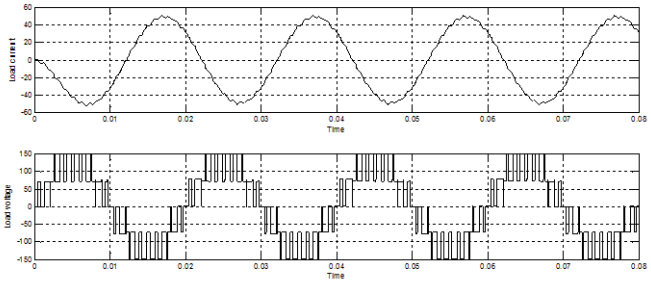


Fig 5.13 Load current and load voltage waveform of OTCHB model

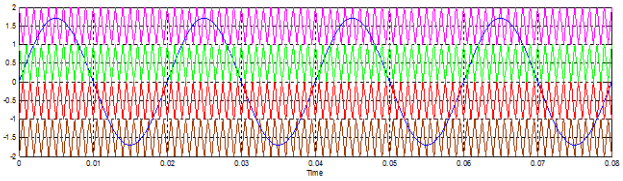
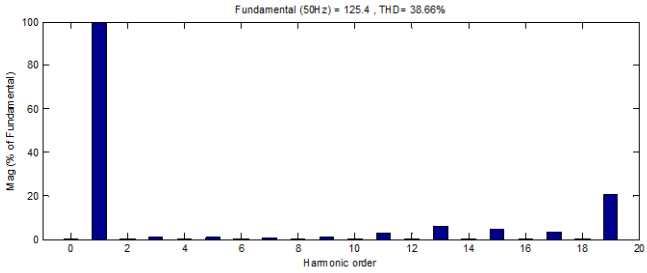


Fig 5.14 Carrier waveform and signal waveform of OTCHB

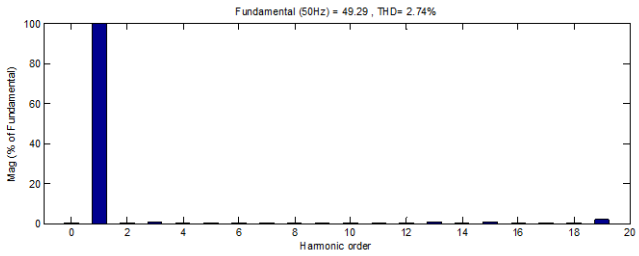
5.9 Voltage THD analysis



Total Harmonic Distortion (THD) = 38.66%

0 Hz	(DC):	0.12%	270.0°
50 Hz	(Fnd):	100.00%	0.0°
100 Hz	(h2):	0.07%	171.9°
150 Hz	(h3):	1.06%	10.5°
200 Hz	(h4):	0.10%	82.3°
250 Hz	(h5):	0.80%	0.0°
300 Hz	(h6):	0.01%	97.8°
350 Hz	(h7):	0.49%	0.0°
400 Hz	(h8):	0.02%	41.5°
450 Hz	(h9):	0.95%	177.7°
500 Hz	(h10):	0.00%	221.0°
550 Hz	(h11):	2.66%	0.0°
600 Hz	(h12):	0.04%	0.0°
650 Hz	(h13):	6.06%	0.0°
700 Hz	(h14):	0.09%	0.0°
750 Hz	(h15):	4.79%	0.0°
800 Hz	(h16):	0.04%	94.2°
850 Hz	(h17):	3.25%	0.0°
900 Hz	(h18):	0.11%	117.5°
950 Hz	(h19):	20.78%	0.0°

Fig. 5.15 Load voltage THD analysis of OTCHB



Total Harmonic Distortion (THD) = 2.74%

0 Hz	(DC):	0.17%	90.0°
50 Hz	(Fnd):	100.00%	141.6°
100 Hz	(h2):	0.05%	0.0°
150 Hz	(h3):	0.53%	122.1°
200 Hz	(h4):	0.03%	186.4°
250 Hz	(h5):	0.26%	64.0°
300 Hz	(h6):	0.00%	9.7°
350 Hz	(h7):	0.12%	16.1°
400 Hz	(h8):	0.00%	54.6°
450 Hz	(h9):	0.17%	0.0°
500 Hz	(h10):	0.00%	5.8°
550 Hz	(h11):	0.39%	92.9°
600 Hz	(h12):	0.01%	19.1°
650 Hz	(h13):	0.75%	86.7°
700 Hz	(h14):	0.01%	14.3°
750 Hz	(h15):	0.51%	80.4°
800 Hz	(h16):	0.00%	181.0°
850 Hz	(h17):	0.31%	70.9°
900 Hz	(h18):	0.01%	217.7°
950 Hz	(h19):	1.75%	75.5°

Fig 5.16 current THD analysis waveform

Table 1 Comparison of harmonics in multilevel inverter

S.No.	Type of inverter	THD harmonics (%)
1	Normal inverter	70.99
2	Cascaded 5 level multilevel inverter	37.64
3	OTCHB model proposed 5-level inverter	2.74

It can be seen from the Table 2 that with the use of normal inverter, there is a decrease in the %THD level to 70.99%. Further with the use of Cascaded 5 level multilevel inverter and %THD level 37.64% , respectively. While using the proposed model(OTCHB model proposed 5-level inverter) the % THD level is decrease to 2.74%. This shows an improved performance of the cascaded H-bridge5-level inverter.

VI. CONCLUSION

H – bridge 5-level multilevel inverter has been simulated with reduced harmonics and implemented. Finally the harmonics in multilevel inverter at different stages are compared. From that comparison, it is seen that the OCTHB 5-level inverter has least value of THD. The simulation results are shown in section 5 with the prediction. The experimental results closely agree with the simulation results.

VII. FUTURE SCOPES

This work use in upcoming a novel current multilevel (CML) inverter topology, named boost CML inverter, and its application on energy dealing out of single-phase grid-connected photovoltaic systems. The major using the CML technique are balanced current sharing among semiconductor switches and the decrease of the current slope in the circuit devices, with a following reduction of conducted and radiate electromagnetic interference. The CML technique also allows minimizing current waveforms harmonic content. System description, mathematical advance, and design strategy ,the proposed concepts, experimental measurements, can made in a small-scale laboratory and result can be find results data the possibility of the application of this new topology on single-phase grid-connected PV systems.

There is a tough demand to push voltage-source inverters into distribution voltage level, which is between 11kv–16 kV, or typically 13.8 kV. , the power electronics for distribution and transmission voltage levels are mainly conquered by current source converters, with reverse voltage blocking capability.

As power level increased with new devices, the multilevel inverter power-handling capability is also proportionally increased. The application to the distribution voltage level can be achieved with less than five levels when the mentioned high-voltage 11 kv,33kv range materials are used.

REFERENCES

[1] Krishna Kumar Gupta, Shailendra Jain ,,Maulana Azad National Institute of Technology Bhopal, India, "A NOVEL UNIVERSAL CONTROL SCHEME FOR MULTILEVEL INVERTERS", IEEE 2011.

[2] José Rodríguez, Jih-Sheng Lai " Multilevel Inverters: A survey of Topologies Control signal and Applications" IEEE, vol. 49, no. 4, 2002

[3] Alireza Nami, Firuz Zare, Frede Blaabjerg, "A HYBRID CASCADE CONVERTER TOPOLOGY WITH SERIES-CONNECTED SYMMETRICAL AND ASYMMETRICAL DIODE-CLAMPED H-BRIDGE CELLS", IEEE, vol. 26, no. 1, 2011 .

[4] J. Dagan, Raul Rabinovici and Dmitry Baimel, "An Analytical Approach to Total Harmonic Distortion Reduction in Multi-Level Inverters" 2010 IEEE Convention of Electrical and Electronics Engineers in Israel.

[5] Divya Subramanian, Rasheed, "Five Level Cascaded H-Bridge Multilevel Inverter Using Multicarrier Pulse Width Modulation Technique" (IJEIT) Volume 3, Issue 1, July 2013, ISSN: 2277-3754

[6] MURUGESAN.G, Dr.Rangaragan, JAGABAR SATHIK.M, PRAVEEN.M,"a new multilevel inverter topology using less number of switches" ISSN : 0975-5462 Vol. 3 No. year 2011.

[7] Nasrudin A. Rahim, Senior Member, IEEE, and Jeyraj Selva "Multistring Five-Level Inverter With Novel PWM Control Scheme for PV Application raj" IEEE transactions on industrial electronics, vol. 57, no. 6, june 2010 2011.

[8] Arif Al-Judi, Hussain Bierk and Ed Nowicki, Member, IEEE "Selective Harmonic Power Optimization in Multilevel Inverter Output" 978-1-61284-247-9/11,2011 IEEE.

[9] T.Prathiba, P.Renuga, "A comparative study of Total Harmonic Distortion in Multi level inverter topologies "Journal of Information Engineering and Applications www.iiste.org ISSN 2225-0506 Vol 2, No.3, 2012.

[10] Ayşe KOCALMIŞ, Sedat SÜNTER "modeling and simulation of a multilevel inverter using space vector modulation technique" year 2009.

[11] Ilhami Colak, Ramazan Bayindir and Seref Sagiroglu "The Design and Analysis of a 5-Level Cascaded Voltage Source Inverter with Low THD" 2009 IEEE.

[12] Optimization H. Taghizadeh , M. Tarafdar Hagh, "Harmonic elimination of Cascade Multilevel Inverters with Non equal

DC Sources Using Particle Swarm Optimization" IEEE, vol. 57, no. 11, 2010

[13] Suroso and Toshihiko Noguchi " New H-Bridge Multilevel Current-Source PWM Inverter with Reduced Switching Device Count" The 2010 International Power Electronics Conference.

[14] Ivo Pereira, António Martins, Dr Roberto Frias "Multicarrier and Space Vector Modulation for Three-Phase NPC Converters" 2009.

[15] Mohamed S. A. Dahidah, Vassilios G. Agelidis "Selective Harmonic Elimination PWM Control for Cascaded Multilevel Voltage Source Converters" IEEE transactions on power electronics, vol. 23, no. 4,2008