Low Power 4/5 Counter Using Dual Dynamic Node Pulsed Hybrid Flip-Flop

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Abstract - Designing a new dual dynamic node hybrid flip-flop (DDFF) and low power 4/5 Counter was based on DDFF. The proposed designs eliminate the large capacitance present in the precharge node by following a split dynamic node structure to separately drive the output pull-up and pull down transistors. The DDFF offers a power reduction of up to 62% and 48% compared to the conventional flip-flops like Power PC 603 flip-flop and semi dynamic flip-flop. The aim of the DDFF-ELM is to reduce pipeline overhead. It presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. The performance comparisons made in a 90 nm UMC process show a power reduction of 48% compared to the Semi dynamic flip-flop, with no degradation in speed performance. The leakage power and delay variations of various designs are compared with the proposed designs. The Footed logic is used to reduce power in the circuits. An efficient power reduction was obtained using footed logic.

Keywords: Low power, Leakage current, Dual Dynamic Flip Flop, high speed, Footed logic.

I. INTRODUCTION

In the world of modern communication, a frequency synthesizer with a high frequency prescaler is an important building block. New techniques offering higher integration density, lower power consumption, and high-speed capability are developed to achieve a high-speed CMOS prescaler. Some circuits, using advanced processes and/or special circuit techniques, are proposed to realize the high-speed dual-modulus prescalers. Among them, the true single phase circuit technique has resulted in many complex CMOS circuits operating at clock frequencies of several hundred MHz , and some CMOS circuits operating at > 1 GHz in the last few years. A new architecture of a dual-modulus prescaler is presented and fabricated with 0 . 6 CM OS technology.Power consumption plays major roll in Integrated circuits of VLSI design. In synchronous systems, high speed has been achieved using advanced pipelining techniques. In modern deep-pipelined architectures, pushing the speed further up demands a lower pipeline overhead.

II. SYSTEM MODEL

Dual Dynamic Flip-Flop (DDFF)

In DDFF architecture Node X1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture nodeX2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases:

1) The evaluation phase, when CLK is high, and

2) The precharge phase, when CLK is low.

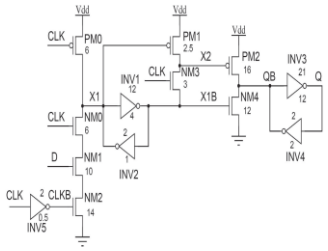

Fig. 2.1 Dual Dynamic Flip Flop

Evalution Phase

- When Clk=1 and D=1, x1 discharged , it switches the INV1-2 (pair) and X1B=1 & QB discharge QB=0&Q=1.
- X1=0 will maintain throughout the evaluation phase.
- Clk=0->1 and D=0 X1=1 X2=0, QB=1 &Q=0.

Precharge Phase

- CLK =0 and D=1 X1=1 it switches the state of INV1-2 and X2 is in inactive state. It stores the charge dynamically.
- QB maintain previous state QB=0 and Q=1.

- CLK =0, D=0 it will remain previous state Q=0 and QB=1.

I. PREVIOUS WORK

Semi Dynamic Flip Flop (SDFF)

Semi dynamic flip flop is fastest classic hybrid structure. They are purely dynamic designs as well as pseudo dynamic design, which has an internal precharge structure and static output. Dynamic frontend and static output.

Disadvantages

- Redundant data transitions,
- Not efficient for power consumption because of large clock and large precharge capacitance,
- High power consumption devices,
- Area is also high.

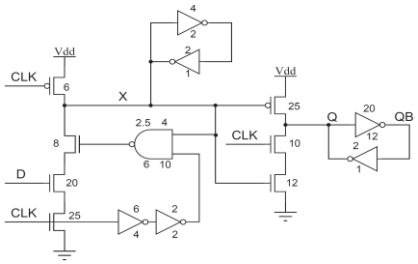

Fig. 3.1 Semi Dynamic Flip Flop

Power PC 603 Flip Flop

PowerPC 603 is one of the most efficient classic static structures. The PowerPC 603 was based on master slave latch. They dissipate comparatively lower power and have a low clock-to-output (CLK-Q) delay. In a synchronous system, the delay overhead associated with the latching elements is expressed by the data to output (D-Q) delay rather than CLK-Q delay. It has advantages of having low power keeper structure and low latency direct path. Disadvantage of large data to output delay during large setup time.

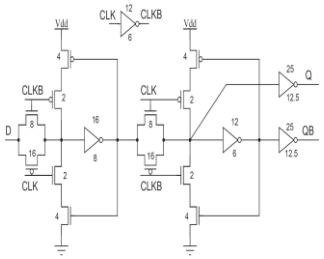

Fig. 3.2 Power PC 603 Flip Flop

Cross Charge Control Flip Flop (XCFF)

A low power and high-speed flip-flop named Cross Charge control Flip-Flop (XCFF). It has two dynamic nodes driving output transistors separately. The minimum power-delay product of the XCFF is 48% smaller than that of CMOS flip flop and 20% smaller than that of the semi dynamic Flip-Flop (SDFF). Charge sharing is uncontrollable when complex functions are embedded is the disadvantage.

Conditional Data Mapping Flip Flop (CDMFF)

A new family of low power and high-performance flip flops, namely conditional data mapping flip flops (CDMFFs), which reduce their dynamic power by mapping their inputs to a configuration that eliminates redundant internal transitions.The conditional data mapping flip flop (CDMFF) is one of the most efficient which uses an output feedback structure to conditionally feed the data to the flip flop. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted.

II. PROPOSED METHODOLOGY

Footed Logic

An NMOS transistor is introduced in the circuit whose gate is shorted with its drain and connected to the source of the NMOS (before) clock transistor.

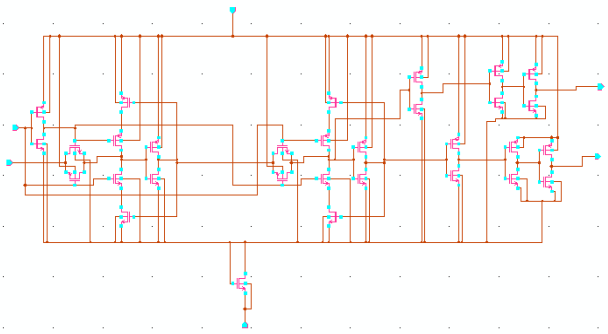

Fig.4.1 Schematic Diagram of PowerPC 603 Flip Flop with footed

The source of NMOS transistor is connected to gate. When input is low then dynamic node is always high and output is kept low regardless of operating phase.

Power PC Flip Flop with Footed logic

Dual Dynamic Flip Flop with Footed Logic

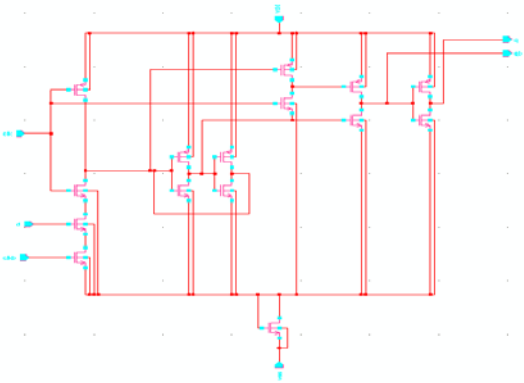

Fig.4.2 Schematic Diagram of Dual Dynamic Flip Flop with footed

III. SIMULATION/EXPERIMENTAL RESULTS

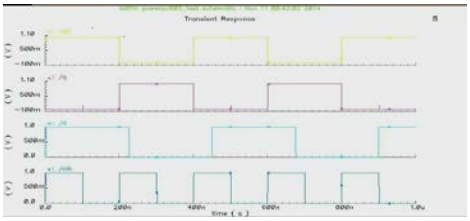

Fig.5.1 Output Waveform of PowerPC Flip Flop with Footed logic

The clk and d which are the input signal and q&qb are considered as output signals.The output was based on D flip flop so when 1 is given as input to d then 0 as getting output for q and qb as inverted output of 1.

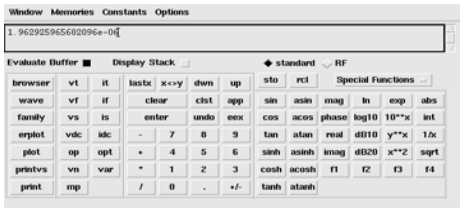

Fig.5.2 Power of PowerPC Flip Flop with Footed logic

The overall power in footed logic is reduced upto 63% when compared with power pc flip flop.

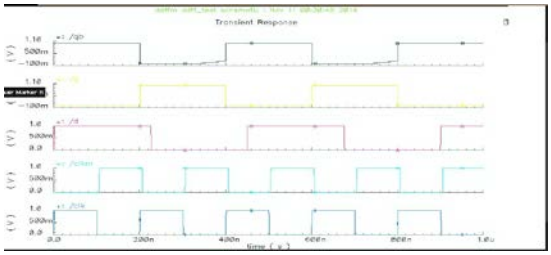

Fig.5.3 Output Waveform of Proposed Dual Dynamic Flip Flop with Footed logic

The clk, clkm and d which are the input signal and q&qb are considered as output signals.The output was based on D flip-flop so when clk is given as 1 input the clkb is consider with the inverted input as 0 and then for d flip flop when 1 is given as input then 0 as getting output for q and qb as inverted output of 1.

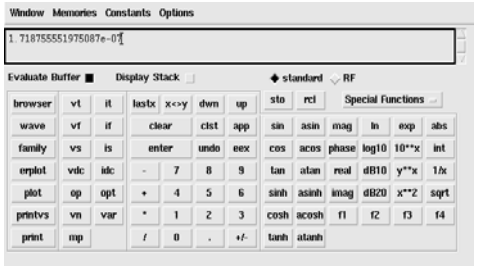

Fig.5.4 Power of Proposed Dual Dynamic Flip Flop with Footed logic

The overall power in footed logic is reduced upto 82% when compared with dual dynamic flip flop.

Table 1. Comparison of Power Performance

Flip Flop	Number of transistor	Total power(µw)	Total Power using Footed logic(µw)
Power PC 603	22	81.59	1.96
DDFF	18	3.31	0.718

IV. CONCLUSION

A new low power DDFF and power pc flip flop is designed using footed logic. The proposed DDFF eliminates the redundant power dissipation present in the XCFF.A comparison of the proposed flip-flop with the conventional flip flops with Footed logic showed that it exhibits lower power dissipation along with comparable speed performances. The diode footed domino circuit design style and demonstrated that the technique is leakage-tolerant, achieves high-performance and low power compared to the conventional domino styles, and is suitable for scaled CMOS

technologies. Power is reduced using low power techniques such as FOOTED DIODE and MTCMOS.

V. FUTURE SCOPES

A low power 4by5 counter is going to design by using this Footed logic technique and with the help of proposed DDFF. The counter design consists of one 2*1 MUX, one 2input NAND gates, one 2input NOR gate and three dual dynamic flip flop.

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