Design and verification of an FPGA based Bit-Error-Rate-Tester in Wireless Systems

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Abstract: ***The bit error ratio (also BER) is the number of bit errors divided by the total number of transferred bits during a time duration. The proposed BER tester (BERT) integrates fundamental baseband signal processing modules of a typical wireless communication system along with a realistic fading channel simulator and an accurate Gaussian noise generator onto a single FPGA to provide an accelerated and repeatable test environment. The error rate performance of single- and multiple-antenna systems over a wide range of parameters can be rapidly evaluated by using a developed graphical user interface. The FPGA-based Bit Error Rate should reduce the need for time-consuming software based simulations, hence increases the productivity. The BERT modules were developed using device-independent HDL, and no specific features of the FPGAs, such as processors, were utilized. Therefore, the system is portable and can easily be synthesized onto larger and faster new FPGAs for the rapid prototyping of increasingly complex emerging wireless communication systems. FPGA offer significant cost reduction compared to commercially available solutions.***

Keywords: Bit-error rate tester (BERT), field-programmable gate array (FPGA), fading channel simulation, Gaussian noise.

I. INTRODUCTION

Free space wireless networks capacity has been continuously growing in the last twenty years as worldwide research efforts have been directed towards understanding the various wireless impairments for performance. However, much lower attention has been devoted to the performance monitoring of the signals, since it becomes critical for the designer to test all the layers of a network at the final stage. Now a days world moving towards on fourth generation of wireless The pace of wireless system development using the latest communication techniques is increasingly limited by the design productivity. To accurately estimate the BER performance of a communication system over a time-varying fading channels. The error performance needs to be averaged not only on independent instances of noise and data, but also on the fading channel samples over a long period. This performance evaluation can require several weeks or months of software simulations. Simulation of digital communication systems under additive white Gaussian noise (AWGN) channels is straightforward as the system performance is averaged over a large number of independent instances of noise and data, The BER performance measurement of wireless systems over time-varying fading channels requires significantly longer simulation times because of the dependence between the channel instances. Hardware simulators can accelerate the performance evaluation of communication systems compared with software simulators by several orders of magnitudes. This makes hardware-accelerated prototyping and validation of the PHY layer as an increasingly attractive alternative. While using system level tools can eliminate the need for extensive hardware knowledge and will usually shorten the design time, a simulation library may include only a set of basic digital communication components and might not include modules, such as new coding algorithms.. Thus, designers will still need to implement various communication modules with compatible interfaces with other components. Most of the published BER testers (BERTs) verify the performance under the linear AWGN channel which is a rather inadequate model for wireless mobile communication systems. Fading channel models for mobile communication systems must reproduce the statistical properties of radio propagation environments.

II. SYSTEM MODEL

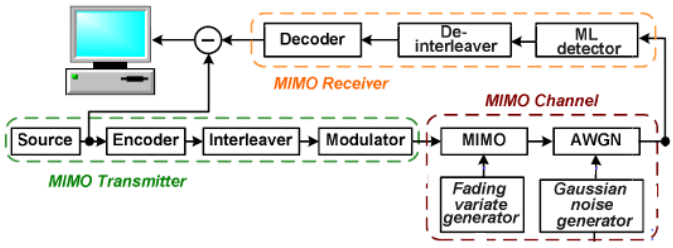

Fig 2.1 BERT System

To generate BER versus SNR characteristics using simulation method. To discuss our methodology, we developed a FPGA based BERT for wireless systems. A source encoder generates a sequence of random bits. The generated bit stream is then passed through various processing modules at the transmitter, then transmit by the radio channel and noise added by the AWGN channel. It is

important to note the BER performance measurements need to be averaged not only over independent instances of AWGN samples and transmitted bit samples, but also over the fading channel samples. A sequence of baseband signal modules at the receiver recovers the transmitted bits from the noisy received symbols bits. Therefore, to accurately estimate the BER performance of a wireless communication system over a time-varying fading channel, a large number of random bits. Typically, the fading channel response changes slower than the data signal. Channel coding is applied to the data bits to improve system performance and robustness in the presence of channel impairments Therefore, the effects of a deep fade can last over a relatively long sequence of data samples, which can result in a burst of errors. In the MIMO transmitter block. Also source bits, generated by a Pseudo Random Noise Generator, are encoded using an extended binary code, interleaved with a interleaver, and modulated using 4-quadrature amplitude modulated (QAM) symbols. Interleaving the data samples before transmission causes bursts of errors arising in the channel to be broken up by the de-interleaver in the receiver. The interleaved bits are modulated and passed through the MIMO channel where they are attenuated by the multipath fading and corrupted with AWGN . The resulting isolated bit errors can then be more readily detected and corrected by the error correction decoder. In the receiver, a maximum likelihood (ML) detector estimates the transmitted bit samples. After ML detection, the bit stream is de-interleaved, samples are decoded for the extended Golay code, and compared to the transmitted bit stream.

III. PREVIOUS WORK

[1] “FPGA-Based Bit Error Rate Performance Measurement of Wireless Systems” by A. Alimohammad, S. F. Fard Proc. IEEE , vol. 22,issue 7 july 2014

This paper presents the bit error rate (BER) performance of digital baseband communication systems on a field-programmable gate array (FPGA). The proposed BER tester (BERT) integrates fundamental baseband signal processing modules of a typical wireless communication system along with a realistic fading channel simulator and an accurate Gaussian noise generator onto a single FPGA to provide an accelerated and repeatable test environment in a laboratory setting. Also Using a developed graphical user interface (GUI), the error rate performance of single- and multiple-antenna systems over a wide range of parameters can be evaluated. The FPGA-based BERT should reduce the need for time-consuming software based simulations, hence increases the productivity. This FPGA-based solution is more cost effective than conventional performance measurements made using expensive commercially available test equipment and channel simulators.

[2]“Hardware-based error rate testing of digital baseband communication systems” by A. Alimohammad, S. F. Fard in the year 2008.

Here present a flexible architecture for calculating the bit-error-rate (BER) performance of digital baseband communication systems. The BER tester uses an accurate fading channel model and a Gaussian noise generator to provide a realistic and repeatable test environment in the laboratory. Using an efficient elastic buffer interface, baseband module can be added to the cascaded architecture of a digital baseband communication system. An independent of the module's operating rate and its position in the cascade structure, and its latency. This evaluation environment should reduce the need for time consuming field tests in laboratory, hence reducing the time-to market and increasing productivity.

IV. PROPOSED METHODOLOGY

Software used:

1) Xilinx® ISE® Design Suite 13

2) Matlab 10

We used MATLAB Software for implementation of the system. The flexibility in the software we can changes in the system as per specification changes.

The flow of our implementation is described following algorithm

Algorithm:

A) Transmitter
   1. Generate message string of 1’s and 0’s.
   2. Interleave the above message string.
   3. Convert the serial string into parallel blocks equal to no. of carriers.
   4. Apply 16-qam modulation on each block of data.

B) Receiver.
   1. Apply 16-qam De-modulation.
   2. Convert the parallel blocks into serial string.
   3. De-Interleave the above message string.

C) Error Analysis

BER vSNR

1. Add AWGN with different SNR values in transmitted signal at low multipath effect (0.1 and 0.05)
2. Compare original and received message string to find error ration.
3. Plot graph of BER vs SNR at Low multipath effect.
4. Apply same process for high Multipath effect= 0.5 and 0.4
5. Plot graph of BER vs SNR at High multipath effect.

V. SIMULATION/EXPERIMENTAL RESULTS

Simulation :

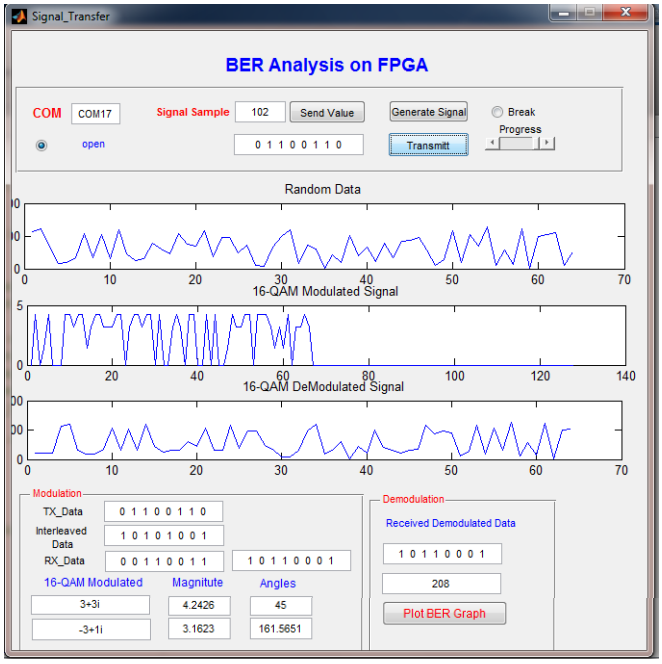

Fig 5.1 BER analysis on FPGA

Device utilization summary:

Selected Device : 3s50atq144-4
Number of Slices: 92 out of 704 13%
Number of Slice Flip Flops: 96 out of 1408 6%
Number of 4 input LUTs: 166 out of 1408 11%
Number used as logic: 158
Number used as Shift registers: 8
Number of IOs: 13
Number of bonded IOBs: 13 out of 108 12%
Number of GCLKs: 2 out of 24 8%

BER vs SNR Graph:

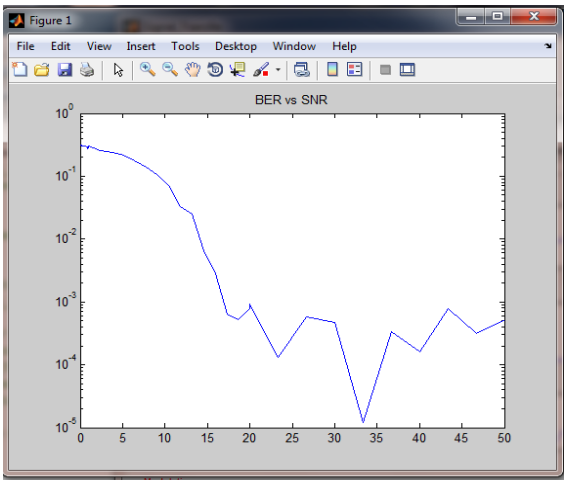

Fig 5.2. BER performance of a 2×2 coded MIMO system measured using the FPGA-based BERT

To estimate each BER point at each SNR, we measured the performance of signal transmission on the hardware platform. We can verify that the hardware generated BER results accurately match the computer generated BER performance.

VI. CONCLUSION

An FPGA-based Bit Error Rate performance testing scheme is introduced. The scheme can measure the BER performance of a wide range of digital communication systems. To achieve BER of 0.001 we require 14 to 15 dB SNR. Compared with traditional standalone BERT and ATE equipment, the proposed solution is much cheaper. Compared with traditional software simulations, the proposed BER testing scheme is a few orders of magnitude faster. It is also easy to set up for BER testing under different noise conditions as a novel implementation of an AWGN communication channel emulator is included in this scheme. In addition, FPGA-based solution makes it easy to interface.

VII. FUTURE SCOPES

One can note that the DUT of the BER testing system must be the combination of an encoder and a decoder, or the combination of a modulator and a demodulator. If we want to test the performance of a decoder, a reference module (e.g. an encoder) needs to be added in the testing setup. It would be more convenient to test the BER performance of a receiver using the IP cores if a parameterized reference encoder and/or modulator can be included in the testing scheme.

In addition, as BER and jitter are closely related, jitter testing and jitter separation schemes can be devised based on BER

testing schemes .Jitter testing is a94 very challenging issue and its importance has been widely recognized as the transmission speed is becoming higher and higher. The proposed BERT core and the AWGN core can be used as a good start point for jitter testing research. With the continuing enhancement of FPGA performance, it is possible to build a jitter testing scheme in a single FPGA, especially in a SoC or DSP oriented FPGA device.

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