Delay Reduction Caused by on State Resistance of Power MOSFET using Elmore Model

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Abstract:- This thesis work presents a comprehensive study of parasitic elements on the MOSFET switching performance. To evaluate the MOSFET switching characteristics, a circuit-level analytical model has been considered that takes MOSFET parasitic capacitances, p-n junctions, resistances, and reverses current of the diode. This work we analyze the parametric estimation for MOSFET switching delay, leakage current reduction over to the parasitic devices. One solution to the problem of ever-increasing leakage is to force a non-stack device to a stack of two devices without affecting the input load. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. Due to stacking of the devices, the drive current of a forced-stack gate will be lowered results in a increased delay. Using stack transistors, here we designed a full adder logic circuit.

Keyword- MOSFET, parasitic elements, switching characteristics.

I. INTRODUCTION

Discrete power MOSFETs employ semiconductor processing techniques that are similar to those of today's Very Large Scale Integration circuits, although the geometry of device, voltage and current levels are significantly different from the design used in VLSI devices. The MOSFET is based on the original field-effect transistor introduced in the 70s. Figure 1.1 shows the device schematic for a MOSFET. The invention of the power MOSFET was partially driven by the restrictions of bipolar power junction transistors that till recently, was the device of choice in power electronics applications. Although it is impossible to outline fully the operative boundaries of a power device we will loosely confer power device as any device which will switch a minimum of 1A. The bipolar power transistor is a current controlled device. A large base drive current as high as $1/5^{th}$ of the collector current is needed to stay the device in the ON state.

Also, higher reverse base drive currents are needed to get fast turn-off. Despite the high advanced state of manufacturability and lower prices of BJTs, these limitations of BJT's have created the base drive circuit design more complex and hence more costly than the power MOSFET.

Another limitation of BJT is that both electrons and holes contribute to conduction. Hole's presence with their higher carrier lifetime causes the switching speed to be many orders of magnitude slower than for a power MOSFET of same size and voltage rating. On the other hand, Power MOSFETs are majority carrier devices with the no minority carriers injection. They are superior to the BJTs in high frequency applications where switching power losses are vital. Also they can withstand simultaneous application of high voltage and current without undergoing destructive failure because of second breakdown.

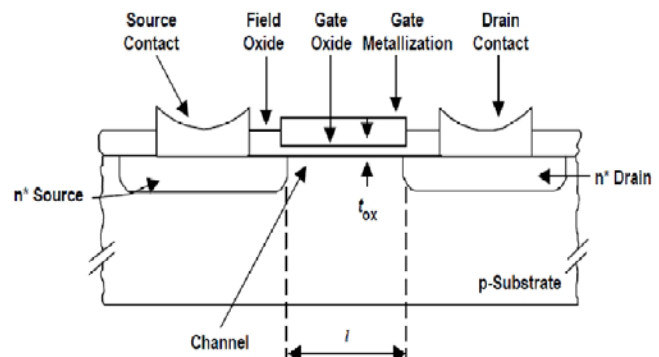

fig 1.1 MOSFET Device.[16]

Power MOSFETs can also be connected in parallel easily because with increase in temperature the forward voltage drop increases, ensuring an even distribution of current among the all components. However, at high breakdown voltages the on-state voltage drop of the power MOSFET becomes higher than that of a similar size bipolar device with similar voltage rating. This makes it more attractive to use the bipolar power transistor at the expense of worse high frequency performance.

Figure 1.1 shows schematic diagram and Figure1.2 shows the physical origin of the parasitic components in an n-channel power MOSFET. With increasing drain voltage, the parasitic JFET appears between the two body implants restricts current flow when the depletion widths of the two adjacent body diodes extended into the drift region. The device can become susceptible to unwanted device turn-on and premature breakdown by parasitic BJT. The base

resistance Rb must be minimized through careful design of the doping and distance under the source region. Cgs is the capacitance due to the overlapping of the channel regions and the source by the polysilicon gate and is not dependent of the applied voltage. Cgd consists of two parts, the first part is capacitance associated with the overlapping of the polysilicon gate and the silicon beneath within the JFET region. The second part is the capacitance related to the depletion region immediately under the gate. Cgd is a non-linear function of voltage. Finally, Cds the capacitance related to the body-drift diode, varies reciprocally with the square root of the drain-source bias. [18]

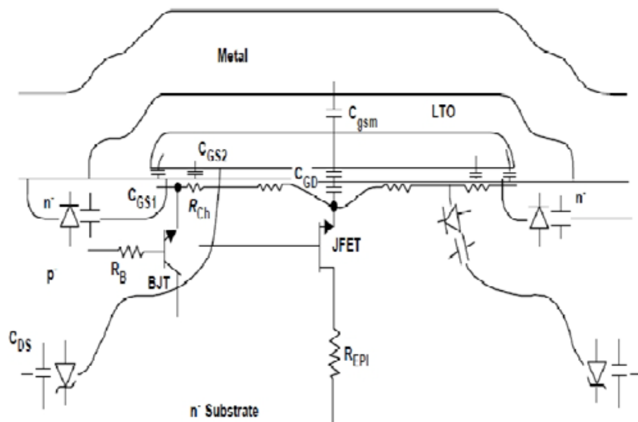

Fig 1.2 MOSFET Parasitic Components.[1]

II. PROBLEM FORMULATION

The reduce in channel length will create non ideal effects such as body effect, channel length modulation effects, oxide breakdown effect, drain punch through effects, hot electron effects, drain-induced barrier lowering, etc In our design we will analyze the performance of long channel device and the reducing the channel size by maintaining the same performance by reducing these non ideal effects. This work we analyze the parametric estimation for MOSFET switching delay, leakage current reduction, power dissipation and variation of temperature effects due to the parasitic devices. One solution to the problem of ever-increasing leakage is to force a non-stack device to a stack of two devices without affecting the input load. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. Logic gates after stack forcing will reduce leakage power, but incur a delay penalty. Due to stacking of the devices, the drive current of a forced-stack gate will be lowered results in a increased delay. Using stack transistors, here we designed a full adder logic circuit.[1]

Also The RC model of an inverter which represents transistor as a resistance and a charging or discharging capacitance. In this paper we will discuss the performance analysis and Delay Estimation on the RC Delay MOSFET model of structure of array decoder. [7]

2.1 Parasitic Resistances:

Parasitic resistance has become a obstacle affecting the performance of the CMOS devices. But, series resistance quantification in the CMOS devices is becoming extremely difficult. channel resistance (Rchannel), series resistance (RSD) is becoming a larger fraction of the total device resistance (RTotal = RSD + Rchannel) and it is limit the performance in advanced devices. We are currently focused on RSD minimization. In the power MOSFET the on-state resistance is made up of various components:

$$R_{DS(on)} = R_{source} + R_{ch} + R_{A} + R_{J} + R_{D} + R_{sub} + R_{wcml}$$

Where;

Rsource is a Source diffusion resistance of MOSFEET
Rch is a Channel resistance of MOSFEET
RA is a Accumulation resistance OF MOSFEET
RJ is a "JFET" component-resistance of the region between the two body region
RD is a Drift region resistance
Rsub is a Substrate resistance
Rwcml is a Sum of Bond Wire resistance.

At high voltages the RDS(on) is dominated by JFET component and epitaxial resistance. At lower voltages RDS(on) is dominated by the channel resistance and contributions of metal to semiconductor contact, bond wires metallization and lead frame. The contribution of substrate becomes more important for lower breakdown voltage device. [7] Most RSD extraction techniques involve RTotal measurements on an array of devices with various gate lengths or, at the very least, a comparison between long- and short-channel devices. These “L-array” extractions all suffer from several disputed assumptions involving the RSD /effective channel length (Leff) dependence, the accuracy of the extracted Leff itself, and the effective mobility (μeff)/Leff dependence. These unresolved experimental discrepancies have led many researchers to pursue alternative RSD extraction methodologies. However, these approaches still involve assumptions leading to significant error. We design a very simple RSD base 4X1 array logic. This design does not require knowledge of Leff , the effective channel width (Weff), oxide capacitance (Cox), or μeff and thus frees it from the most troubling concerns

inherent to the commonly used “Larray” methods. Since these parameters are particularly difficult to quantify in short-channel devices, the proposed extraction procedure is well suited to monitor RSD as channel lengths continue to scale.

The proposed RSD extraction methodology relies on the common linear drain current (ID) expression

$$I_D = \mu_{\text{eff}} C_{\text{OX}} \frac{W_{\text{eff}}}{L_{\text{eff}}} \left(V_G - V_{\text{ON}} - \frac{m}{2} V_D \right) V_D$$

Where

VG - gate bias,

VON - threshold voltage obtained via the linear extrapolation at maximum trans-conductance method, m - body-effect coefficient and VD - drain bias.

First, we simplify further by taking m = 1 and defining Vth as VON + 1/2 VD.

$$I_D = \mu_{\text{eff}} C_{\text{OX}} \frac{W_{\text{eff}}}{L_{\text{eff}}} (V_G - V_{\text{th}}) V_D.$$

Accounting for the source and drain series resistances we can write

$$I_D = \mu_{\text{eff}} C_{\text{OX}} \frac{W_{\text{eff}}}{L_{\text{eff}}} \left(V_G - V_{\text{th}} - \frac{I_D R_{\text{SD}}}{2} \right) (V_D - I_D R_{\text{SD}})$$

where

VG is now the applied gate-to-source terminal bias and

VD is the applied drain-to-source terminal bias.

Now take the ratio of two ID–VG curves recorded at two similar linear drain biases.3.

$$\frac{I_{D1}}{I_{D2}} = \frac{\mu_{\text{eff}} C_{\text{OX}} \frac{W_{\text{eff}}}{L_{\text{eff}}} \left(V_G - V_{\text{th1}} - \frac{I_{D1} R_{\text{SD}}}{2} \right.}{\mu_{\text{eff}} C_{\text{OX}} \frac{W_{\text{eff}}}{L_{\text{eff}}} \left(V_G - V_{\text{th2}} - \frac{I_{D2} R_{\text{SD}}}{2} \right.}$$

$$R_{\text{SD}}^2 \left(\frac{I_{D2} - I_{D1}}{2} \right) + R_{\text{SD}} \left(V_{\text{th2}} - V_{\text{th1}} + \frac{V_{D1} - V_{D2}}{2} \right) - \frac{(V_G - V_{\text{th1}}) I_{D2} V_{D1} - (V_G - V_{\text{th2}}) I_{D1} V_{D2}}{I_{D1} I_{D2}} = 0$$

The advantage of this approach is that these two linear ID–VG measurements are taken on the same device, which allows one to quite reasonably cancel out the most difficult to measure quantities in (μeff , Cox, and Leff).

2.2 RC Model of Inverter:

The Rc model of an inverter which represents transistor as a resistance and a charging or discharging capacitance. The propagation delay of the network excited by the step function is proportional to the time constant of the network. In this case time constant is the product of the resistor and load capacitor. Hence propagation delay for low to high transistor at 50% reach is tPHL =ln2 τ = 0.69 τ = 0.69 Ron CL

where,

Ronn , Ronp are the on resistance of the NMOS and PMOS

Ronp = 1/β(Vgs – Vt)p

Ronn = 1/β(Vgs – Vt)n

Therefore overall propagation delay of the inverter is

tp = (tPHL + tPLH) / 2

=0.69CL { Ronn + Ronp } / 2

When we apply a step input going from 0 to V the transient response of this circuit is exponential function and is given by

Vout (t) = (1-e –t/ τ) V

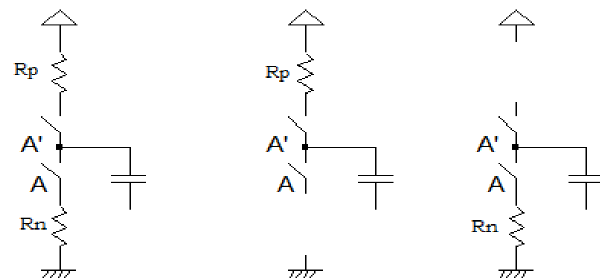

Fig 2.1 RC Model of basic CMOS[17]

2.3 RC Delay model of NAND Gate:

The propagation delay calculation for a CMOS gate is similar to that in static inverter. For the purpose delay analysis each transistor is model as resistor in series with an ideal switch. The value or resistance is depends on the power supply voltage and an equivalent large signal resistance, scale by the ratio of device width over the length.

The propagation delay in complex gate depends on the input pattern e.g. for the NAND input transition of A=0, B=0, A=0, B=1, A=1, B=0 this will turn on the pull up network of

NAND logic gate and the output load capacitor charges towards Vdd. If both inputs are driven high i.e A=1, B=1, the pull down network are on and output load capacitor discharges towards ground. The delay in this case is 0.69 Ron CL/2, since two transistors are in parallel. When only one PMOS transistor turn on i.e. either A or B the delay is called as worst case delay and is given by 0.69 Ron CL. For pull down path the output is discharge only if both A and B switch to logic high and delay in this case is given by 0.69(2Ron CL), since two transistors are in series.

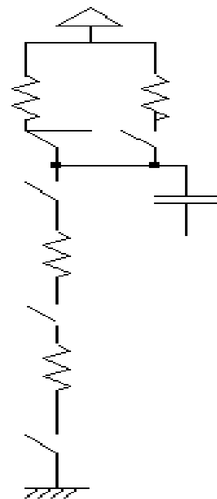

Fig 2.2 RC Model for 2 input NAND logic gate.[17]

Here we have ignore the effects of node capacitance while calculating delay.

tPHL = 0.69(R1C4 + C3 (R1+R2) +C2 (R1+R2+R3) + C1(R1+R2+R3+ R4)

if R1=R2=R3=R4 =RN , tPHL = 0.69RN (C4 +2C3+ 3C2+ 4C1)

A simple RC model provides a very rough approximation of the actual transient behaviour of the digital gates. The accuracy of simple model can be improved significantly by dividing R and C in segments. To Calculate delay between the nodes the Elmore delay model is used. [17]

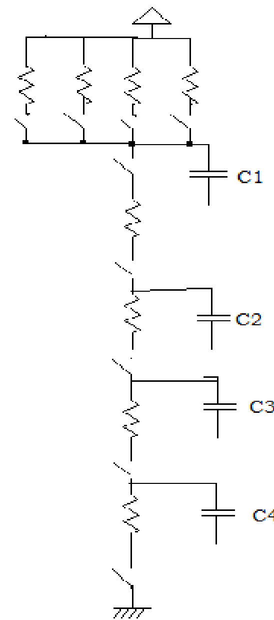

Fig 2.3 RC Model for 4 input NAND logic gate.[17]

The important points of the network are

1) There are no resistor loop in the circuit.

2) All of the capacitor in an RC tree are connected between a node and the ground.

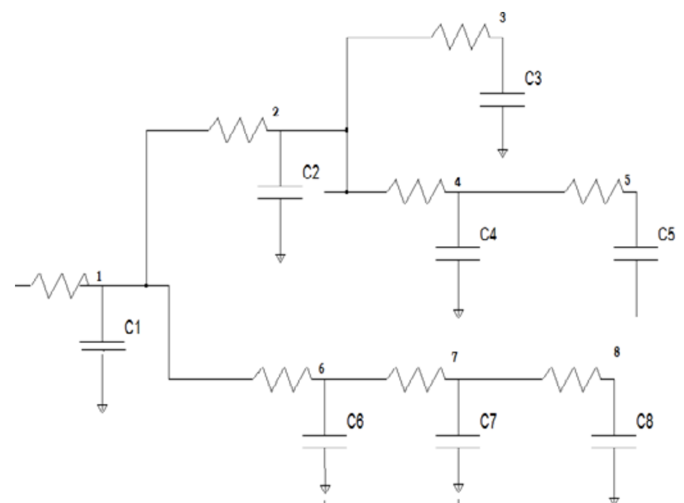

Fig 3.5 Elmore delay model [17]

3) There is no input node in the circuit.

tdp7=C1R1+C2R1+C3R1+C4R1+C5R1+C6(R1+R6)+C7(R 1+R6+R7)+C8 (R1+R6+R7+R8)

Pi denotes the unique path from input node to node I =1,2,3,----N.

In order to get equal rise and fall time the resistance of NMOS and PMOS transistor should be matched. To achieve this the width of PMOS transistor should be increase to have equal Rn and Rp. But this does not reduce the propagation delay of the gate. To get minimum propagation delay the NMOS and PMOS transistor should be size properly for minimum NMOS PMOS ratio.

In CMOS having identical transistors, the load capacitance of the inverter can be divided into an intrinsic and extrinsic component. i.e Cl= Cint + Cext.

Where,

Cint = represents the intrinsic load capacitance of the inverter and is associated with the diffusion capacitances of NMOS and PMOS transistor as well as the gate drain capacitances

Cext represents the equivalent capacitance due to fan-out and wiring capacitances.

tp = 0.69 Ron (Cint + Cext)

= 0.69 Ron Cint (1 + Cext/Cint)

= tpo (1 + Cext/Cint)

Where,

tpo = is intrinsic delay of unloaded gate.

III. DESIGN AND IMPLEMENTATION

This thesis work is focused on following points:

1. Leakage current reduction causes due to sub-threshold conduction in parasitic pn junction. For this we used stack technique. In this we force a on stack device to a stack of two devices without affecting the input load.

2. Delay reduction caused by on state resistance of power MOSFET. For this we used Elmore model

4. Description of previous Test Circuit:

IV. FULL ADDER

A full adder circuit is an arithmetic circuit block that can be used to add three bits to produce a SUM and a CARRY output. Such a building block becomes a necessity when it comes to adding binary numbers with a large number of bits. The full adder circuit overcomes the limitation of the half-adder, which can be used to add two bits only. Let us recall the procedure for adding larger binary numbers. We begin with the addition of LSBs of the two numbers. We record the sum under the LSB column and take the carry, if any, forward to the next higher column bits. As a result, when we add the next adjacent higher column bits, we would be required to add three bits if there were a carry from the previous addition. We have a similar situation for the other higher column bits also until we reach the MSB. A full adder is therefore essential for the hardware implementation of an adder circuit capable of adding larger binary numbers. A half-adder can be used for addition of LSBs only.. In order to arrive at the logic circuit for hardware implementation of a full adder, we will firstly write the Boolean expressions the two output variables, that is, the SUM and CARRY outputs, in terms of input variables. These expressions are then simplified by using any of the simplification techniques. The Boolean expressions for the two output variables for the SUM output (S) and for the CARRY output (Cout) are given in Equation (4.3)

$$S = \overline{A}.\overline{B}.C_{\text{in}} + \overline{A}.B.\overline{C}_{\text{in}} + A.\overline{B}.\overline{C}_{\text{in}} + A.B.C_{\text{in}}$$

$$C_{\text{out}} = \overline{A}.B.C_{\text{in}} + A.\overline{B}.C_{\text{in}} + A.B.\overline{C}_{\text{in}} + A.B.C_{\text{in}}$$

Table :4.1 Truth table of Full adder:

A	B	C	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The next step is to simplify the two expressions. We will do so with the help of the Karnaugh mapping technique. Karnaugh maps for the two expressions are given in Fig. 4.4(a) for the SUM output and Fig. 4.4 (b) for the CARRY output. As is clear from the two maps, the expression for the SUM (S) output cannot be simplified any further, whereas the simplified Boolean expression for Cout is given by the equation

Cout = B . Cin + A . B + A . Cin (4.4)

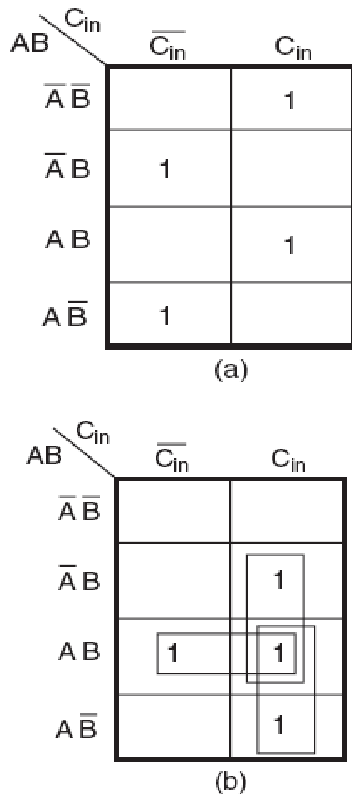

Fig 4.4 Karnaugh maps for the sum (a) and carry-out (b) of a full adder[18]

Figure 4.5shows the logic circuit diagram of the full adder. A full adder can also be seen to comprise two half-adders and an OR gate. The expressions for SUM and CARRY outputs can be rewritten as follows:

$$S = \overline{C}_{in}.(\overline{A}.B + A.\overline{B}) + C_{in}.(A.B + \overline{A}.\overline{B})$$
$$S = \overline{C}_{in}.(\overline{A}.B + A.\overline{B}) + C_{in}.(\overline{\overline{A}.B + A.\overline{B}})$$

$$C_{out} = A.B + C_{in}.(\overline{A}.B + A.\overline{B})$$

Boolean expression (4.5) can be implemented with a two-input EX-OR gate provided that one of the inputs is Cin and the other input is the output of another two-input EX-OR gate with A and B as its inputs. One of them is the AND output of A and B. The other is also the output of an AND gate whose inputs are Cin and the output of an EX-OR operation on A and B. The whole idea of writing the Boolean expressions in this modified form was to demonstrate the use of a half-adder circuit in building a full adder. Figure 4.5 (a) shows logic implementation of Equations (4.7) and (4.8). Figure 4.6 (b) is nothing but Fig. 4.6 (a) redrawn with the portion of the circuit representing a half-adder replaced with a block

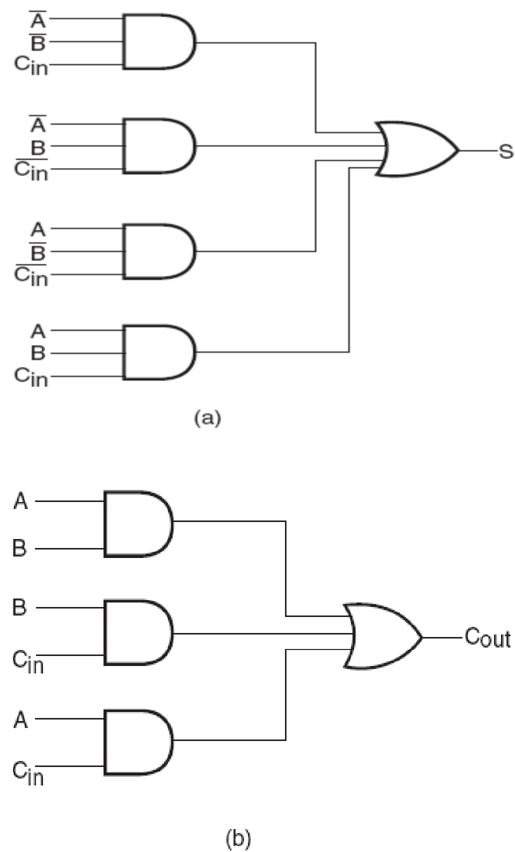

Fig 4.5 (a) &(b) Logic circuit diagram of a full adder[18]

V. PROPOSED TECHNIQUE

Stack technique:

Fig. below shows the block diagram of a digital circuit using Stack technique. In stack technique, MOS transistor is divided and stacked into two half width size transistors. When two half size stacked MOS transistors are turned off together, it induces reverse bias between them which results in the reduction of sub-threshold leakage power. However with increase in the number of transistors overall propagation delay of the circuit increases. Using CMOS technology is basically for consuming less power. In this design criterion it focuses on sub threshold leakage power consumption and it also focuses on body biasing effect and stack effect. One of the main contributors for the static power consumption is sub threshold leakage current which is shown in the Figure i.e., the drain to source current when the gate voltage is smaller than the threshold voltage. As the technology feature size shrink sub current is increases exponentially as the decrease of threshold voltage. Stacking transistor can reduce sub-threshold leakage. So it is called

stacked effect. Where two or more stacked transistor is turned off together, the result can reduce the leakage power [4]

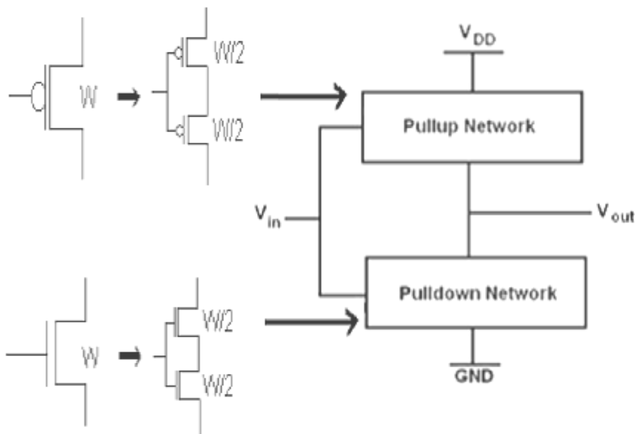

Fig 6.1 Single Transistor and Stacked transistor[4]

5.7 Layout design for full adder logic with stack transistor

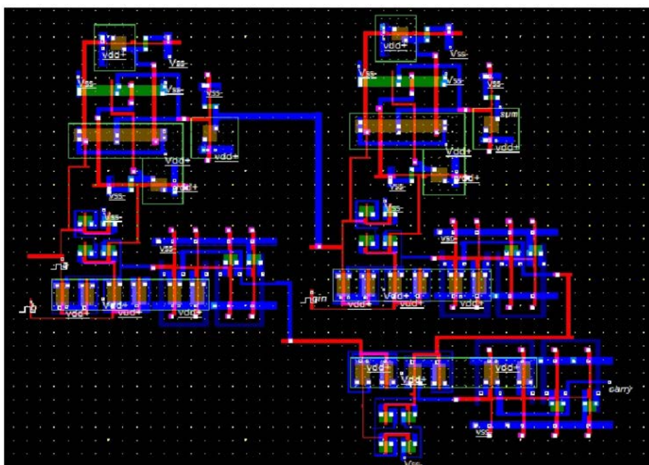

Fig 5.16 Layout design for full adder logic with stack transistor

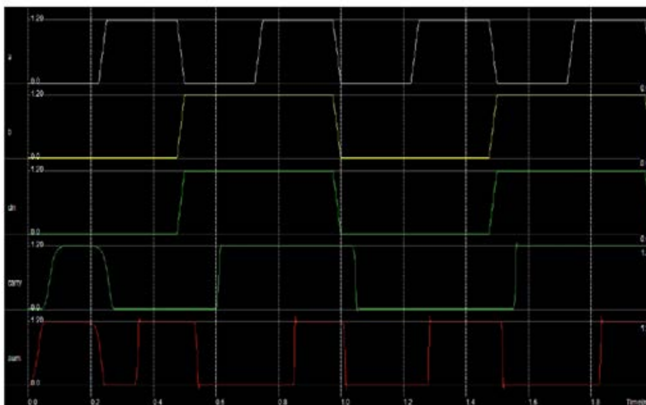

Fig 5.17 Timing simulation for full adder logic with stack transistor

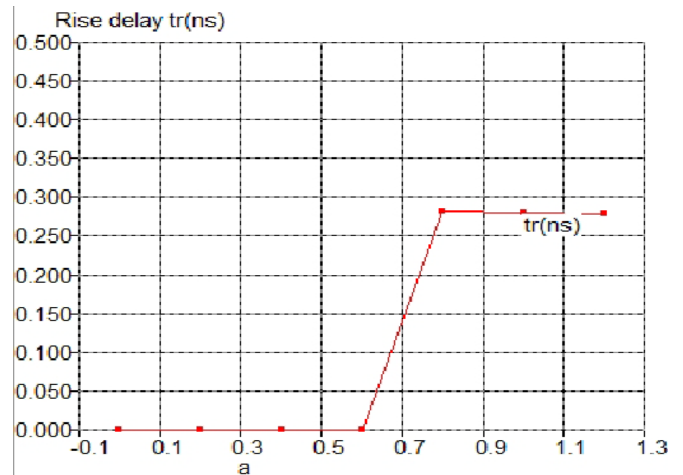

Fig 5.18 Rise delay from b to y2 for array logic logic with stack transistor

5.8 Elmore delay model

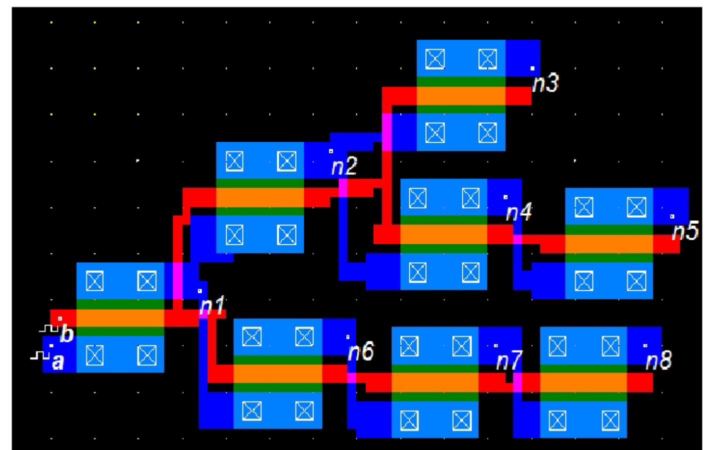

Fig 5.19 Elmore delay model simulation at node n7

Table 5.1 Delay analysis at each node of Elmore delay model

Node	Rise Delay ns
N1	0.231
N2	0.273
N3	0.278
N4	0.289
N5	0.295
N6	0.262
N7	0.279
N8	0.285

Table 5. 2 Montecarlo analysis at -25 to 110oC temperature delay analysis at node n1 of Elmore delay model

5.9 Layout design for array logic with long resistive path

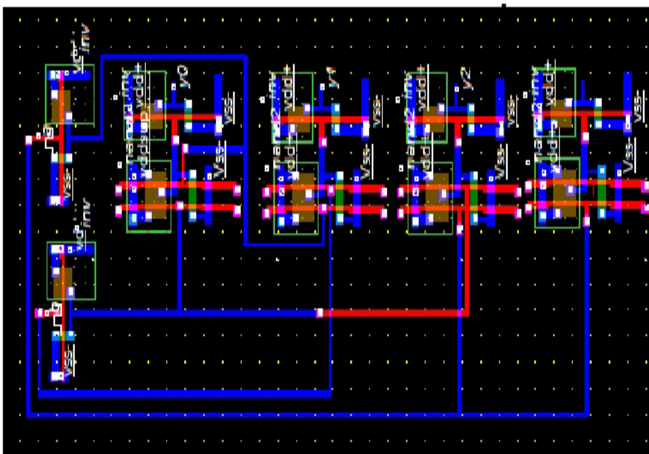

Fig 5.20 Layout design for array logic with long resistive path

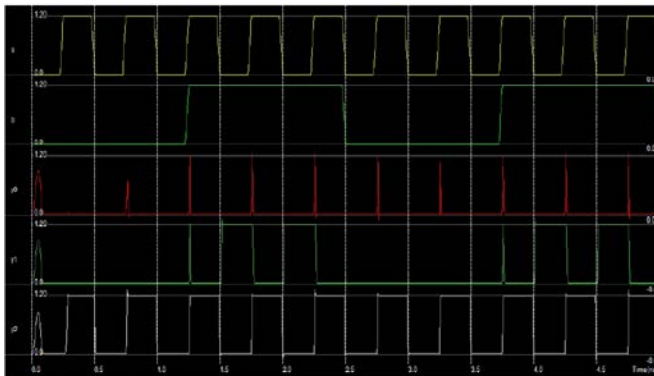

Fig 5.21 Timing simulation for array logic with long resistive path

5.10 Layout design for array logic with short resistive path

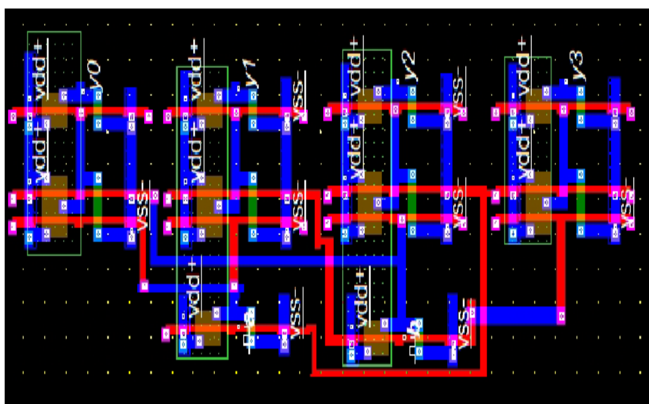

Fig 5.22 Layout design for array logic with short resistive path

Montecalo simulation at -25 to110 degree celcious	
Temperature	Delay ns
-25	0.078
2	0.023
29	0.01
56	6
83	0.004
110	0.003

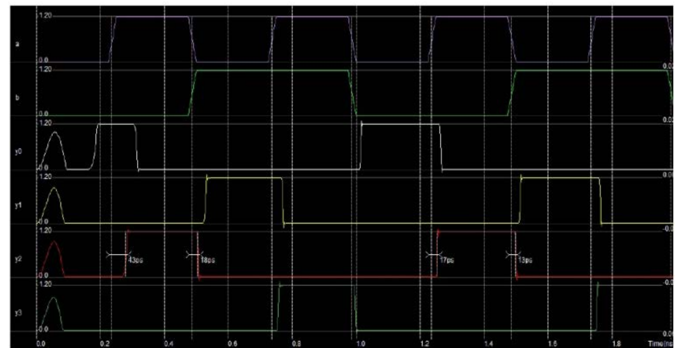

Fig 5.23 Timing simulation for array logic with short resistive path

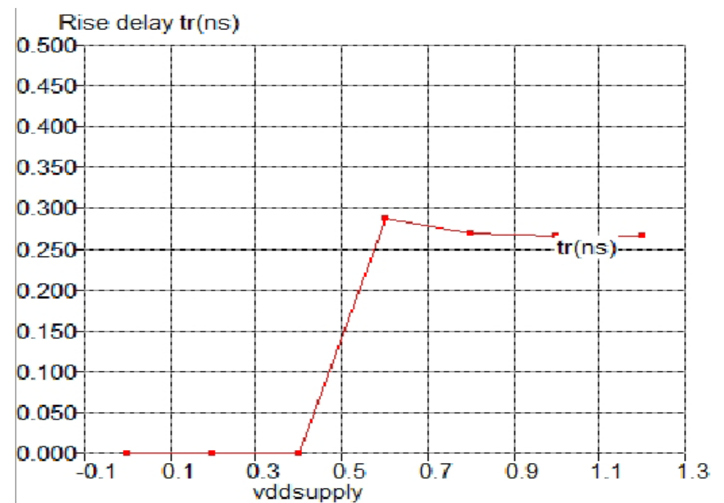

Fig 5.24 Rise delay from b to y2 for array logic with short resistive path

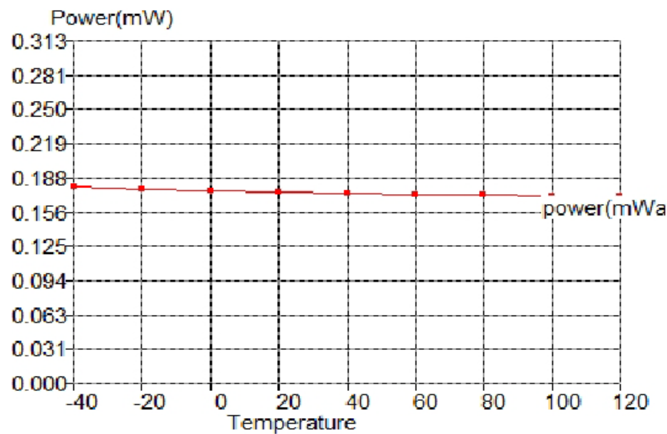

Fig 5.25 Power dissipation at y3 for array logic with short resistive path at 120°C temperature

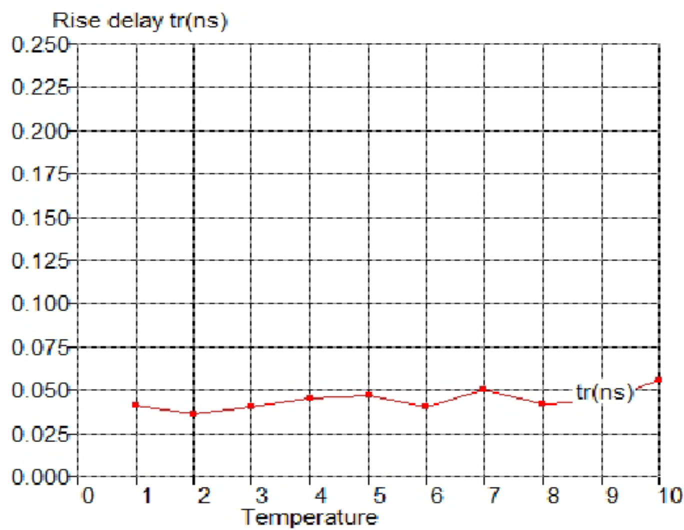

Fig 5.26 M Carlo analysis Rise delay from a to y3 for array logic with short resistive path at 120 0C temperature

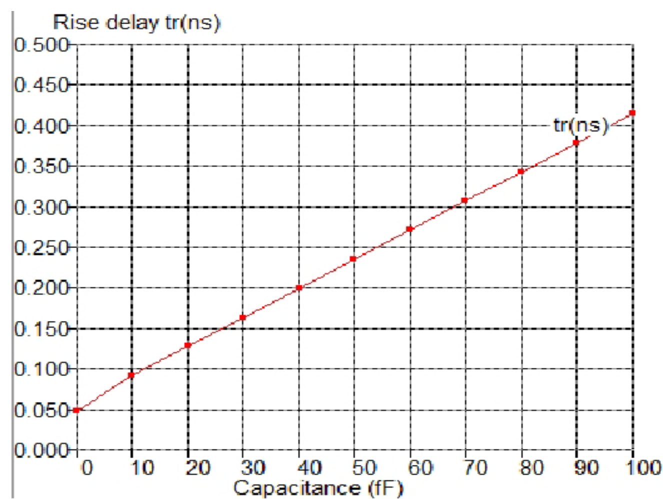

Fig 5.27 Rise delay from a to y3 for array logic with short resistive path at variable capacitance

VI. RESULT ANALYSIS

Table 6.1 Comparative analysis with related work

Comparative analysis with related work		
	Reference	Our work
Wn	0.5 to 1.0 un	0.6 un
Delay analysis	8.56ns to 3.72ns	0.23ns
Delay at -25oC temperature	10.5ns	78ps
Delay at 30oC temperature	3.52ns	1ps
Delay at 60oC temperature	1.7ns	6ps
Delay at 100oC temperature	0.91ns	3ps

VII. CONCLUSION

This thesis presents a comprehensive study on the influences of parasitic elements on the MOSFET switching performance. A circuit-level analytical model that takes MOSFET parasitic capacitances, pn junctions, resistances, and reverse current of the diode into consideration is given to evaluate the MOSFET switching characteristics. This work we analyze the parametric estimation for MOSFET switching delay, leakage current reduction , power dissipation and variation of temperature effects due to the parasitic devices.

This work reviewed circuit optimization design techniques for controlling the OFF current of CMOS circuits in both standby and active modes of circuit operation. The sub-threshold leakage control techniques that do not adversely affect the circuit performance and layout cost. This is especially important in light of both statistical process parameter variations and their impact on leakage currents. The average current for PMOS in this circuit is calculated as 1.948mA. The stacking of two off devices has significantly reduced sub-threshold leakage compared to a single off device. Logic gates after stack forcing will reduce leakage power, but incur a delay penalty, similar to replacing a low Vt device with a high-Vt device in a dual Vt design.

- In this thesis a stack transistor base layout for full adder circuit is design which reduces the leakage current.
- And also Estimate Delay on the RC Delay MOSFET model of structure of array decoder

VIII. FUTURE SCOPE

The advent of a mobile computing era has become a major motivation for low power design because the operation time of a mobile device is heavily restricted by its battery life. The growing complexity of mobile devices such as a cell phone with a digital camera or a personal digital assistant with global positioning system makes the power problem more challenging.

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