Robust Review of Carry Select Adder

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Abstract- In this review research work we have analyzed the various adders in order to improve the system performance of Carry Select Adder. A multiplier is one of the key hardware blocks in most digital and high performance systems such as in FIR filters, in digital signal processors and in the microprocessors etc. With the advances in technology, a lot of researchers have tried and are still trying to design the multipliers that offer any of the following- low power consumption, high speed, regularity of layout and hence less area of them in multiplier. Area and speed are two main conflicting constraints. Therefore improving speed results that always in larger areas. In this review work we have tried to analysis various adders and compare their speed and complexity of the circuit that is. the area occupied. The Carry Adder has a smaller area while having lesser speed, in the contrast to where Carry Select Adders are high speed except posses a larger area. Carry Look Ahead Adder is in the spectrum that having a proper tradeoff between the time and the area complexities.

Keywords- FPGA, Area efficient, Carry Select Adder (CSLA) & Square-root CSLA.

I. INTRODUCTION

In the study of area and power efficient high-speed data path logic systems are one of the main substantial areas of researches in VLSI system designs. In the digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum .However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input cin = 0 and cin = 1, then the final sum and carry are selected by the multiplexers. The power and Area of the Carry select Adder can be reduced by using BEC-1 converter instead of Ripple Carry Adder (RCA). The basic idea of this work is to use transistor level modified Binary to Excess-1 Converter (BEC) instead of Ordinary BEC (gate level) with cin = 1 in the CSLA to achieve lower area and power consumption. The main advantage of this transistor level modified BEC-1 comes from the lesser number of MOS transistor than the Ordinary BEC-1.

Power Optimization

Power refers to number of Joules dissipated over a certain amount of time whereas energy is the measure of the total number of Joules dissipated by a circuit. In digital CMOS design, the *power-delay product* is commonly used to assess the merits of designs. In a sense, this can be shown as *power* × *delay = (energy/delay)* × *delay = energy*, which implies delay is irrelevant.

Low-Power Multiplier Design

Multiplication consists of three steps: generation of partial products or (PPG), reduction of partial products (PPR), and finally carry-propagate addition (CPA).In general there are sequential and combinational multiplier implementations. Consider combinational case here because the scale of integration now is large enough to accept parallel multiplier implementations in digital VLSI systems. Different multiplication algorithms vary in the approaches of PPG, PPR, and CPA. For PPG, radix-2 is the easiest. To reduce the number of PPs and consequently reduce the area/delay of PP reduction, one operand is usually recoded into high-radix digit sets. The most popular one is the radix-4 digit set **{**-2,-1, 0, 1, 2**}.** For PPR, two alternatives exist: reduction by rows, performed by an array of adders, and reduction by columns, performed by an array of counters. The final CPA requires a fast adder scheme because it is on the *critical path*. In some cases, final CPA is postponed if it is advantageous to keep redundant results from PPG for further arithmetic operations.

The Adders

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. In any book on computer arithmetic, someone looks that there exists a large number of different circuit architectures with different performance characteristics and widely used in

the practice. Although many researches dealing with the binary adder structures have been done, the studies based on their comparative performance analysis are only a few. In this project, qualitative evaluations of the classified binary adder architectures are given. Among the huge member of the adders the VHDL code for Ripple-carry, Carry-select and Carry-look ahead to emphasize the common performance properties belong to their classes. With respect to asymptotic delay time and area complexity, the binary adder architectures can be categorized into four primary classes as given in Table 1. The given outcomes in the below table are the highest exponent term of the exact formulas, very complex for the high bit lengths of the operands. The first class consists of the very slow ripple-carry adder with the smallest area. In the second class, the carry-skip, carry-select adders with multiple levels have small area requirements and shortened computation times. From the third class, the carry-look ahead adder and from the fourth class, the parallel prefix adder represents the fastest addition schemes with the largest area complexities.

Complex (A)	Delay (T)	Product (AxT)	Adder Class Schemes
O(n)	O(n)	O(n2)	Ripple-Carry(1)
O(n)	O($n^{1/*1+1}$)	O(n^{1+2l+1})	Carry Select (2) Carry-skip (2) Carry-Inc (2)
O(n)	O(logn)	O(nlogn)	Carry look ahead (3)

TABLE 1 Categorization of adders w.r.t delay time and capacity

II. SYSTEM MODULE

Ripple Carry Adders (RCA)

Ripple carry adder is composed of cascaded full adders for n-bit adder, as shown in figure.1.It is constructed by cascading full adder blocks in series. The carry out of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder it requires n full adders.

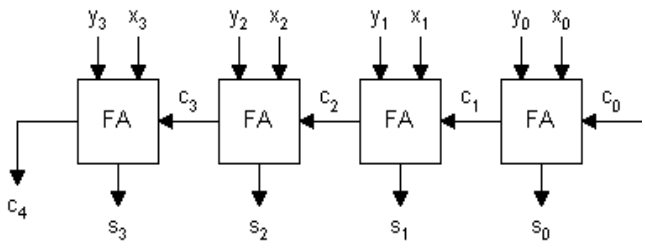

Fig.1. A 4-bit Ripple Carry Adder

- Not very efficient when large number bit numbers are used.
- Delay increases linearly with bit length.

Delay

Delay from Carry-in to Carry-out is more important than from A to carry-out or carry-in to SUM, because the carry-propagation chain will determine the latency of the whole circuit for a Ripple-Carry adder. Considering the above worst-case signal propagation path. For a k-bit RCA worst case path delay is

$$TRCA - k\ bit\ =\ TFA(x0, y0\ c0)\ +\ (k-2) * TFA(Cin\ Ci)\ +\ TFA(Cin\ Sk-1)\ .$$

Logic equations

$$gi\ =\ ai\ bi$$
$$p\ =\ ai\ xor\ bi.$$
$$Ci+1\ =\ gi\ +\ pici$$
$$Si\ =\ pi\ xor\ ci.$$

Complexity and Delay for n-bit RCA structure

$$ARCA\ =\ O\ (n)\ =\ 7n$$
$$TRCA\ =\ O\ (n)\ =\ 2n$$

Carry Select Adders (CSLA)

In Carry select adder scheme, blocks of bits are added in two ways: one assuming a carry-in of 0 and the other with a carry-in of 1.This results in two precompiled sum and carry-out signal pairs (s0i-1:k , c0i ; s1i-1:k , c1i) , later as the block's true carry-in (ck) becomes known , the correct signal pairs are selected. Generally multiplexers are used to propagate carries.

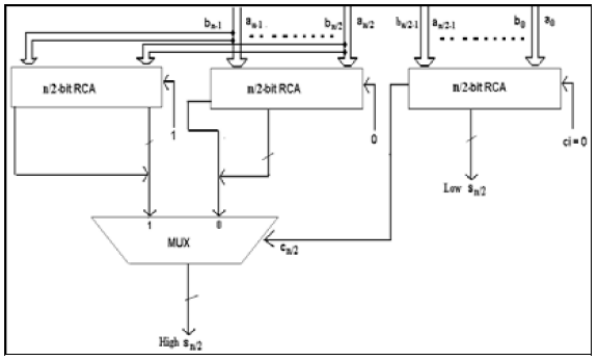

Fig.2. Carry Select Adder with 1 level using n/2- bit RCA

- Because of multiplexers larger area is required.

- Have a lesser delay than Ripple Carry Adders (half delay of RCA).
- Carry Select Adder while working with smaller no of bits.

Logic equations

$$si-1:k \;=\; ck\,s0i-1:k \;+\; ck\,s1i-1:k\_$$
$$ci \;=\; ck\,c0i \;+\; ck\,c1i$$

Complexity and Delay for n-bit CSLA structure

$$ACSLA \;=\; O\,(n) \;=\; 14n$$
$$TCSLA \;=\; O\,(n1/*\,l+1) \;=\; 2.8n1/2.$$

BEC

As stated above the main idea of this work is to use transistor level modified BEC instead of the ordinary BEC with cin=1 in order to reduce the area and power consumption of the CSLA. To replace the n-bit ordinary BEC, an n-bit transistor level modified BEC is required. The function table of a 3-b BEC the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

Input [0:3]	Output [0:3]
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

TABLE 2:FUNCTION TABLE OF THE 3-BIT BEC

III. LITERATURE REVIEW

In the year of 2014 Pandey, S.; Khan, A.A.; Sarma, R., [1] Investigated on comparison between the design of the 8T adder based Carry Select Adder (CSA) and 10T adder based CSA. Using both the designs of adders 4-bits CSA architecture has been developed and compared with the 28T adder 4-bit CSA. The 10T CSA design has reduced delay, power and area as compared with the 28T CSA with a slight tradeoff for area as compared to 8T CSA. The analysis shows that the 10T CSA is better than both 8T adder based CSA and 28T CSA. This work evaluates the performance of the 10T CSA design in terms of power, delay and area using 180nm CMOS process technology Cadence Virtuoso tool and Spectre simulator.

In the year of 2014 Paradhasaradhi, D.; Prashanthi, M.; Vivek, N[2] described that the Carry Select Adder (CSLA) provides a good compromise between cost and performance in carry propagation adder design. A Square Root Carry Select Adder using RCA is introduced but it offers some speed penalty. However, conventional CSLA is still area-consuming due to the dual ripple carry adder structure. In the proposed work, generally in Wallace multiplier the partial products are reduced as soon as possible and the final carry propagation path carry select adder is used. In this paper, modification is done at gate level to reduce area and power consumption. The Modified Square Root Carry Select-Adder (MCSLA) is designed using Common Boolean Logic and then compared with regular CSLA respective architectures, and this MCSLA is implemented in Wallace Tree Multiplier. This work gives the reduced area compared to normal Wallace tree multiplier. Finally an area efficient Wallace tree multiplier is designed using common Boolean logic based square root carry select adder.

In the year of 2014 Rahul Chandran, G.; Saraswathi, N [3] presented that the Carry Select Adder (CSLA) is one of the most commonly used adder circuits in many arithmetic operations. Most of the multipliers and adders make use of CSLA's. Regular Square root Carry Select Adder.

In the year of 2014 Naaz, S.A.; Pradeep, M.N.; Bhairannawar, S.; Halvi, S.,[4] presented the study of field of communication and signal processing applications. Every application demands for a higher throughput arithmetic operation. One of the key arithmetic operations is multiplication which takes maximum execution time. The development of efficient multiplier is a subject of interest over decades. So there is a need for an efficient multiplier which obtains higher performance for real time signal processing application. The modular design of Vedic multiplier using carry select adder. The delay of proposed multiplier is reduced due to high speed carry select adder. The proposed multiplier is applied to parallel FIR filter. It can be observed that the combinational delay reduced for the proposed multiplier compared to existing architecture.

In the year of 2013 Mugilvannan, L.; Ramasamy, S., [5] Investigated on Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient transistor level modification in BEC-1 converter to significantly reduce the area and power of the CSLA. Based on this modification 16-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the SQRT CSLA architecture using ordinary BEC-1 converter. The proposed design has reduced area and power as compared with the SQRT CSLA using ordinary BEC-1 converter with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, and power by hand with logical effort and through Cadence Virtuoso. The results analysis shows that the proposed CSLA structure is better than the SQRT CSLA with ordinary BEC-1 converter.

In the year of 2013 Vijayalakshmi, V.; Seshadri, R.; Ramakrishnan, S., [6] worked on the study of the VLSI design of the carry look-ahead adder (CLAA) based 32-bit unsigned integer multiplier and the VLSI design of the carry select adder (CSLA) based 32-bit unsigned integer multiplier. Both the VLSI design of multiplier multiplies two 32-bit unsigned integer values and gives a product term of 64-bit values. The CLAA based multiplier uses the delay time of 99ns for performing multiplication operation where as in CSLA based multiplier also uses nearly the same delay time for multiplication operation. But the area needed for CLAA multiplier is reduced to 31% by the CSLA based multiplier to complete the multiplication operation. These multipliers are implemented using Altera Quartus II and timing diagrams are viewed through avan waves.

IV. PROBLEM FORMULATION

The problem originally, on Low Power Techniques on different multipliers needs to be done in order to make us choose a proper multiplier in accordance with the requirements by making the best possible trade off choice between Speed and Power in different circumstances. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low- power VLSI system design. There has been extensive work on low-power multipliers at technology, physical, circuit and logic levels. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. Though, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully parallel.

V. CONCLUSIONS & FUTURE SCOPE

We studied about different adders among compared them by different criteria like Area, Time and then Area-Delay Product etc. so that we can judge to know which adder was best suited for situation. After comparing all we came to a conclusion that Carry Select Adders are best suited for situations where Speed is the only criteria. Similarly Ripple Carry Adders are best suited for Low Power Applications. But Among all the Carry Look Ahead Adder had the least Area-Delay product that tells us that, it is suitable for situations where both low power and fastness are a criteria such that we need a proper balance between both as is the case with our study. This review study is to complete area efficient objectives that are to study different Multiplier and learn the Power and Time trade off among them so that we can design Efficient Faster Low Power Multiplier. To develop arithmetic algorithm and architecture level optimization techniques for low-power multiplier design, the research presented in this analysis through review work has achieved good demonstration the efficiency of high level optimization techniques.

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