Efficient On-Chip Interconnection Routing of VLSI Design for Faster Computation

Swati Nigam[1], Prof. Nitesh Dodkey[2]

[1]M-Tech Research Scholar, [2]HOD, Research Guide

Department of Electronics & Communication Surabhi Group of Institutions, Bhopal

Abstract - The proposed routing technique for the on chip interconnection of network is shown in this paper. The network on chip is considered for the faster routing and computation of signal in networks using integrated circuits. These ICs works on the different routing techniques some researchers worked on that and made improvements. In this paper we are proposing a mesh based routing methodology to enhance the performance as well as speedup calculations. The outcomes will be shown in terms of area, delay and Max. Frequency of the proposed routing methodology. The programming has been synthesized on XILINX 13.1 and from synthesis report it is clearly visible that the proposed work has better architecture than previous one.

Keywords - NoC, Verilog, Mesh, Fast Computation, Interconnection.

I. INTRODUCTION

The NoC design paradigm has been proposed as the future of ASIC design. The major driving force behind the transition to NoC based solutions is the inadequacy of current day VLSI inter-chip communication design methodology for the deep sub-micron chip manufacturing technology. The negative effect of technology scaling on global interconnects, increased dependence on fault-tolerant mechanisms as feature size reduces, increasing use of parallel architectures are the reasons why NoC is becoming popular. The NoC based system on chips impose various design issues on the fabrication of such integrated chips.

Firstly, the suitable topology for the target NoCs such that the performance requirements and design constraints are satisfied. Secondly, the design of network interfaces to access the on chip network and routers to provide the physical interconnection mechanisms to transport data between processing cores. Thirdly, the selection of communication protocols which are suitable for on chip interconnection networks. Finally, as technology scales and switching speed increases, future network on chips will become more sensitive and prone to errors and faults. Fault tolerance is becoming critical for on chip communications.

Today's SoCs need a network on chip IP interconnect fabric to reduce wire routing congestion, to ease timing closure, for higher operating frequencies and to change IP easily. Network on chips are a critical technology that will enable the success of future system on chips for embedded applications. This technology of network on chips are expected to dominate computing platforms in the near future.

On the other hand, a Network on a Chip (NoC), i.e., a communication-centric platform, offers an on-chip interconnection network. The NoC is one of the on-chip communication systems. The NoC is used in place of conventional shared bus systems. For example, the NoC is used for applications such as optical or wireless communications, etc.In the NoC, the number of wires is able to be reduced in the chip area, since neighboring cores are connected to each other. But, the conventional shared bus systems have some problems: one problem is increasing the huge number of wires as the number of cores increases, the other is that it is very hard to control clocks in the chip Thus, these problems in the shared bus system can be solved by the NoC. In addition, since the neighboring cores are connected to each other, high speed communication can also be achieved. The constraint of the clock in the design of the chip can resolve by the NoC architectures. However, latency can be caused in data transmission, since data traverses over the several numbers of cores in the NoC.

For connecting cores to each other, there are many NoC topologies such as Mesh and Ring, Spidergon. To evaluate the NoC topologies, a simulation based approach was used for the modeling and analysis of the topologies. However, some properties of the topologies could affect the performance of the NoC systems. Among many topologies in massively parallel computer systems including the NoC architectures, interconnection networks have become the center of focus because of those network structures and topologies as well as the processing elements greatly influencing system cost and performance.

II. SYSTEM MODEL

In this work, we present the performances of the topologies about the communication aspects by the simulation based approach and comparative study of various topologies in terms of average network delay and comparing all the topologies according to the delay parameter.

ISO/OSI network protocol stack model:

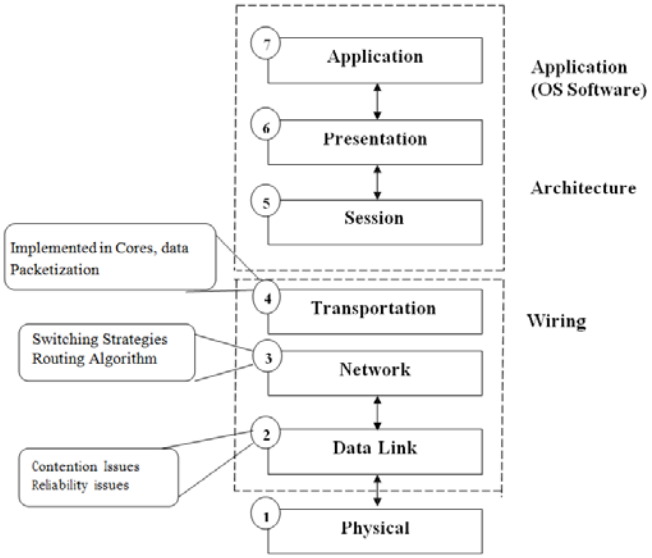

Figure 1 ISO/OSI network protocol stack model

Initially the chip designing was aimed at producing chips that contained a single stand alone design. As the number of transistors that is fabricated onto a single chip increased, the concept of system on chip was made possible. In a system on chip (SoC), multiple stand alone designs, referred to as cores or Intellectual Property cores are stitched together on a chip to provide a functional system. NoC is an approach to design the communication subsystem between intellectual property cores in a system on chip. The communication strategy in system on chip uses dedicated buses between communicating resources. This will not give any flexibility since the needs of the communication, in each case, have to be thought of every time a design is made. Another possibility is the use of common buses, which have the problem that it does not scale very well, as the number of resources grows. NoC is intended to solve the shortcomings of these, by implementing a communication network of switches/micro routers and resources.

The NoC design paradigm has been proposed as the future of ASIC design. The major driving force behind them transition to NoC based solutions is the inadequacy of current day VLSI inter-chip communication design methodology for the deep sub-micron chip manufacturing technology. The negative effect of technology scaling on global interconnects, increased dependence on fault-tolerant mechanisms as feature size reduces, increasing use of parallel architectures are the reasons why NoC is becoming popular.

The NoC based system on chips imposes various design issues on the fabrication of such integrated chips. Firstly, the suitable topology for the target NoCs such that the performance requirements and design constraints are satisfied. Secondly, the design of network interfaces to access them on chip network and routers to provide the physical interconnection mechanisms to transport data between processing cores. Thirdly, the selection of communication protocols which are suitable for on chip interconnection networks. Finally, as technology scales and switching speed increases, future network on chips will become more sensitive and prone to errors and faults. Fault tolerance is becoming critical for onchip communications.

III. PROPOSED METHODOLOGY

The on-chip interconnection network topology defines how the PCs are interconnected by communication links. There are many factors that affect the choice of an appropriate on-chip interconnection network. Major factors include the following [11]:

- Performance requirement. These requirements are generally represented by packet latency and throughput.
- Scalability. A scalable architecture implies that as more PCs are added, the I/O bandwidth, and network bandwidth should increase proportionally.
- Simplicity. Simple designs often lead to higher clock frequencies and may achieve higher performance.
- Distance span. In some interconnection networks, links have very different lengths and some links may very long, producing problems such as coupling, electromagnetic noise, and heavy link cables.
- Physical constraints. Packing components in an interconnection network, such as processors, memories, and/or I/O devices, together usually requires meeting certain physical constraints, such as operating temperature control, wiring length limitation, and space limitation.
- Reliability and fault tolerance. An interconnection network should be able to deliver information reliably, and be designed for continuous operation in the presence of a limited number of faults.

IV. SYNTHESIS OUTCOMES

Simulation refers to the verification of a design, its function and performance. It is the process of applying stimuli to a model over time and producing corresponding responses from a model. The simulation is performed in XILINX ISE 13.1 software. The routing pattern is observed from the output signals (datao). The output signals follow the round robin scheduling algorithm. The data at the input ports is directed to the output port depending on the first three bits of the input data which act as the select lines of the demultiplexer. At that instance the scheduling signal will be high which indicates the port to be read in the next instance. Likewise the other data packets are also routed.

The constructed NoC systems will then be simulated using test benches which specify the simulation parameters, such as traffic pattern, injection rate, packet length, and number of packets to be generated. The simulation results including the injection time and reception time of each packet will be collected and displayed. The performance metrics will then be calculated in Excel.

The demultiplexer directs the input to the proper output port according to the select signal.The select signal is taken as the first three bits of the inputdata. The demultiplexer also has an enable. If this enable is setto 1, then the input data is transferred to the appropriate outputport and the corresponding write enable is set to

1, while the other output ports and write enables are set to zeros. If the enable signal is

0, then the output ports and the write enables are all set to zero.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	492	138240	0%
Number of Slice LUTs	1022	138240	0%
Number of fully used LUT-FF pairs	492	1022	48%
Number of bonded IOBs	51	800	6%
Number of BUFG/BUFGCTRLs	1	32	3%

Fig. 4.1 Device Utilization Summary

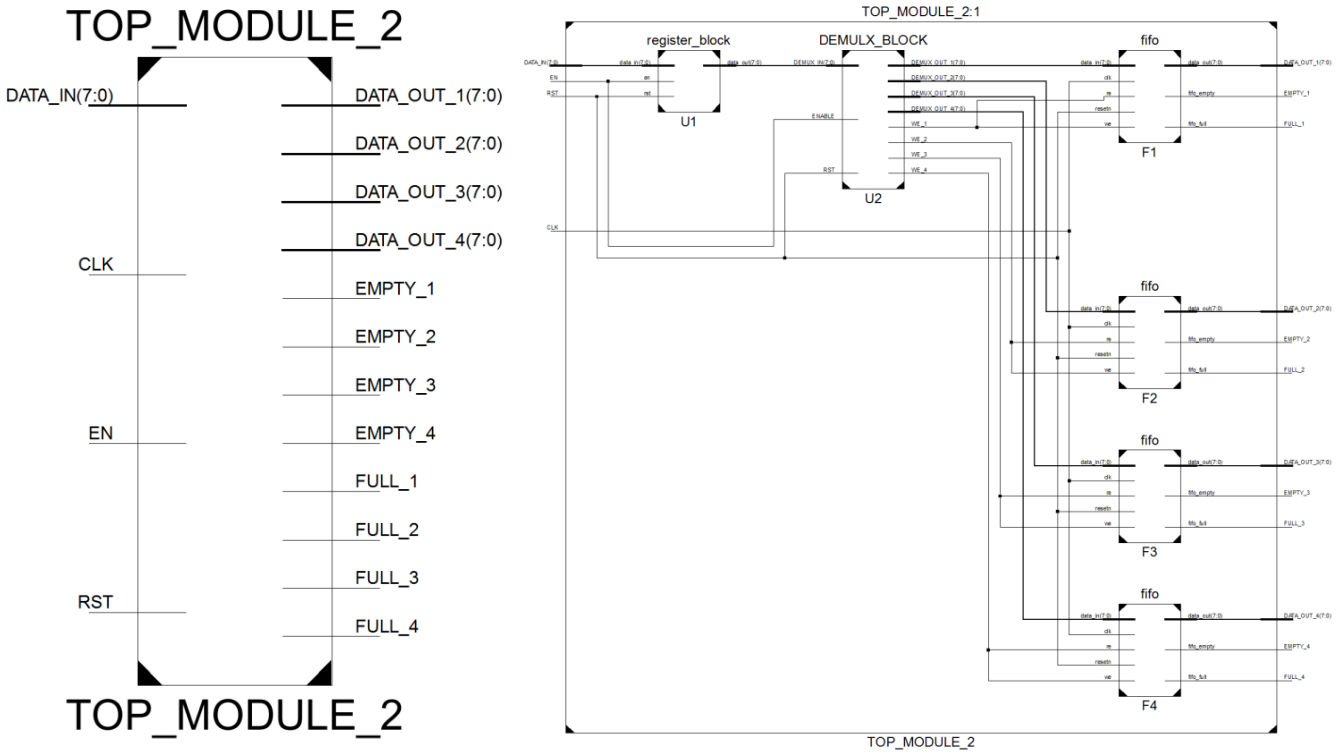

Fig. 4.2 Schematic of Proposed Design

Table I: Timing Summary and Details

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 2.650ns (Maximum Frequency: 377.423MHz)
   Minimum input arrival time before clock: 3.646ns
   Maximum output required time after clock: 4.666ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================
Timing constraint: Default period analysis for Clock 'CLK'
  Clock period: 2.650ns (frequency: 377.423MHz)
  Total number of paths / destination ports: 8833 / 536
-------------------------------------------------------------------------
Delay:               2.650ns (Levels of Logic = 2)
  Source:            F4/read_pointer_3 (FF)
  Destination:       F4/write_pointer_2 (FF)
  Source Clock:      CLK rising
  Destination Clock: CLK rising

  Data Path: F4/read_pointer_3 to F4/write_pointer_2
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net
    ----------------------------------------  ------------
     FD:C->Q              19   0.396   0.903  F4/read_pointer_3
     LUT5:I0->O            1   0.086   0.412  F4/write_pointer_o
     LUT6:I5->O            4   0.086   0.299  F4/write_pointer_o
     FDR:R                     0.468          F4/write_pointer_2
    ----------------------------------------
    Total                    2.650ns (1.036ns logic, 1.614ns route)
                                     (39.1% logic, 60.9% route)

=========================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'CLK'
  Total number of paths / destination ports: 3372 / 968
-------------------------------------------------------------------------
---------
Offset:              3.646ns (Levels of Logic = 5)
  Source:            RST (PAD)
  Destination:       F2/read_pointer_2 (FF)
  Destination Clock: CLK rising

  Data Path: RST to F2/read_pointer_2
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net
    ----------------------------------------  ------------
     IBUF:I->O           526   0.694   0.844  RST_IBUF (RST_IBU
     LUT4:I0->O           81   0.086   0.778  U2/DEMUX_OUT_2<2>1
     LUT4:I0->O            3   0.086   0.496  F2/read_pointer_or
     LUT6:I4->O            2   0.086   0.491  F2/read_pointer_or
     LUT5:I3->O            1   0.086   0.000  F2/read_pointer_2_
     FD:D                     -0.022          F2/read_pointer_2
    ----------------------------------------
    Total                    3.646ns (1.038ns logic, 2.608ns route)
                                     (28.5% logic, 71.5% route)
=========================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'CLK'
  Total number of paths / destination ports: 108 / 36
-------------------------------------------------------------------------
Offset:              4.666ns (Levels of Logic = 3)
  Source:            F3/read_pointer_3 (FF)
  Destination:       EMPTY_3 (PAD)
  Source Clock:      CLK rising

  Data Path: F3/read_pointer_3 to EMPTY_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net
    ----------------------------------------  ------------
     FD:C->Q              18   0.396   0.741  F3/read_pointer_3
     LUT4:I0->O           41   0.086   0.928  F3/fifo_empty411
     LUT5:I0->O            1   0.086   0.286  F3/fifo_empty42
     OBUF:I->O                 2.144          EMPTY_3_OBUF
    ----------------------------------------
    Total                    4.666ns (2.712ns logic, 1.954ns route)
                                     (58.1% logic, 41.9% route)
```

V. CONCLUSION AND FUTURE SCOPE

A Network on a Chip (NoC), i.e. communication centric platform, offers an on-chip interconnection network. We use mesh NoC topologies for connecting cores to each other. To evaluate the NoC topologies, a simulation based approach was used for the modeling and analysis of the topology. However, some properties of the topology could affect the performance Such as Delay, Frequency, memory and Power of the NoC systems. In this work, we present the performances of the mesh topology about the simulation based approach.

The ultimate goal of this project is to develop a FPGA-based NoC emulation system. The work conducted in this work is the first part of the whole project. Future work includes the extension of the NoC simulation system to support more network topologies and the implementation of the simulated NoC architectures on FPGA.

REFERENCES

[1] Chaochao Fengl,2*, Jinwen Lil, Zhonghai Lu2, Axel Jantsch2, Minxuan Zhangl,"Evaluation of Deflection Routing on Various NoC Topologies",2011.

[2] Pratiksha Gehlot , Shailesh Singh Chouhan, "Performance Evaluation of Network on Chip Architectures",2009 International Conference on Emerging Trends in Electronic and Photonic Devices & Systems (ELECTRO-2009).

[3] Haytham Elmiligit, Ahmed A. Morgant, M. Watheq El-Kharashil, and Fayez Gebalit, "Performance Analysis of Networks-on-Chip Routers",2007.

[4] Sudeep Pasricha and Nikil Dutt,"On-Chip Communication Architectures", Chapter 12 .

[5] Shashi Kumar1, Axel Jantsch1, Juha-Pekka Soininen2, Martti Forsell2,Mikael Millberg1, Johny Öberg1, Kari Tiensyrjä2 and Ahmed Hemani3, "A Network on Chip Architecture and Design Methodology",2002

[6] A Delay-Aware Topology-based Design for Network-on-chip Applications By Haytham Elmiligi, Ahmed A. Morgan, M. Watheq El-Kharashi, Fayez Gebali.

[7] M. Nickray, M.Dehyadgari and A. Afzali-khusha; Power and Delay optimization for Network on chip.

[8] Extended-Butterfly fat Tree Interconnection(EFTI) Architecture Network On Chip By Hemayet Hossain IEEE, Md. Mostofa Akbar IEEE and Md. Monirul Islam IEEE.

[9] An application specific NOC mapping for optimized delay By Wenbiao Zhou1,2, Yan Zhang2 Zhigang Mao1.

[10] An Empirical Investigation of Mesh and Torus NoC Topologies Under Different Routing Algorithms and Traffic Models By M. Mirza- Aghatabar+,S.Koohi+, S. Hessabi*, M. Pedram†

[11] J. Duato, S. Yalamanchili, and L. Ni, Interconnection

networks: an engineering approach, Morgan Kaufmann Publishers, 2003, pp. 62.

[12] W. J. Dally and C. L. Seitz, "The torus routing chip," Technical Report 5208: TR: 86, C. S. Dept., California Inst. of Technology, pp. 1-19, 1986.

[13] P. Guerrier and A. Greiner, "A generic architecture for on-chip packetswitched interconnections," Proc. Design and Test in Europe (DATE), 2000, pp. 250-256.

[14] W. J. Dally and B. Towles, "Route packets, not wires: on-chip interconnection networks," Proc. 38th Design Automation Conf. (DAC), pp. 684-689, 2001.

[15] A. Jerraya, H. Tenhunen, and W. Wolf, "Multiprocessor systems-on-chips," Computer, vol. 38, no. 7, pp. 36-41, 2005.

[16] F. Karim, "An interconnect architecture for networking systems on chips," IEEE Micro, vol. 22, no. 5, pp. 36-45, 2002.

[17] P. P. Pande, C. Grecu, A. Ivanov, and R. Saleh, "Design of a switch for network on chip applications," Proc. Int'l Symp. Circuits and Systems (ISCAS), 2003, pp. 217-220.

[18] P. P. Pande, C. Grecu, M. Jones, A. Ivanov, and R. Saleh, "Performance evaluation and design trade-offs for network-on-chip interconnect architectures," IEEE Trans. Comput., pp. 1025-1040, 2005.

[19] S. Kumar, "A network on chip architecture and design methodology," Proc. Int'l Symp. VLSI (ISVLSI), 2002, pp. 117-124.

[20] N. Genko, D. Atienza, G. D. Micheli, and L. Benini, "Feature-NoC emulation: a tool and design flow for MPSoC," IEEE Circuits and Systems Magazine, vol. 7, no. 4, pp. 42-51, 4th Quarter 2007.