High Performance VLSI Architecture for 2-D DWT Using Lifting Scheme

Vivek Gautam[1], Prof. Ashish Singhadia[2]

[1]*Research Scholar, RKDF University, Bhopal*

[2]*Professor, Dept. Of Electronics and Communication Engg., RKDF University, Bhopal*

Abstract:-In this paper, we propose a high-performance and memory-efficient pipeline architecture which performs the one-level two-dimensional discrete wavelet transform (2-D DWT) in the 5/3 and 9/7 filters. In general, the internal memory size of 2-D architecture highly depends on the pipeline registers of 1-D DWT. Based on the lifting-based DWT algorithm, the primitive data path is modified and an efficient pipeline architecture is derived to shorten the data path. Accordingly, under the same arithmetic resources, the 1-D DWT pipeline architecture can operate at a higher processing speed (up to 200MHz in .25um technology) than other pipelined architectures with direct implementation. The proposed 2-D DWT architecture is composed of two 1-D processors (column and row processors). Based on the modified algorithm, the row processor can partially execute each row-wise transform with only two column-processed data. Thus, the pipeline registers of 1-D architecture do not fully turn into the internal memory of 2-D DWT. For an NxM image, only 3.5N internal memory is required for the 5/3 filter, and 5.5N is required for the 9/7 filter to perform the one-level 2-D DWT decomposition with the critical path of one multiplier delay (i.e. N and M indicate the height and width of an image). The pipeline data path is regular and practicable. Finally, the proposed architecture implements the 5/3 and 9/7 filters by cascading the three key components.

Index Terms: lifting-based DWT, two-dimensional discrete wavelet transform, JPEG 2000.

I. INTRODUCTION

The Discrete Wavelet Transform (DWT) plays a major role in the fields of signal analysis, computer vision, object recognition, image compression and video compression standard. The advantage of DWT over other traditional transformations is that it performs multi resolution analysis of signals with localization both in time and frequency as described by Mallat [3]. At present, many VLSI architectures for the 2-D DWT have been proposed to meet the requirements of real-time processing. The implementation of DWT in practical system has issues. First, the complexity of wavelet transform is several times higher than that of DCT. Second, DWT needs extra memory for storing the intermediate computational results. Moreover, for real time image compression, DWT has to process massive amounts of data at high speeds. The use of software implementation of DWT image compression provides flexibility for manipulation but it may not meet timing constraints in certain applications. Hardware implementation of DWT has practical obstacles. First, is that the high cost of hardware implementation of multipliers Filter bank implementation of DWT contains two FIR filters. It has traditionally been implemented by convolution or the finite impulse response (FIR) filter bank structures. Such implementations require both large number of arithmetic computations and storage,which are not desirable for either high speed or low power image/video processing applications. Therefore a new approach called the lifting scheme based wavelet transform was proposed based on a spatial construction of the second generation wavelet and a very versatile scheme for its factorization has been suggested.The lifting scheme has many advantages over the previous approaches. In particular, all the interesting properties of wavelets, such as bi-orthogonality and regularity, are defined by linear relationships between the filter bank coefficients. As a consequence, it is easier to design wavelet filters. Unlike convolutional wavelets, lifting scheme does not depend on Fourier transform of the wavelets. As a consequence, wavelets can be designed on arbitrary lattices in spatial domain. Since the lifting scheme makes optimal use of similarities between the high and low pass filters to speed up the calculation of wavelet transform, it has been adopted in the image compression standard JPEG2000. The various architectures differ in terms of required numbers of the multipliers, adders and registers, as well as the amount of accessing external memory, and leads to decrease efficiently the hardware cost and power consumption of design.Inspite of improving the efficiency of existing architectures, the present requirement is to improve the hardware utilization and capable of handling multiple data streams for the calculation of 2D DWT.

II. DISCRETE WAVELET TRANSFORM USING CONVOLUTION

The inherent time-scale locality characteristics of the discrete wavelet transforms (DWT) have established as powerful tool for numerous applications such as signal analysis, signal compression and numerical analysis. This has led numerous research groups to develop algorithms and hardware architectures to implement the DWT. Discrete wavelet transform (DWT) is being increasingly used for image coding. This is due to the fact that DWT supports features like progressive image transmission, ease of compressed image manipulation, region of interest coding etc. The VLSI architectures proposed in for hardware implementations of DWT are mainly convolution-based. In the conventional convolution method of DWT, a pair of Finite Impulse Response filters (FIR) is applied in parallel to derive high pass and low-pass filter coefficients pyramid algorithm [3] can be used to represent the wavelet coefficients of image in several spatial orientations. The architectures are mostly folded and can be broadly classified into serial and parallel architectures. The architecture in [5] implements filter bank structure efficiently using digit serial pipelining. The architecture proposed in [1] employs polyphase decomposition and coefficient folding technique for efficient implementation of discrete wavelet transform. A general fashion in which DWT decomposes the input image is shown below in Fig.1.

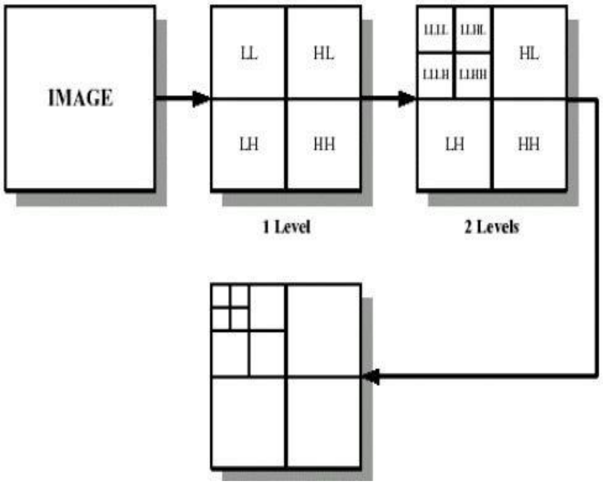


Figure. 1 Three level decomposition of an image

III. LIFTING BASED DWT

The lifting scheme is a new method to construct wavelet basis, which was first introduced by Swelden's. The lifting scheme entirely relies on the spatial domain, has many advantages compared to filter bank structure, such as lower area, power consumption and computational complexity. The lifting scheme can be easily implemented by hardware due to its significantly reduced computations. Lifting has other advantages, such as "in-place" computation of the DWT, integer-to-integer wavelet transforms which are useful for lossless coding. The lifting scheme has beendeveloped as a flexible tool suitable for constructing the second generation wavelets. It is composed of three basic operation stages: split, predict and update. Fig.3. shows the lifting scheme of the wavelet filter computing one dimension signal.The threebasic steps in Lifting based DWT are:

Split step: where the signal is split into even and odd points, because the maximum correlationbetween adjacent pixels can be utilized for the next predict step. For each pair of given input samples x(n) split into even x(2n) and odd coefficients x(2n+1).

Predict step: The even samples are multiplied by the predict factor and then the results are addedto the odd samples to generate the detailed coefficients (dj).Detailed coefficients results in high pass filtering.

$$\mathbf{HP[2n+1]=X[2n-1]-\frac{\mathit{X}[2\mathit{N}]+\mathit{X}[2\mathit{N}+1]}{2}\ldots\ldots\ldots\ldots(1)}$$

Update step: The detailed coefficients computed by the predict step are multiplied by the updatefactors and then the results are added to the even samples to get the coarse coefficients (sj).The coarser coefficients gives low pass filtered output.

$$\mathrm{LP[2n]=X[2n]+}\frac{HP[2n-1]+HP[2n+1]+2}{4}\ldots\ldots\ldots\ldots(2)$$

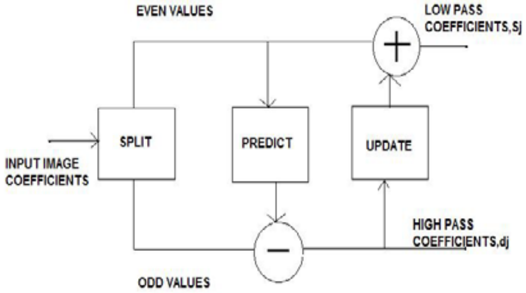


Figure. 2 Block diagram of forward Liftingscheme

IV. TWO-DIMENSIONAL DISCRETE WAVELET TRANSFORM

The main challenges in the hardware architectures for 1-D DWT are the processing speed and the number of multipliers and adders while for 2-D DWT it is the memory issue that dominates the hardware cost and the architectural complexity. A 2-D DWT is a separable transform where 1-D wavelet transform is taken along the rows and then a 1-D wavelet transform along the columns. The 2-D DWT operates by inserting array transposition between the two 1-D

DWT.The rows of the array are processed first with only one level of decomposition. This essentially divides the array into two vertical halves, with the first half storing the average coefficients, while the second vertical half stores the detail coefficients. This process is repeated again with the columns, resulting in four sub-bands within the array defined by filter output.as in three-leveldecomposition.

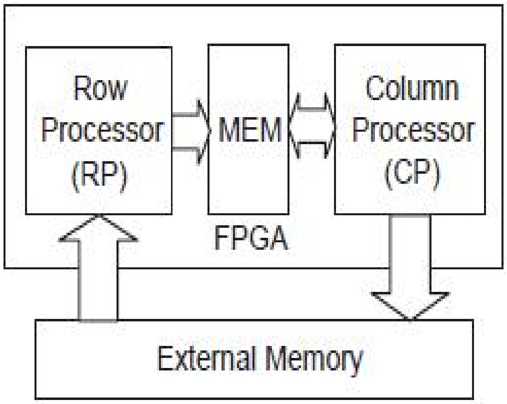


Figure 3. A Generic 2D DWT processor

The LL sub-band represents an approximation of the original image, the LL1 sub-band can be considered as a 2:1 sub-sampled version of the original image. The other three sub-bands HL1, LH1, and HH1 contain higher frequency detail information. This process is repeated for as many levels of decomposition as desired. The JPEG2000 standard specifies five levels of decomposition [21], although three are usually considered acceptable in hardware. In order to extend the 1-D filter to compute 2-D DWT in JPEG2000, two points have to be taken into account: Firstly, the 1-D DWT generates the control signal memory to compute 2-D DWT and manages the internal memory access. Secondly, we need to store temporary results generated by 2-D column filter. The amount of the external memory access and the area occupied by the embedded internal buffer are considered the most critical issues for the implementation of 2D-DWT. As the cache is used to reduce the main memory access in the general processor architectures, in similar way, the internal buffer is used to reduce the external memory access for 2D-DWT. However, the internal buffer would occupy much area and power consumption.

V. PROPOSED ARCHITECTURE

The column processor can be regarded as a 1-D DWT processor acting on the column-wise image data. The proposed column processor [2] is optimized in terms of the arithmetic cost and processing speed. Fig. 4.3 plots the detailed data flow graph (DFG) for Eq. (3.18), which represents the calculations of one lifting step in the modified algorithm. The processor reads one input sample in each cycle, and then multiplies it by the corresponding coefficient in the following cycle. After each input datum is multiplied, the rest of the calculation only requires several addition operations.

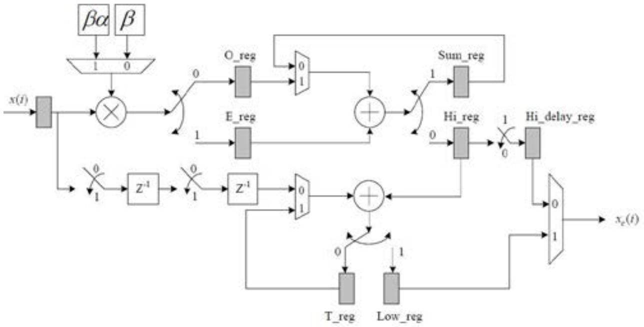


Figure 4.2: 1-D DWT architecture for column Processor

The timing diagram of the DFG in figure 4.3, shows that only one multiplier and two adders are needed at each clock cycle for the computations, and thecritical path between the pipeline registers is mainly limited by one multiplier delay.

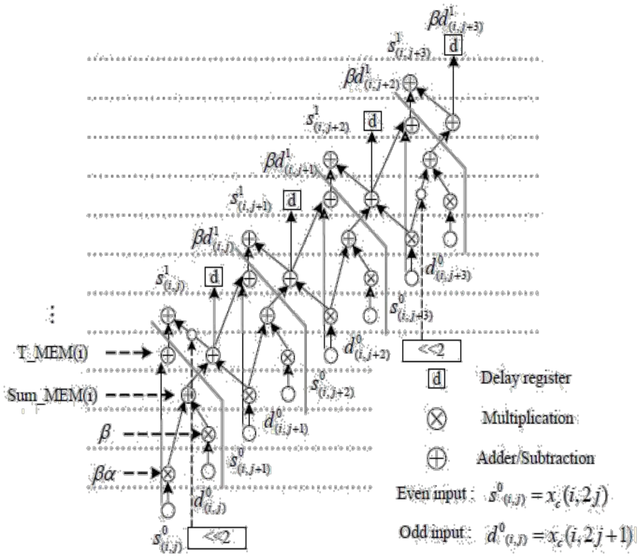


Figure 4.3: The data path of the i-th column-wise transform

The row-wise transform can be considered as the transpose of the column process and is easy to perform in principle. In the hardware implementation, to reduce the internal memory requirement, the column-processed data have to be executed as soon as possible. Moreover, the internal memory size of row processor highly depends on the pipeline registers of 1-D architecture. The trade-off between high speed and less memory is an important issue for the 2-D DWT architecture. Based on the modified algorithm, the column-processed data can be partially executed todecrease the internal memory size. Fig. 4.7 indicates the i-th row-wise data path of the modified DWT algorithms. Once two column processed data are collected, the i-th row-wise transform is then partially performed and the results are temporarily stored in the “Sum_MEM (i)” and “T_MEM (i)”, where the index i is from 0 to N-1. That is, “Sum_MEM (i)” and “T_MEM (i)” are used to preserve the data path of each row transform and the data path is updated by the two new input data.

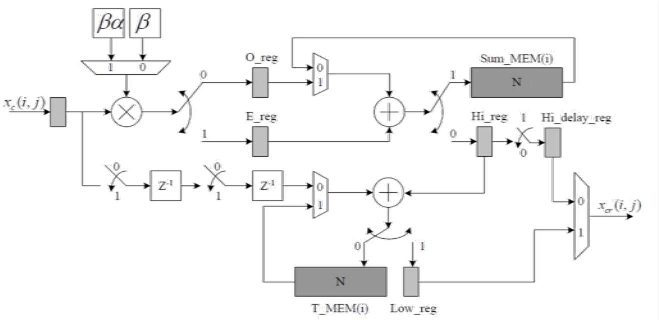


Figure 4.4: 1-D DWT architecture for Row processor

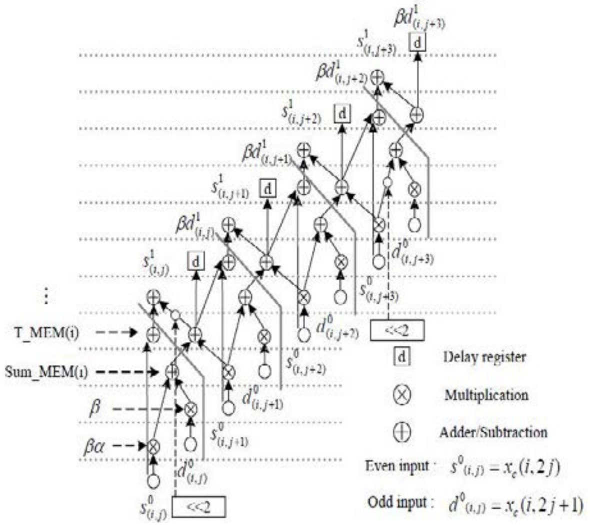


Fig. 4.5 The data path of the i-th column-wise transform

VI. SIMULATION AND RESULTS

This section deals with the simulation of Column Processor and Row Processor in XILINX ISE Simulator as well as in MATLAB showing the 2nd level decomposition of image on application of 2D- DWT. The VHDL simulation of all the components used in Row Processor has been described here. The simulated architecture of column processor has also been described here.

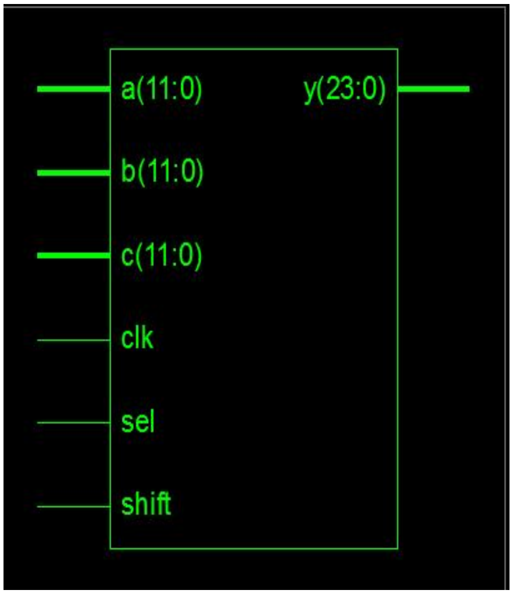


Figure 5.1: Schematic Symbol of Column Processor in Xilinx

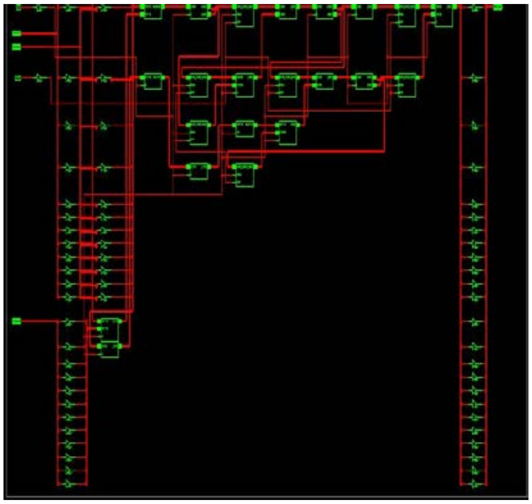


Figure 5.2: Technology Schematic of Column Processor in Xilinx

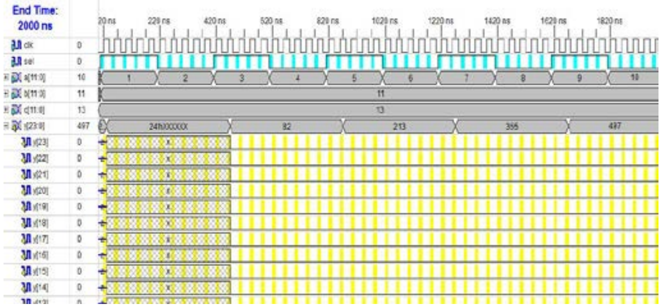


Figure 5.3: Test Bench Waveform of 12 Bit Column Processor.

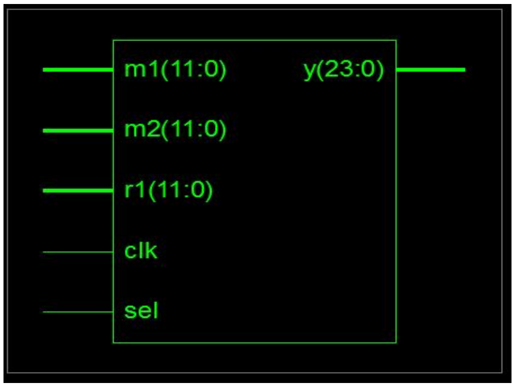


Figure 5.4: Schematic Symbol of 12 Bit Row Processor in Xilinx

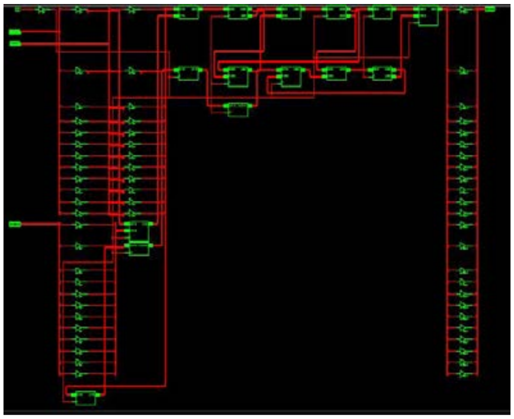


Figure 5.5: Technology Schematic of 12 Bit Row Processor in Xilinx

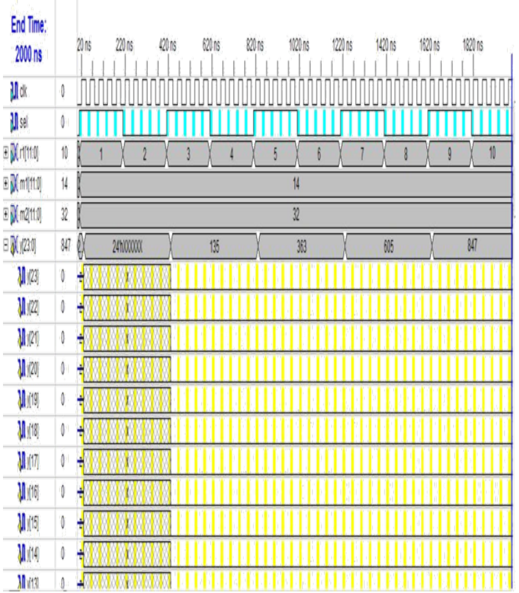
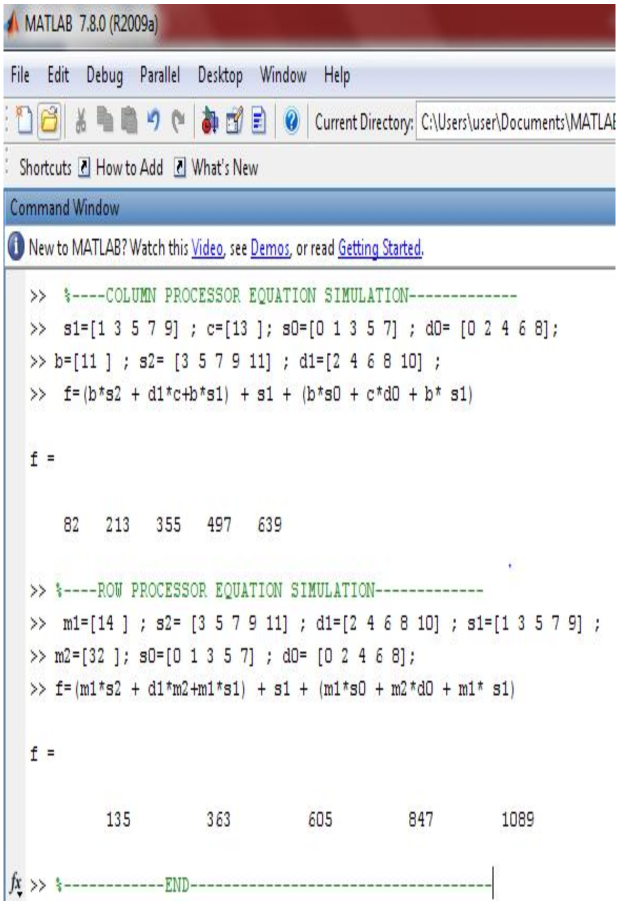


Figure5.6: Technology Schematic of 12 Bit Row Processor in Xilinx


MATLAB 7.8.0 (R2009a)
File
Edit
Debug
Parallel
Desktop
Window
Help
Current Directory: C:\Users\user\Documents\MATLAB
Shortcuts
How to Add
What's New
Command Window
New to MATLAB? Watch this Video, see Demos, or read Getting Started.

```
>> %----COLUMN PROCESSOR EQUATION SIMULATION------------
>>  s1=[1 3 5 7 9] ; c=[13 ]; s0=[0 1 3 5 7] ; d0= [0 2 4 6 8];
>> b=[11 ] ; s2= [3 5 7 9 11] ; d1=[2 4 6 8 10] ;
>>  f=(b*s2 + d1*c+b*s1) + s1 + (b*s0 + c*d0 + b* s1)

f =

    82   213   355   497   639

>> %----ROW PROCESSOR EQUATION SIMULATION------------
>>  m1=[14 ] ; s2= [3 5 7 9 11] ; d1=[2 4 6 8 10] ; s1=[1 3 5 7 9] ;
>> m2=[32 ]; s0=[0 1 3 5 7] ; d0= [0 2 4 6 8];
>> f=(m1*s2 + d1*m2+m1*s1) + s1 + (m1*s0 + m2*d0 + m1* s1)

f =

         135         363         605         847        1089

>> %-----------END-----------------------------------
```

Figure5.7: Result of CP and RP equation (3.12) simulation in MATLAB

VII. CONCLUSION

The Discrete Wavelet Transform provides a multiresolution representation of signals. The transform can be implemented using filter banks. This report presents thesimulation work for column processor, transposing bufferand row processor of 2D DWT architecture for JPEG 2000and the study of high-performance and low-memory pipeline architecture for 2-D lifting-based DWT of the 5/3and 9/7 filters. By merging the predictor and updater into one single step, we can derive efficient pipeline architecture [2]. Hence, given the same number of arithmetic units, the given architecture has a shorter pipeline data path .In this thesis, architectures for the Lifting based Discrete Wavelet Transform have been implemented. For each of them, parameters such as memory requirement and speed were discussed. Based on the application and the constraints imposed, the appropriate architecture can be chosen. The simulation results verify the functionality of the design. The proper scheduling of the wavelet coefficients to the Transposing Buffer ensures that, when the coefficients are finally read back from the Transposing Buffer, they are available in the required order for further processing by Row Processor. The proposed architecture [2] is simple since further levels of decomposition can be achieved using identical processing elements. The architecture enables fast computation of DWT with parallel processing. It has low memory requirements and consumes low power. Finally, the 5/3 and 9/7 filters with the different lifting steps can be realized by cascading the three key components. A better architecture is obtained by replacing the multiplier of architecture with Baugh Wooley multiplier to make it computationally faster and lesser memory storage requirement.

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