

# An Extensive Review on Reversible Logic in VLSI

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*Abstract—As of late reversible rationale has risen as a guaranteeing processing model for provisions in scattering less optical registering, low power CMOS, quantum figuring, and so on. In reversible circuits there exist a coordinated mapping between the inputs and the yields bringing about no misfortune of data. Analysts have actualized reversible rationale doors in optical processing area as it can give fast and low vitality prerequisite alongside simple creation at the chip level. Reversible rationale is generally being recognized as the potential rationale outline style for usage in cutting edge nanotechnology and quantum processing with negligible effect on physical entropy. Late developments in reversible rationale take into account enhanced quantum machine calculations and plans for comparing workstation architectures. Huge commitments have been made in the writing towards the outline of reversible rationale door structures and number-crunching units, notwithstanding, there are relatively few deliberations steered towards the configuration of reversible Alus. In this paper, we propose the configuration of two programmable reversible rationale entryway structures focused at ALU execution and their utilization in the acknowledgment of a proficient reversible ALU is exhibited. The proposed ALU outline is checked and its favorable circumstances over the main existing ALU configuration are quantitatively dissected.*

**Keyword – Arithmetic Logic Unit; Carry Look-Ahead Adder; Carry-Select Adder; Emerging Technologies; Low Power; Nanotechnology; Reversible Logic; Ripple-Carry Adder.**

## I. INTRODUCTION

Sensible processing gadgets without a bijection between information and yield states were showed via Landauer to oblige a negligible high temperature era of  $kT \ln(2)$  joules of vitality for every figuring cycle [1]. This ensuing scattered hotness likewise causes commotion in the remaining hardware, which brings about processing lapses. Bennett demonstrated that the dispersed vitality specifically associated to the amount of lost bits, and that machines might be sensibly reversible, keep up their straightforwardness and give precise computations at reasonable paces [2]. Resultantly, another standard in machine plan emerged with the objective of decreasing the entropy increment and consequent vitality dissemination. Such a sensible structure must have the same number of inputs and one-to-one

mapping between the info and yield states. Any gadget intended to these requirements is known as a reversible rationale gadget. The door utilized within expected circuit or advanced planning is irreversible (aside from NOT entryway) that methods the data can't be followed from yield. For instance the AND entryway, OR door, NAND entryway and so on are irreversible doors. A door is reversible in the event that it has equivalent number of inputs and yields and the Boolean work that maps the info in yield is bijective.

Reversible rationale has developed a critical approach in low power CMOS VLSI plan. A door is said to be Reversible if there is one of a kind yield duty for every unique data i.e. not just the yield could be dead set from info additionally inputs might be repeated from yields. Essentially it doesn't detached data so scatters less hotness. A rationale door M is said to be Reversible if, for any yield O, there is an exceptional data I that is:

$$L(I) = O$$

If a gate M is reversible, there is an inverse gate L' which maps O to I for which

$$L'(O) = I$$

Where I and O are the input and output vectors respectively. Many Reversible logic gates have been designed in past years. Commonly used gates are Feynman gate, Toffoli gates, Fredkin gates, Peres gates, New Gates, TSG gates, MKG gates, HNG gates, PV gates etc.

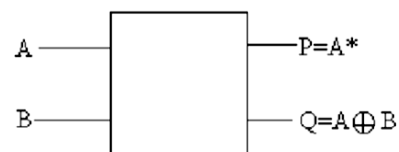


Fig. 1: A Reversible gate with one garbage output

To overcome the force utilization generated by irreversible legitimate operation reversible rationale acquires a critical consideration VLSI engineering. Reversible rationale can possibly have different provisions like low power utilization entryway plan, DNA registering, quantum processing, nanotechnology and so on. The significant imperatives in

outlining Reversible rationale door are refuse yield, which can't be utilized as essential yield and information to the next entryway.

## II. REVERSIBLE LOGIC

### A. Programmable Reversible Design Goals

The three major design goals of reversible logic are as follows. First, minimization of the quantum cost - the number of 1\*1 and 2\*2 reversible calculations necessary to generate the logical output [3] - will reduce the device's computational complexity. Second, minimization of the delay - the logical depth of the device [4] - will improve the throughput of the device. Third, reduction of the ancillary inputs and garbage outputs - inputs and outputs not implemented in the design of the gate and only serve to maintain reversibility of the device - will improve the design space require to implement the logic. A programmable reversible logic gate is defined in [5] as a logic structure which possesses a bijection between input and output states and an equal number of inputs and outputs wherein a subset of the inputs are fixed select lines, and a fixed subset of the output produce guaranteed logical calculations.. An perfect programmable reversible logic gate with j inputs and outputs has a quantity of fixed select the inputs m, fixed select outputs n, data inputs d and propagated outputs p such that |d-p|=|m-n| [5]. In addition, an ideal programmable reversible logic gate with m select inputs may produce at maximum  $n \cdot 2^m$  logical calculations on the n logical outputs [5].

### B. Fundamental Logic Gates

There are three types of fundamental 2\*2 reversible logic gates. First, the square-root-of-not gates utilize the unitary operators to produce reversible logic calculations. The Controlled-V and the Controlled-V+ gates are the two types of square-root-of-not gates. In both of these gates, when the control input is the 0, the second input is propagated to the output. The corresponding unitary operator is propagated to the second output when the control input is 1, where the unitary operation is for the Controlled-V gate

$$V = \frac{i+1}{2} \begin{pmatrix} 1 & -i \\ -i & 1 \end{pmatrix}$$

and for the Controlled-V+ gate.

$$V^+ = \frac{1}{i+1} \begin{pmatrix} 1 & -\bar{1}/i \\ i & 1 \end{pmatrix}$$

When two Controlled-V gates are activated in series, they act as an inverter. The same holds for two Controlled-V+ gates in series. When a Controlled-V and Controlled-V+ gate are activated in series, they act as an identity. The second type of fundamental 2\*2 reversible-logic gate is the Feynman gates, or the Controlled-Not gates. Proposed in [6] by Feynman, it is configured such that its outputs states correlate to the input states in the following manner: P=A. The resulting value of the second output corresponds to the result of a conventional XOR gate. Since fan-out is expressively forbidden in reversible logic, since a fan-out has one input and two outputs, the Feynman gates may be used to duplicate a signal when B is equal to 0. Its quantum configuration is shown in Fig 2.



Fig 1: Quantum Representation of the Feynman gate

The third type of fundamental 2\*2 reversible logic gates is the integrated qubit gate. This gate is implemented with a Feynman gate with either a Controlled-V or Controlled V+ gate. The XOR output of the Feynman gate is used as the control signal for the Controlled-V or V+ gate it is coupled with. The quantum cost of the integrated qubit gate is 1 and its worst-case delay is 1. The quantum configurations of these gates are shown below in Fig. 3.

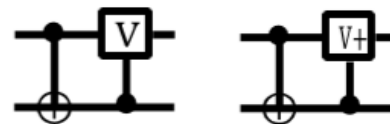


Fig 3: Quantum Representations of Integrated Qubit Gates

## III. LITERATURE REVIEW

Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan [7] The two new reversible entryways ORG-I and ORG- II are proposed as they can execute a reversible viper with lessened optical expense which is the measure of number of Mzis switches and the spread deferral, and with zero overhead regarding number of ancilla inputs and the waste yields. The proposed all optical reversible viper outline focused around the ORG-I and ORG-II reversible doors are contrasted and indicated with be superior to the next existing outlines of reversible snake proposed in non-optical space regarding number of Mzis, deferral, number of ancilla inputs and the rubbish yields. The proposed all optical reversible

swell convey snake will be a key segment of an all optical reversible ALU that could be connected in a wide mixed bag of optical indicator preparing requisitions.

Bibhash Sen, Manojit Dutta, Debajyoty Banik, Dipak K Singh, Biplab K Sikdar [8] This work targets outline of reversible ALU (arith- metic rationale unit) in QCA (Quantum-dab Cell Automata) system. The outline is focused

around the reversible QCA structure (RQCA) presented in this paper. An issue tolerant structural planning of reversible ALU is likewise combined. The proposed plans are verified and assessed over the current ALU outlines and discovered to be more proficient regarding outline multifaceted nature and quantum cost.

Table 1: Summary of Literature Review

Year	Author	Title	Approach	Result
2012	Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan,	Mach-Zehnder Interferometer Based Design of All Optical Reversible Binary Adder	Optical reversible ripple carry adder	ALU that can be applied in a wide variety of optical signal processing applications
2012	Bibhash Sen, Manojit Dutta, Debajyoty Banik, Dipak K Singh, Biplab K Sikdar,	Design of Fault Tolerant Reversible Arithmetic Logic Unit in QCA	Design of reversible ALU (arith- metic logic unit) in QCA (Quantum-dot Cellular Automata) framework	More efficient in terms of design complexity and quantum cost
2011	Y. Syamala A. V. N. Tilak	Reversible Arithmetic Logic Unit	Design of a reversible Arithmetic Logic Unit (ALU)	Number of garbage outputs and constant inputs produced
2011	Matthew Morrison, Matthew Lewandowski and Richard Meana	Design of a Novel Reversible ALU using an Enhanced Carry Look- Ahead Adder	Reversible logic allow schemes for computer architectures	Novel programmable reversible logic gate is presented and verified
2010	Anindita Banerjee	Reversible cryptographic hardware with optimized quantum cost and delay	Reversible hardware cryptography	Optimize quantum cost and delay

Y. Syamala, A. V. N. Tilak [9] a capacity is reversible if each one information vector generates a special yield vector. Reversible rationale is of developing imperativeness to numerous future workstation innovations. In this paper, the outline of a reversible Math Rationale Unit (ALU) is displayed making utilization of multiplexer unit and additionally control signs. ALU is a standout amongst the most paramount segments of CPU that could be some piece of a programmable reversible figuring gadget, for example, a quantum workstation. In multiplexer based ALU the operations are performed relying upon the choice line. The control unit based ALU is produced with 9n basic reversible doors for four fundamental number-crunching coherent operations on two n-bit operands. The arrangement of operations are performed on the same line relying upon control signs, as opposed to selecting the craved come about by a multiplexer. The later outline is discovered to be

profitable over the previous regarding number of waste yields and steady inputs handled.

Matthew Morrison, Matthew Lewandowski, Richard Meana and Nagarajan [10] In this work, a novel programmable reversible rationale door is introduced and confirmed, and its execution in the configuration of a reversible Math Rationale Unit is exhibited. At that point, reversible executions of swell convey, convey select and Kogge-Stone convey look-ahead adders are investigated and thought about. Next, usage of the Kogge-Stone viper with sparsity-4, 8 and 16 were composed, checked and thought about.

Anindita Banerjee [11] so as to shield the force examination ambush reversible rationale is a great applicant as it in a perfect world does not disperse any high temperature and today reversible rationale is a developing exploration territory. In writing diverse outlines for reversible equipment

cryptography have been proposed yet they have been actualized utilizing complex entryway libraries and further hypotheses have been proposed defining more level farthest point of usage expense which is quantum taken a toll. We have proposed novel outlines for reversible ALU of a crypto processor which have been executed in standard entryway library and the quantum expense reported here are superior to the more level limits reported in writing. Further we have figured deferral of the proposed plans. We have verified that our proposed plans are insignificant as for entryway tally which is circuit fetched by mimicking it in Revkit. This is for the first time that the advancement calculations to upgrade quantum cost and deferral have been connected to ad lib on the expense metric in reversible ALU.

#### IV. CONCLUSION

Reversible logic is gaining significant consideration as the potential logic design style for execution in cutting edge nanotechnology and quantum processing with negligible effect on physical entropy. Late developments in reversible rationale permit plans for machine architectures utilizing enhanced quantum workstation calculations. Critical commitments have been made in the writing towards the configuration of reversible rationale entryway structures and number juggling units, be that as it may, there are very few exertions controlled towards the outline of reversible Alus. In this work, a narrative programmable reversible rationale entryway is displayed and checked, and its usage in the outline of a reversible Number-crunching Rationale Unit is exhibited. At that point, reversible executions of swell convey, convey select and Kogge-Stone convey look-ahead adders are broke down and analyzed.

#### REFERENCES

- [1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process," IBM Journal of Research and Development, vol. 5, 1961, pp. 183-91.
- [2] C. Bennett, "Logical Reversibility of Computation," IBM Journal of Research and Development, vol. 17, 1973, pp. 525-532.
- [3] T. Toffoli, "Reversible Computing," Technical Report MIT/LCS/TM- 151, 1980.
- [4] A. Peres, "Reversible Logic and Quantum Computers," Physical Review, vol. 32, iss. 6, 1985, pp. 3266-3267.
- [5] M. Morrison and N. Ranganathan, "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," To Appear in the IEEE International Symposium on VLSI, 2011.

- [6] R. Feynman, "Quantum Mechanical Computers," Foundations of Physics, vol. 16, iss. 6, 1986,
- [7] Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan, "Mach-Zehnder Interferometer Based Design of All Optical Reversible Binary Adder" 2012 IEEE.
- [8] Bibhash Sen, Manojit Dutta, Debajyoty Banik, Dipak K Singh, Biplab K Sikdar, "Design of Fault Tolerant Reversible Arithmetic Logic Unit in QCA" 2012 International Symposium on Electronic System Design.
- [9] Y. Syamala, A. V. N. Tilak, "Reversible Arithmetic Logic Unit", 2011 IEEE.
- [10] Matthew Morrison, Matthew Lewandowski, Richard Meana and Nagarajan Ranganathan, "Design of a Novel Reversible ALU using an Enhanced Carry Look- Ahead Adder" , 2011 11th IEEE International Conference on Nanotechnology Portland Marriott August 15-18, 2011, Portland, Oregon, USA
- [11] Anindita Banerjee , "Reversible cryptographic hardware with optimized quantum cost and delay" 2010 Annual IEEE India Conference (INDICON).

#### Author's Profile



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