High Performance Binary To BCD Converter For Decimal Adder

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Abstract--In view of increasing distinction of commercial, economic and Internet-based applications that process data in decimal arrangement. In this paper, a new architecture decimal addition of binary coded decimal (BCD) operands, which is the main design part of high speed low power multi-operand binary adders Based on this add-3 digit BCD adder, new architectures for higher order (n-digit) BCD adders such as ripple carry adder are developed. The proposed circuits are compared (both qualitatively as well as quantitatively) with the obtainable circuits. Simulation results show that the proposed add-3 digit BCD adder realizes an improvement of 50% in delay. shown to achieve at least 70% faster than the obtainable ripple carry one.

key words-- BCD adder,add-3 algorithm ,binary to bcd convertor, decimal arithmetic.

I INTRODUCTION

Decimal Arithmetic is receiving significant attention in commercial business and internet based Applications, providing hardware support in this direction is henceforth necessary.

Improving BCD architectures, to enable faster and compact arithmetic. In this paper we introduce a new architecture for binary to BCD Conversion of partial

Products which forms the core of decimal multiplication algorithms such as [7] and [8]. The

speedup, area reduction and power consumption of the proposed architecture is analyzed and comparisons

With recent architectures is provided. The current state of art conversion scheme [7] is studied and Irregularities in the implementation of their converter will be discuses. The results show that the proposed design brings significant improvement in terms of delay , area and power consumption.

In general binary numbering system is, remotely the most ordinary numbering system in use in computer systems application in this scenario. In days Because of there were all the computer systems that were based on the decimal numbering system moderately than the binary numbering system. This type of computer systems were very trendy in systems usually or for business/marketable/commercial application .And internet supported applications, regular though systems designers have recognize that binary arithmetic is not quite always better than the decimal arithmetic for general calculation and application the parable still continue that decimal arithmetic is better for rupees calculations and some general purpose application than binary arithmetic. This feature is for the most part valuable when working with fractional values since fixed and floating point binary representations cannot exactly represent many applications . From a VLSI design perspective, this is the easiest adder to implement. One just needs to design and lay out one FA cell, and then array N of these cells to create an N-bit RCA.

Ripple carry adder O(N) = 2n

For a k-bit RCA worst case path delay is

$T_{RCA\text{-}k\ bit} = T_{FA}(x_0, y_0\ c_0) + (k-2) * T_{FA}(C_{in}\ Ci) + T_{FA}(C_{in}\ S_{k-1}$

Complexity and Delay for n-bit RCA structure

$A_{RCA} = O(n) = 7n$

$T_{RCA} = O(n) = 2n$

II. RELATED WORK

Shift the binary numbers left one by bit. In the proposed algorithm shifting is done by 16 bit shifts, and the binary coded decimal number divided in the Five category ten thousand, thousand , Hundreds, Tens, and Units column. So If the binary number in any of the columns is five or greater than five , then add 3 algorithm applied to that value in that

binary coded decimal column. Otherwise Go to 1.table 1 show method that how to take bits and shift into, ten thousand, thousand hundred , units ,tens column and how to add 3 procedure apply

The algorithm then iterates number of times. On each iteration, the integral graze space is left-shifted one bit. However, before the left-shift is done, any BCD digit which is greater than 4 is incremented by 3. The increment ensures that a assessment of 5, incremented and left-shifted, becomes 16 thus correctly "moving" into the next BCD digit. Show in Table1.1 show how to shift bit.

Operation	Tens	Units	Binary
HEX			E
Start			1 1 1 0
Shift 1		1	1 1 0
Shift 2		1 1	1 0
Shift 3		1 1 1	0
Add 3		1 0 1 0	0
Shift 4	1	0 1 0 0	
BCD	1	4	

Table1.1 show how to shift bit

Fig. 1.1 show the Conversion flow chart for 16 bit binary to BCD Conversion

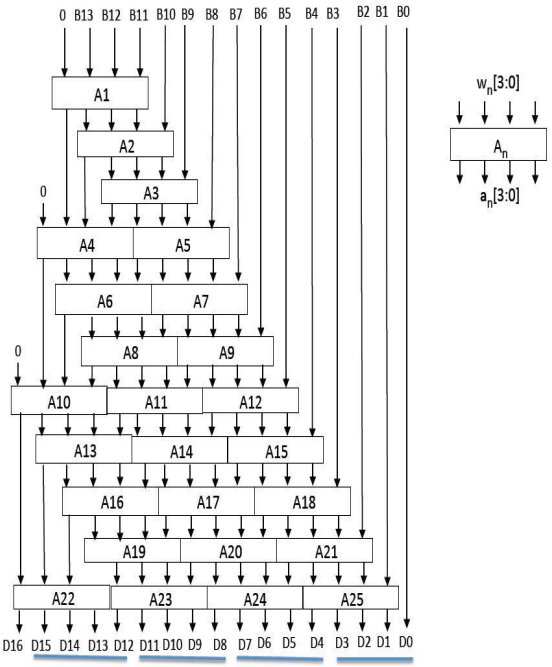

Fig .1 Conversion flow chart for 16 bit binary to BCD Conversion

III PROPOSED ALGORITHM

The main goal of the proposed algorithm is to perform greatly proficient fixed bit binary to BCD conversion in terms of delay ,power and area. As mentioned earlier, most of the recently proposed adder use 16-bit binary to BCD converters.

The proposed algorithm has been purposely designed for such converters. The following subsection explains the proposed algorithm.

The algorithm then iterates number of times. On each iteration, the entire space is left-shifted by one bit. on the other hand, before the left-shift is done, any BCD digit which is greater than 4 is incremented by 3. The increment ensures that a assessment of 5, incremented and left-shifted, turn out to be 16, thus appropriately "carrying" into the next BCD digit, this algorithm is tradition but proposed architecture integrate each bcd bits also overcome the area required and get enhanced speed as conventional adder fig.3 shown RTL view of synthesize 16 bit bcd to binary code

IV BINARY TO BCD CONVERTER

All the 16 bit Binary to BCD converters and add and shift structures were described using VHDL data flow modeling and simulated using Simulator (Isim) 14.7. simulator tool The Binary to BCD converters and Multi-operand implemented and planned on, RTL Compiler on 14.7(I- sim simulator tool). All the inputs were position to have a clock rate of 100%. binary to bcd structures based on the proposed algorithm were designed and the Binary to BCD converter in the proposed algorithm was replaced with that of architecture[8] for the comparisons. Table III shows the comparison of Binary to BCD converter with existing design [8]. Synthesis results show that there is a reduction in delay by 55 % with a tradeoff in power by 18 %. This in turn reduces power delay by 27 % and Total REAL time to Xst completion: 1.00 sec .Total CPU time to Xst completion:0.10 sec.

V ADDER IMPLEMENTATION

Implementation of 16 bit BINARY TO BCD Converter using add -3-addition ripple carry adder has been done using Xilinx 14.1 and simulator has carried out by lSim 14.1e tool. Fig .2 show 16 bit binary to BCD input RTL View RTL Compiler on 14.7(I- sim simulator tool).RTL view of 15 bit binary to bcd converter binary_ in,clk,rst

are inputs which is going to (N-1 downto 0) bcd0, bcd1, bcd2, bcd3, bcd4: are outputs

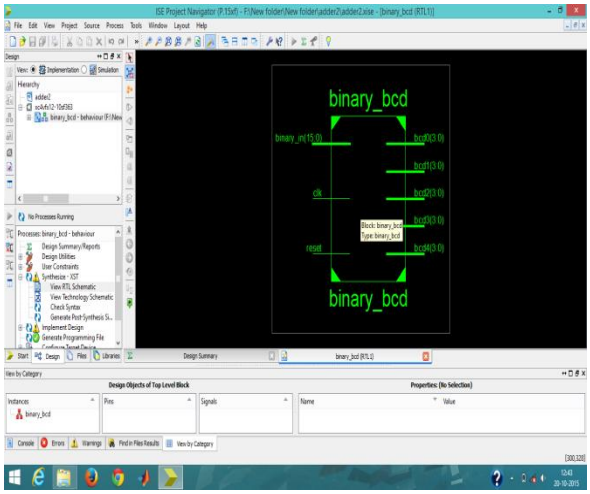

Fig .2 Conversion 16 bit binary to BCD

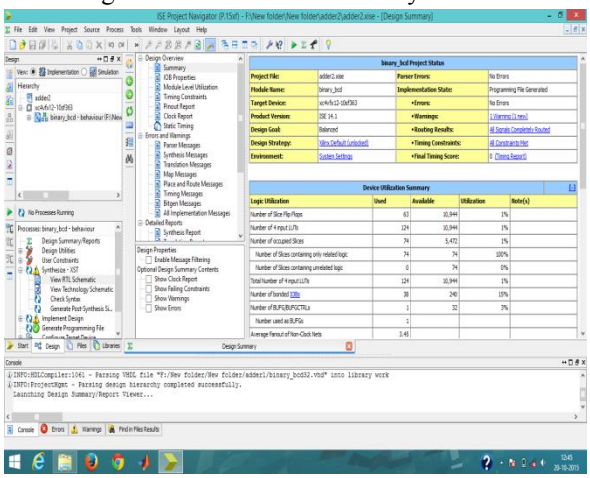

Fig .3 show 16 bit binary to BCD Synthesized Report Using the FPGA editor and Floor planner of the ISE the system can be made more efficient in terms of space acquired when deployed on a real hardware chip.

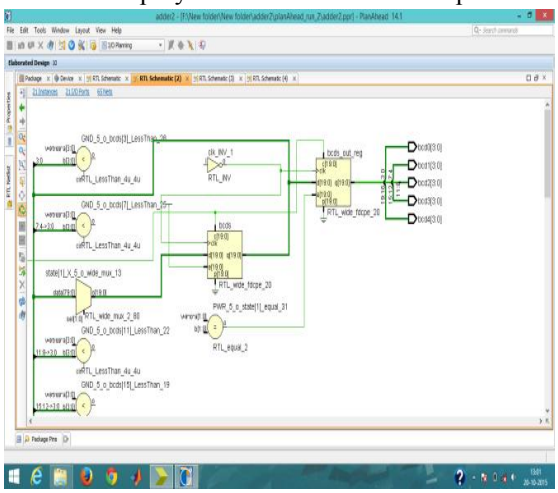

Fig .3 show 16 bit binary to BCD FGPA floor plan

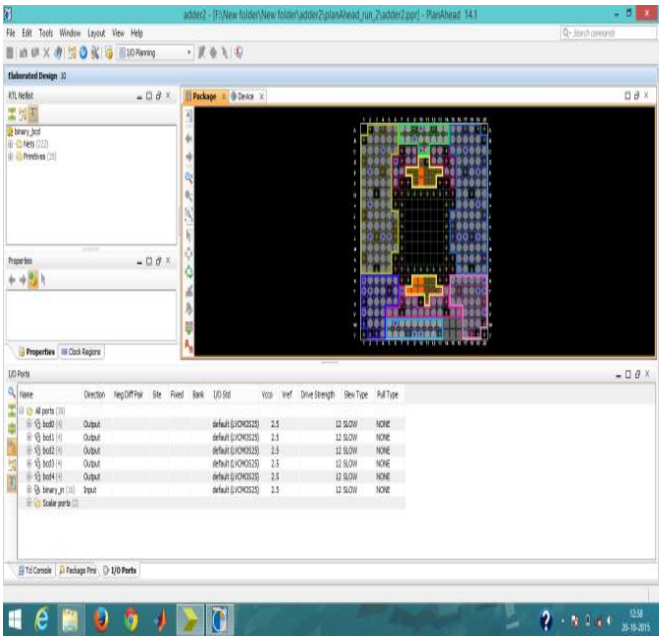

Fig .4 show 16 bit binary to BCD FPGA Floor Plan

Fig. 5 shown the technical RTL view of 16 bit

binary to bcd converter

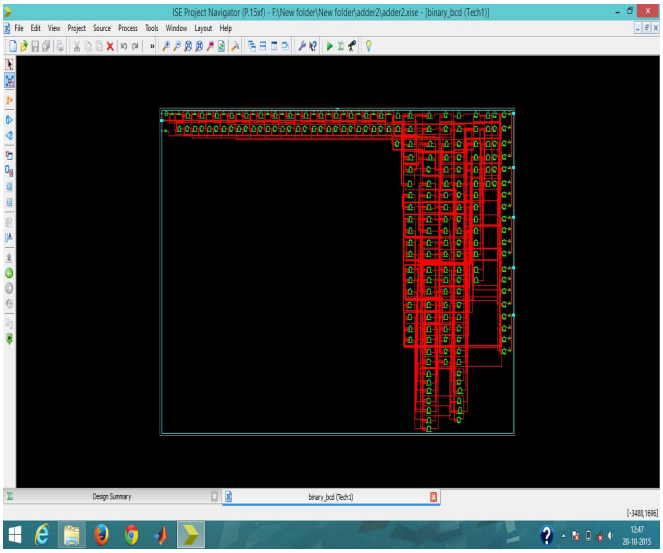

Fig. 6 shown the technical RTL view of 16 bit binary to bcd converter

IV. SIMULATION RESULTS

Total memory usage is 537168 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 4 (0 filtered)
Number of infos : 0 (0 filtered)

Maximum combinational path delay: 2.710ns secs . from these three designs, the proposed multi-operand adder in concurrence with modified binary to bcd adder using add-3 [3] gives better performance in terms speed as well as power and delay product. Further it is evident from Table II that the proposed design performs better compared to [4] with respect to delay as well as power delay product Comparison Of Proposed add-3 Adder With customized hundred And units and tens– Four Split [8] Adders All the 16 -bit Binary to BCD converters and Multioperand adder structures were described using VHDL data flow modeling and simulated using Simulator (Isim) 14.7. The Binary to BCD converters and Multi-operand designs . All the inputs were set to have a clock rate of 100%. Binary to bcd structures based on the proposed algorithm were designed and the Binary to BCD converter in the proposed algorithm was replaced with that of architecture [8] for fair comparisons. Table 2 shows the comparison of Binary to BCD converter with existing design [8]. Synthesis results show that there is a reduction in delay by 65 % with a tradeoff in power by 18 %. This in turn reduces power delay by 27 % and Minimum period: 2.600ns (Maximum Frequency: 384.645MHz) & Minimum input arrival time before clock: 2.765ns & Maximum output required time after clock: 4.714ns Maximum combinational path delay: No path found

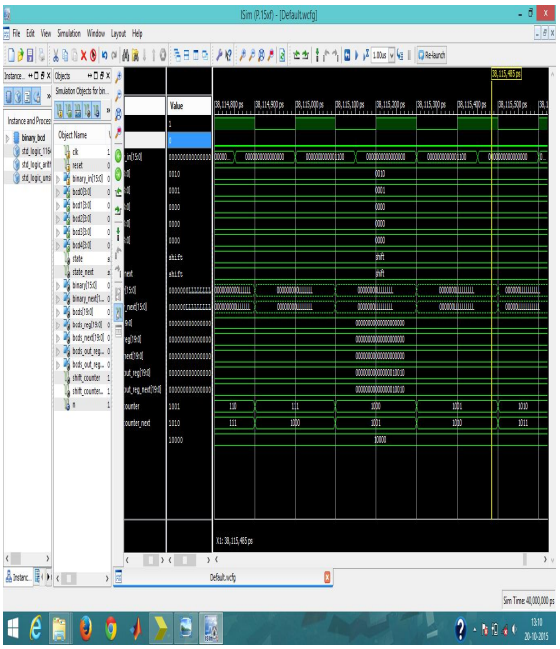

Fig.7 shown . simulation wave form for16 bit binary to bcd converter

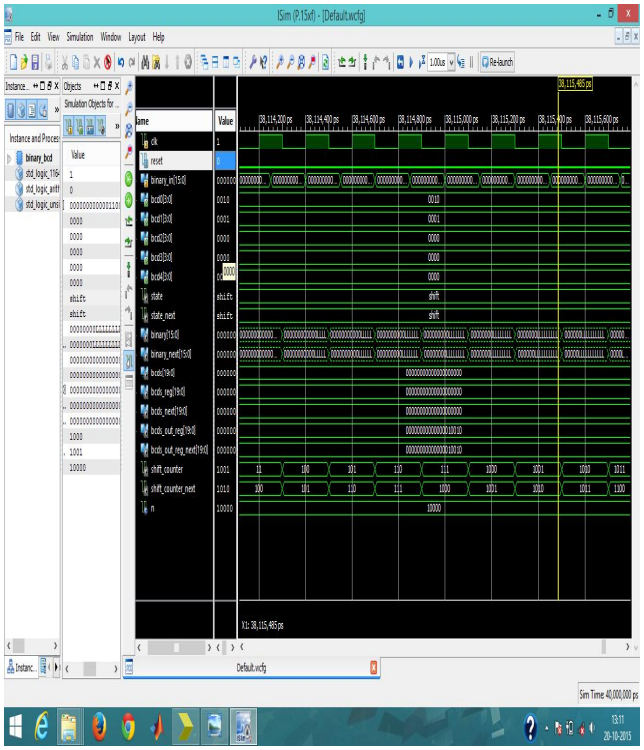

Fig. 7 simulation wave form for16 bit binary to bcd converter

COMPARISON TABLE

Metric	Area (μm2)	Delay (ns)	Power (nw)	Power Delay product
Proposed design	89.90%	2.710ns	0.4714	0.397
Design [a]	50.40%	2600	0.185	0.358
Design[b]	10.80%	3.957	0.64	0.773

VI. CONCLUSIONS

A Novel integrated BCD/ Binary multi-operand addition algorithm has been proposed. The binary parallel multioperand addition is realized using by programmers to convert a binary number to decimal. It is performed by add 3 shift and add 3 algorithm, and can be implemented using a less number of gates in computer hardware,. The proposed binary to bcd converter forms the core of the multi-operand binary adder. Simulation results show the efficiency of our Proposed BD converter in addition to multi-operand decimal adder with respect to exiting designs.[10]

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