Efficient Delay Architecture of 32-Bit Multiplier Using Recursive Adder

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Abstract - Every digital circuit has some logic to perform which is basically an algorithm of frequent operations of addition, subtraction, division and multiplication to achieve a specific task. The repeated addition operation is nothing but multiplication. The speed of this repeated operation is highly depends on the structure of the adder and multiplier operation highly depends on the architecture of the adder. This paper shows the proposed optimum adder design and multiplier utilizing the adder architecture with better speed. The improved design is of 32-bit which has a delay of 38.739ns for performing multiplication operation which is 61% less than previous 32-bit multiplier design. The proposed recursive adder based multiplier design is implemented on Virtex 7 FPGA device.

Keywords - Recursive addition, 32-bit Multiplier, Delay, Area.

I. INTRODUCTION

As the scale of integration keeps growing with the advancement of technology, more and more sophisticated signal processing systems are being implemented on a single VLSI chip. These signal processing applications not only demand great capacity of computation but also consume significant amount of energy. While performance and Area remain to be the two major design tolls, power consumption has become a critical concern in today's VLSI system design. The need for low-power in VLSI systems arises from two main forces. First, with steady growth of operating frequency and processing capacity per chip, large amount of currents have to be delivered and heat due to large power consumption must be properly removed by proper cooling techniques. Second, battery life is limited in portable electronic devices. The designs utilizing low power directly leads to prolonged operation time in these portable devices. Multiplication is one of the fundamental operation in most of the signal processing algorithms. Multipliers consumes larger areas, have long latency and consume considerable amount of power. Hence low-power multiplier design has been an important part in low- power VLSI system design. There has been widespread work on low-power multipliers at technological, physical, circuital and logical levels. The performance of a system is generally determined by the performance of the multiplier because the multiplier is usually the slowest element in the system. Moreover, it is generally the most area consuming part of the circuit. Hence, optimization of the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in large consumption of areas. As a result, a whole spectrum of multipliers with different area and speed constraints has been designed with fully parallel multipliers.

The multipliers which are Fully Parallel are at one end of the spectrum and fully serial multipliers are at the end. In between these are digit serial multipliers in which single digits consisting of several bits are operated on. The performance of multiplier is moderate in both speed and area. However, existing digit serial multipliers have been overwhelmed by complicated switching systems and/or irregularities in design. Multipliers having radix 2^n which operate on digits in parallel examines the above problems. These structures are modular and iterative. The pipelining done at digit level brings the benefit of constant speed of operation irrespective of the multiplier's size. The speed of the clock is only determined by the digit size which is already fixed before the implementation of design.

A multiplier is generally one of the key hardware blocks in most digital and high performance systems which includes FIR filters, digital signal processors and microprocessors etc. With the advancement in technology, many researchers have tried and are trying to design the multipliers which offer either of the following- low power consumption, high speed, regularity of layout and therefore lesser area consumption or even combination of them in a single multiplier. Thus making the multipliers suitable for various low power, high speed, and compact VLSI implementations. However area and speed are two conflicting constraint. So improvement in speed results always in larger areas. So here we try to find out the best trade off solution amongst both of them. Generally as we know that multiplication goes in two basic steps. Firstly partial product is done and then addition.

Addition is the most common and frequently used arithmetic operation on digital signal processor, microprocessor, especially in case of digital computers. Also, it serves as a basic building block for the synthesis of all other arithmetic

operations. Therefore, regarding the efficient implementation of an arithmetic unit, binary adder structures become a very significant hardware unit. In any book which is on computer arithmetic, if someone looks that there exists a large number of different circuit architectures with different performance characteristics that are widely used in practice. Although many researches which deals with binary adder structures have been done, the studies based on their comparative performance analysis are only a few.

II. PROPOSED ARCHITECTURE

Multiplication Algorithm for 32 bit:

Let the product register size be 64 bits. Let the multiplicand registers size be 32 bits. Store the multiplier in the least significant half of the product register. Clear the most significant half of the product register.

Repeat the following steps for 32 times:

1. If the least significant bit of the product register is "1" then add the multiplicand to the most significant half of the product register.

2. Shift the content of the product register one bit to the right (ignore the shifted-out bit.)

3. Shift-in the carry bit into the most significant bit of the product register. Figure 4.Shows a block diagram for such a multiplier [2].

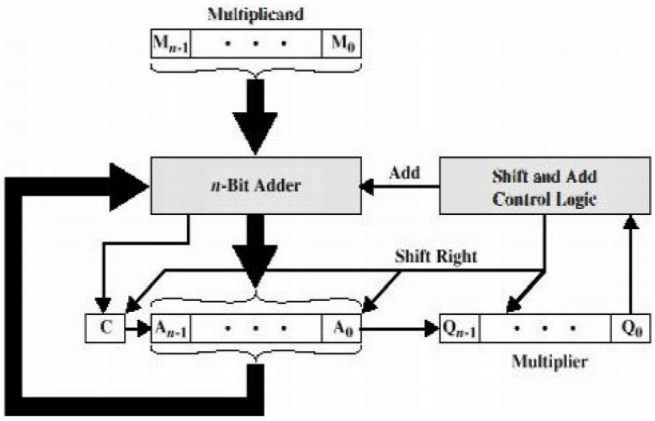

Fig. 2.1 Multiplier of two n-bit values

The proposed multiplier architecture using recursive adder and its schematic is shown in the figure below. Fig. 2.2 shows the schematic of the recursive adder architecture and Fig. 2.3 shows the schematic of the multiplier architecture.

The recursive adder utilizes the 4-bit addition logic recursively for 8 times to calculate 32-bit calculations. The recursive logic significantly reduces the delay of the calculations will also shown in the next section of the paper.

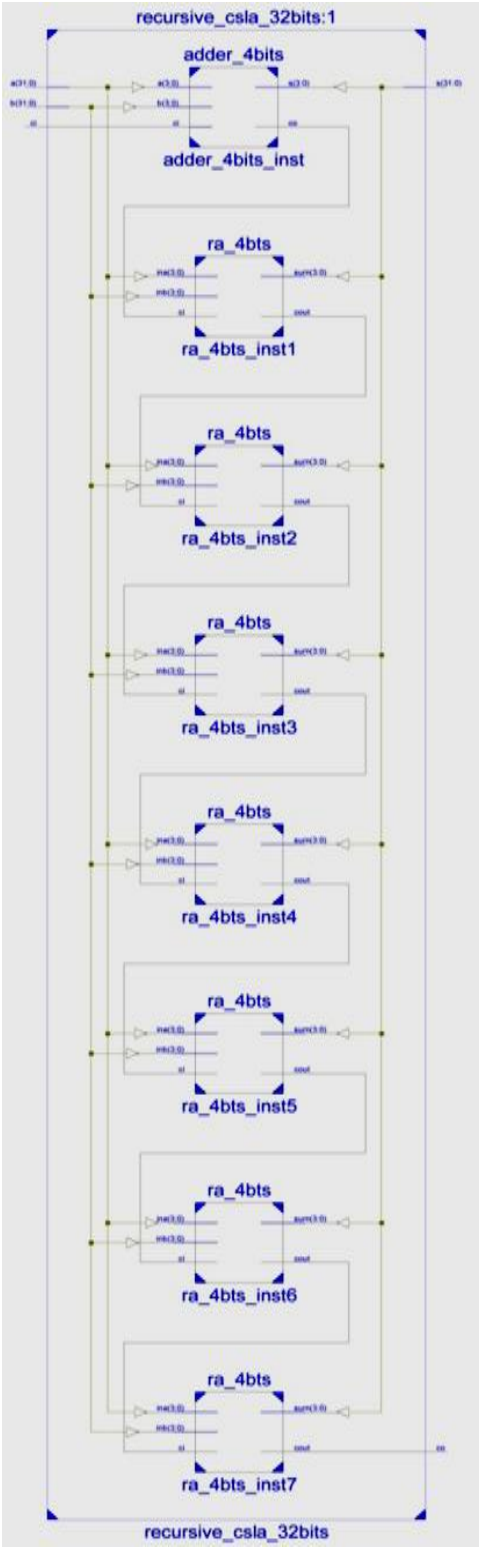

Fig. 2.2 RTL Schematic of Recursive Adder Design

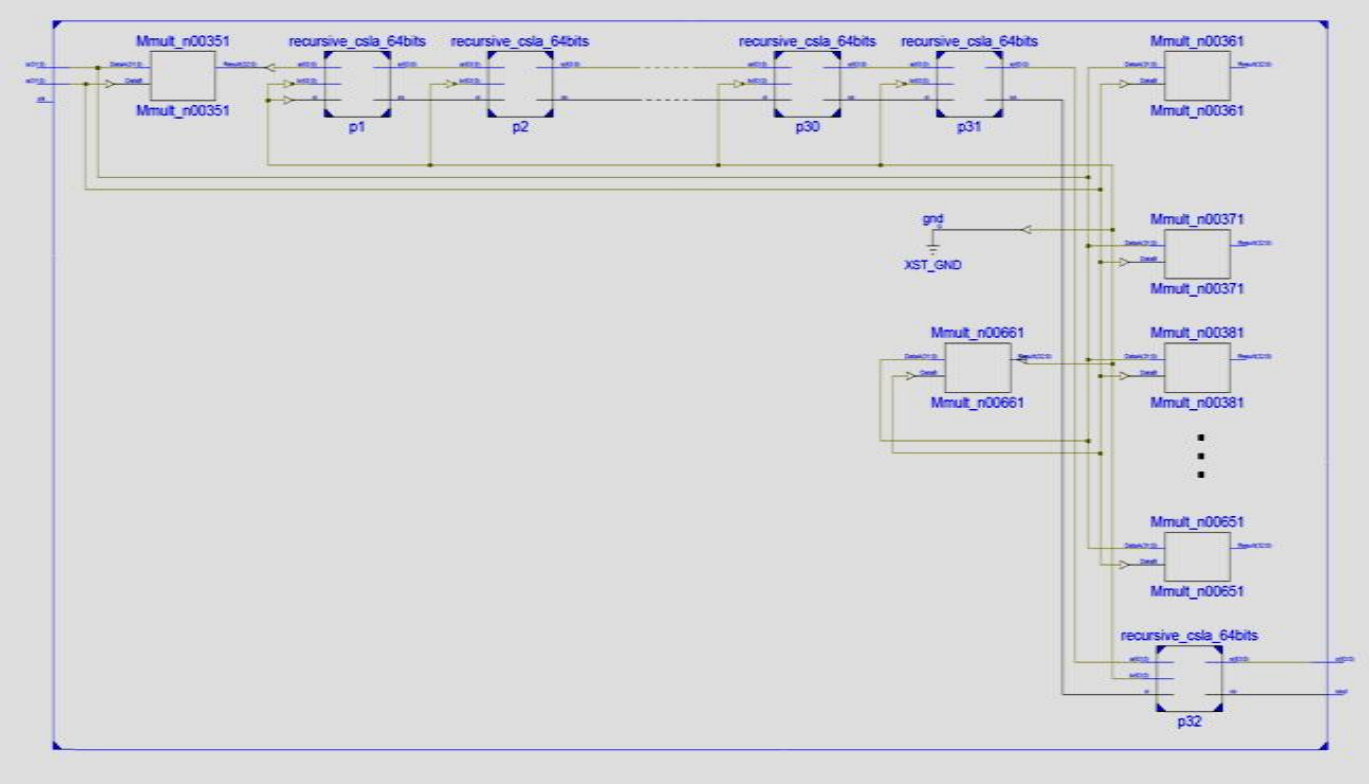

Fig. 2.3 RTL Schematic of Proposed Multiplier Design

III. SYNTHESIS RESULTS

The synthesis of the proposed design is done on the XILINX 13.1 using Virtex 7 FPGA device. The synthesis outcomes as test bench waveforms are shown in the below figure. The proposed 32-Bit multiplier design is explained in the previous section is having lower delay profile as well as the area occupied. The details of the delay and area is given in this section. The device utilization summary is given in Table 1.

In Fig. 3.1 the test bench of the proposed multiplier architecture is shown where three different calculations are done.

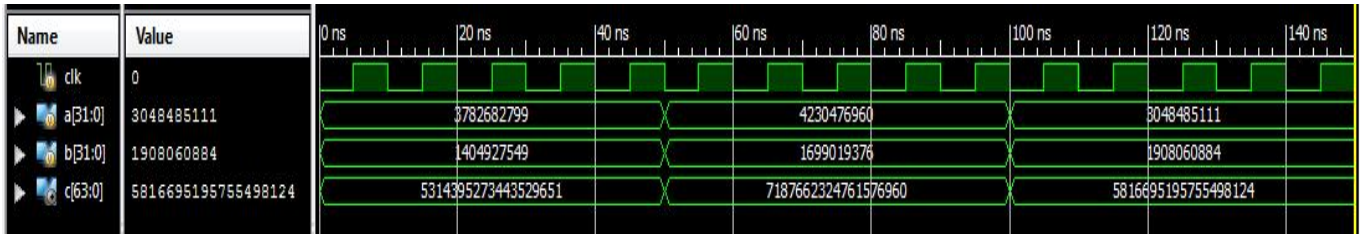

Fig. 3.1Test Bench Waveforms of the Proposed 32-Bit Multiplier

Table 1: Comparison of Delay and Area Utilization

Property / Work	Delay	Area	Delay Area Product
Previous Work	99.50 ns	2039	202880.5
Proposed Work	38.74 ns	2769	107271.06

IV. CONCLUSION AND FUTURE SCOPES

The proposed design is implemented using Verilog for 32-bit unsigned multiplier with recursive adder. Verilog was used to model and synthesis our multiplier. Using recursive logic improves the overall performance of the multiplier. Thus a 61% less delay and 47.5% area delay product reduction is possible with the use of the recursive adder based 32-bit unsigned multiplier than existing CSLA based 32 bit unsigned multiplier. The future extension could the use

of same adder architecture to implement higher bit sized architectures for example64-bit or 128-Bit which will significantly improved in terms of area as well as delay.

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