Design of CMOS Based Integer-N PLL Synthesizer with Current Starved Voltage Control Oscillator

Rachit Kourav, Braj Bihari Soni

M. Tech. Scholar, Department of Electronics and Communication, NIIST, Bhopal

Assistant Professor, Department of Electronics and Communication, NIIST, Bhopal

Abstract – In this paper, integer -N PLL synthesizer is premeditated by means of CMOS technology for providing efficient communication over high frequency ranges. There are many ways to realize synthesizers, but possibly the most common is based on a phase-locked loop (PLL). PLL-based synthesizers be capable of be further subdivided by which type of a dissection is used in the feedback path. The division ratio N be able to be moreover an integer called integer- N PLL synthesizers. The PLL based synthesizer is a feedback system that compares the phase of a reference fr to the phase of a alienated down output, fo, of a controllable signal source (also known as a voltage-controlled oscillator or a VCO). PLL can be designed by employing current starved voltage controlled oscillator (CSVCO) for improving the power dissipation and phase noise of the PLL system. The integer-N PLL synthesizer is operated from 32 MHz to 1GHz. Current consumption has been minimize by bring into play of a combine of analog and digital blocks. The simulated phase noise is -43.9 dbc/Hz at 300MHz and overall power dissipation is 50 µW

Keywords: Frequency synthesizer, phase locked loop (PLL), CSVCO, Charge Pump (CP).

I. INTRODUCTION

Latest advances in integrated circuit (IC) technology, make production process very appropriate for digital designs. Undersized-area and low-voltage designs are mandated by market necessities. One more improvement of a digital design is its scalability and trouble-free redesign with progression changes or shrinks. In view of the fact those analog blocks are nearby in a number of digital and mixed-signal ICs, their redesign is an vital factor in the liberate of a new product [11]. However, the recital provisions of analog blocks necessitate a complete redesign in a original process, thereby growing the design cycle time. Reducing the quantity of analog circuitry can get better the redesign of these mixed-signal ICs [9]. Phase locked loops (PLLs) are widely used in microprocessors and digital signal processors for clock creation and as a frequency synthesizers, in RF communication systems for clock extraction and generation of a low phase noise local oscillators [8].

Phase locked loops have been described in literature ever since 1923 [1]. But it was only in late 1970s that PLLs were used in modern communication systems due to the rapid development of integrated circuits. Since then the use of PLLs has been shifted from high precision instruments to more reliable consumer electronic products. A PLL is a circuit synchronize an output signal (generate by means of an oscillator) with a reference or input signal in frequency as well as in phase. In the synchronized (locked) state, the phase error between the oscillator's output signal and the reference signal is zero, or it remains constant [1].

This paper presents the design of an integrated low power phase locked loop system in CMOS technology to be used as a clock generator for ultra-low power applications. The phase of reference signal is compared with output signal coming from the frequency divider in the phase frequency detector. Depending on the phase error, the charge pump in next stage pumps current into or out of the loop filter. In the next stage is a voltage controlled oscillator whose frequency keeps changing until lock is obtained, that is, until there is no phase error between reference and output signal. Once in locked state, VCO frequency becomes N times the reference frequency, where N is the division value of the divider.

II. CIRCUIT IMPLEMENTATION

The PLL is a feedback system that forces the divided-down VCO output phase to follow the reference signal phase. That is, it is a negative feedback loop with phases as the input and output signals. The loop is composed of a phase detector, a low pass filter, a VCO, and a divider [3]. The phase detector, which is the summing block of the feedback system, is used to compare output phase θ_o to reference phase θ_r. The low pass filter is usually a linear transfer function that is placed in the system to control the loop's dynamic behavior including the settling time and transient response [2]. The VCO generates the output signal and the divider divides the VCO output signal back down to the same frequency as the input. A feedback system based on phase rather than frequency because in any feedback loop without infinite dc gain there is

always an error (finite error signal) between the input (reference) and the output [3].

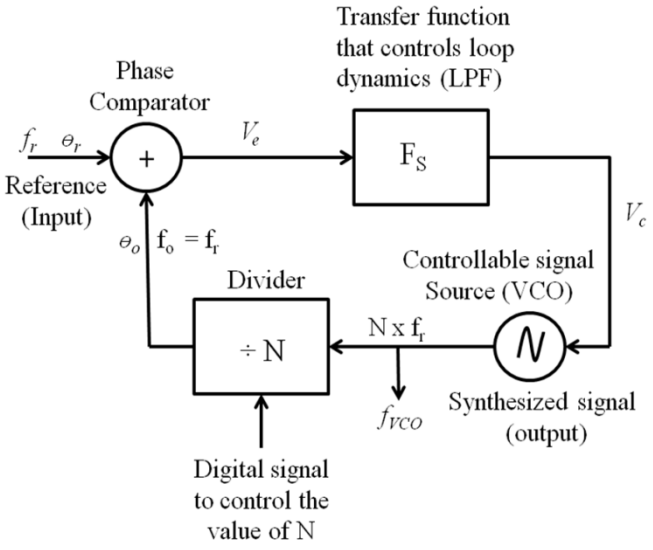


Fig.1 Simple Integer-N frequency synthesizer

Thus, if we used a frequency-locked loop, then in most cases, there would be an error in the output frequency and it would not track the input as precisely as does a loop based on phase. The input reference in wireless communications is a quartz crystal. These crystals are low cost and can be made to resonate with extreme accuracy at a particular frequency determined by the physical properties of the crystal. Unfortunately, they can only resonate at frequencies as high as about 100 MHz and therefore cannot be used directly as an LO in RF applications [4]. The other disadvantage to using a crystal directly is that there is no convenient way to tune their frequency. This is one of the main reasons that frequency synthesizers have become so popular. If the divider block is implemented using circuitry such that the divide ratio is programmable, then a range of frequencies can be obtained without the need to change the reference frequency [3].

III. PLL COMPONENTS

III.1 Phase Detector

A phase detector produces an output signal relative to the phase difference of the signals applied to its inputs. The inputs and outputs can be sine waves, square waves, or other periodic signals, not necessarily having a 50% duty cycle. The output signal could be a current or voltage and it could have multiple frequency components [3]. Since the dc value is the component of interest, the phase detector is typically followed by some sort of filter. Thus, the equation that describes a phase detector is:

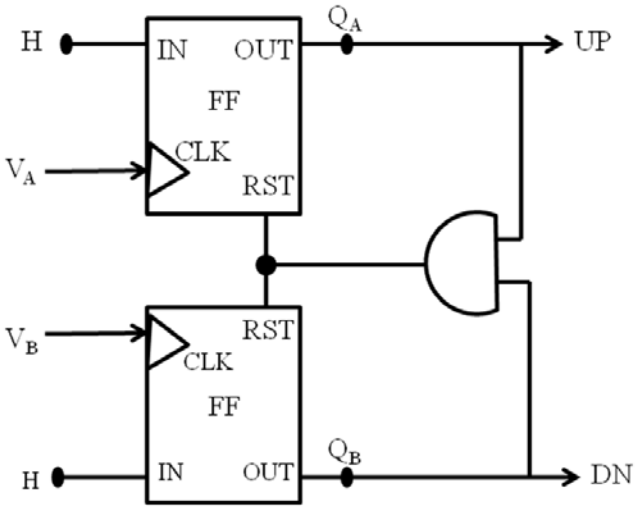


Fig. 2. Phase Frequency Detector

$$V_e(S) = K_{phase}\left(\theta_R(S) - \theta_o(S)\right) \quad (1)$$

The output of the phase detector, $V_e(S)$, is often also called the error voltage and is seen to be proportional to the difference of the input phases with proportionality constant K_{phase}. Let us assume start in the middle state, the tri-state where both outputs are zero. Then, depending on which edge arrives first, the PFD moves either to the up state or to the down state [5].

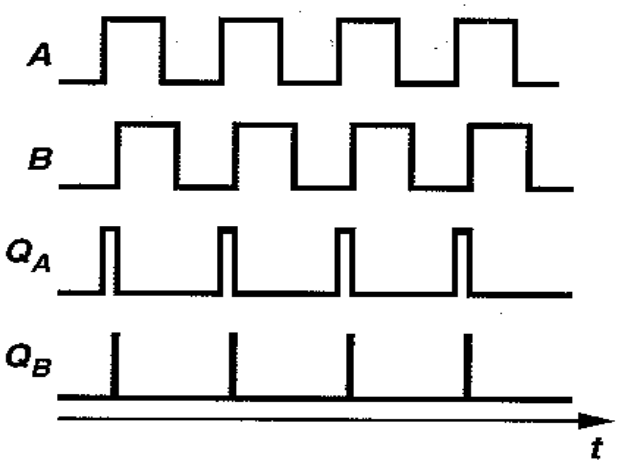


Fig. 2.1 Output waveforms of PFD

III.2 Charge Pump

The charge pumps current drive the PFD output. It converts the amount produced by digital PFD signal addicted to analog signal. Essentially, the charge pump consists of a current source, a current sink and two switches [7]. On the other hand, the charge pump is typically followed by a

passive loop filter that integrates, the charge pump output current to a VCO control voltage.

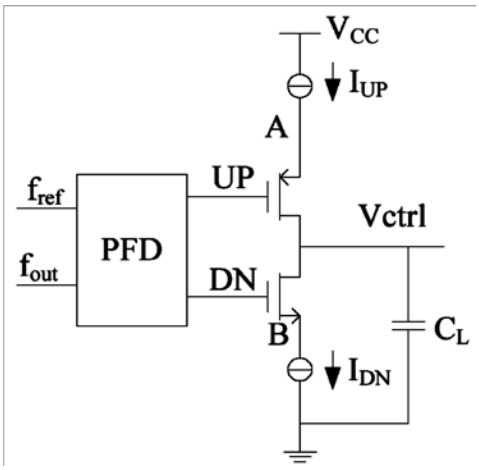
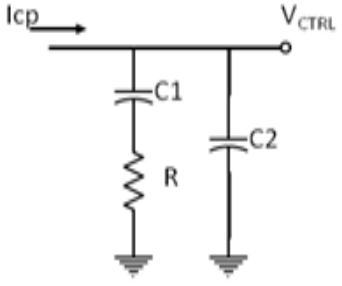


Fig. 3. Phase Frequency Detector with Charge Pump

Thus, the charge pump output voltage for eternity corresponding to the VCO control voltage. The charge pump moreover sources or sinks current in line with UP and DOWN signal. This quantity of current is transformed into controlled voltage by the loop filter for tuning the VCO [3]. To let alone current mismatching, the source and sink current values must be same. The control voltage increases while the reference signal leads the feedback signal and decreases when reference signal lags the feedback signal. If, the source and sink current of the charge pump are in cooperation I_{CP} the phase detector gain is given by

$$K_{phase} = \frac{I_{CP}}{2\pi} \qquad (2)$$

III.3 Loop Filter



Normally, VCOs are controlled by voltage and not current. Thus, generally we need a method to turn the current produced by the charge pump back into a voltage. In addition, low pass filtering is needed since it is not desirable to feed pulses into the VCO [6]. This is usually done by dumping the charge produced by the charge pump onto the terminals of a capacitor. In addition to turning the current back into the voltage, loop filters are also the components most commonly used to control system-level loop dynamics[3].

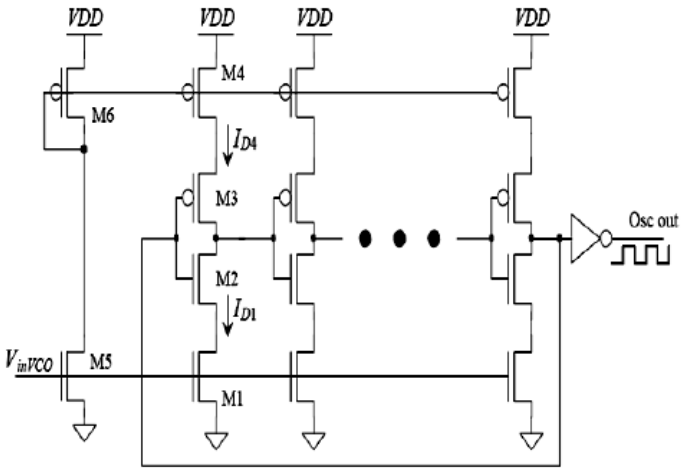


Fig. 4. Loop Filter

$$F(S) = \frac{V_{CTRL}(S)}{I_{CP}(S)} = R + \frac{1}{C_1 S} \| \frac{1}{C_2 S} \qquad (3)$$

where V_{CTRL} is the voltage across the loop filter and I_{CP} is the current coming from the charge pump circuit.

$$\frac{R\,C_1\,S + 1}{RC_1C_2\,S^2 + S(C_1 + C_2)} = K_F . \frac{S + \omega_z}{S.\left(\frac{S}{\omega_p} + 1\right)} \qquad (4)$$

Thus, we have obviously acquire a zero ω_z and a pole ω_p which are given by

$$\omega_z = \frac{1}{R\,C_1} \qquad (5)$$

$$\omega_p = \frac{C_1 + C_2}{C_1\,C_2\,R} \qquad (6)$$

III.4 Current Starved Voltage Controlled Oscillator (CSVCO)

Within the VLSI environment the design of a linear and broad range voltage controlled oscillator designed for RF purpose is a challenging work for electronics engineers. VCO is the most important component in the numerous RF circuits [10]. VCO is the heart of Phase Lock Loop system. An oscillator is a self-governing system which generates a sporadic output without any input.

A ring oscillator is comprised of an amount of delay stages, with the output of the last stage fed back to put in the first.

The current starved VCO is planned using ring oscillator and its function is also similar to that.

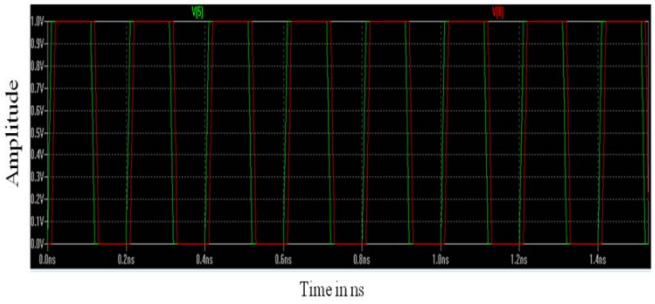


Fig. 5. Current Starved Voltage Controlled Oscillator

From the schematic circuit shown in the Figure 5, pragmatic that MOSFETs M2 and M3 work as an inverter, while MOSFETs M1 and M4 control as current sources. The current sources, M1 and M4, bound the current accessible to the inverter, M2 and M3; in other words, the inverter is famished for the current. The MOSFETs M5 and M6 drain currents are the indistinguishable and are situate by input control voltage. The currents in M5 and M6 are mirrored in each one inverter/current source stage. The upper PMOS transistors are linked to the gate of M6 and source voltage is functional to the gates of all lower NMOS transistors [10].

The total capacitance on the drains of M2 and M3 is given by

$$C_{total} = C_{out} + C_{in} \quad (7)$$

$$C_{total} = C_{ox}' \left(W_p L_p + W_n L_n\right) + \frac{3}{2} C_{ox}' \left(W_p L_p + W_n L_n\right) \quad (8)$$

This is merely the output and input capacitances of the inverter. This equation can be written in a more useful form as

$$C_{total} = \frac{5}{2} C_{ox}' \left(W_p L_p + W_n L_n\right) \quad (9)$$

The time taken to charge C_{total} from zero to V_{SP} with the constant current I_{D4} is given by

$$t_1 = C_{total} \frac{V_{SP}}{I_{D4}} \quad (10)$$

where V_{SP} is switching point of the inverter.

The oscillation frequency of the current-starved VCO for N (an odd number > 3) stages is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N C_{total} V_{DD}} \quad (11)$$

IV. SIMULATION OF PROPOSED INTER-N PLL FREQUENCY SYNTHESIZER

V.

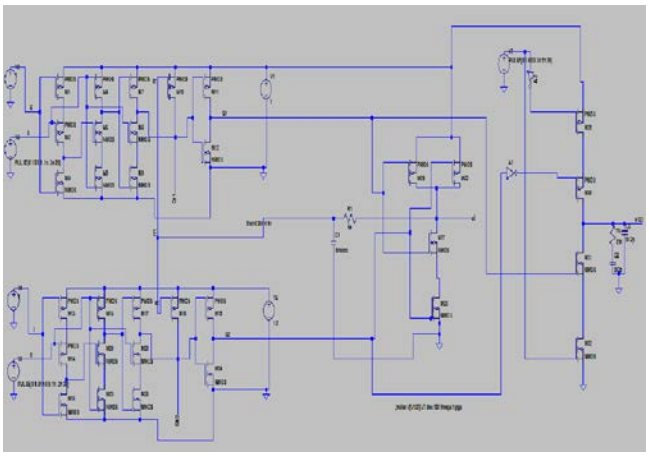


Fig. 6. Schematic of proposed PFD with CP and loop Filter

The circuit is shown in Fig. 6. Two static D flip-flops are used to detect rising edges of reference clock and feedback signal. The Q outputs are combined by an AND gate to reset the flip-flop states. Whenever there is a phase difference between the reference and feedback signals, a short pulse is generated at either UP or DOWN pins to charge or discharge the loop filter to minimize the phase error. The pulse duration is lengthened by a 50 ns RC delay block to eliminate the dead zone problem, which can put a lower limit on the PFD phase error in locked condition [5].

A charge pump circuit is used to convert the logical state of phase frequency detector to voltage related information. This is done by generating charging or discharging current depending on the output coming from phase frequency detector. The output from the charge pump enters the loop filter which controls the VCO.

A second order passive loop filter was realized. The loop bandwidth and phase margin were selected to be 1 GHz .The component values are calculated from linear model [11] with VCO gain obtained from schematic simulations. Values of 21 kΩ + 207 pF)//31.7 pF were selected.

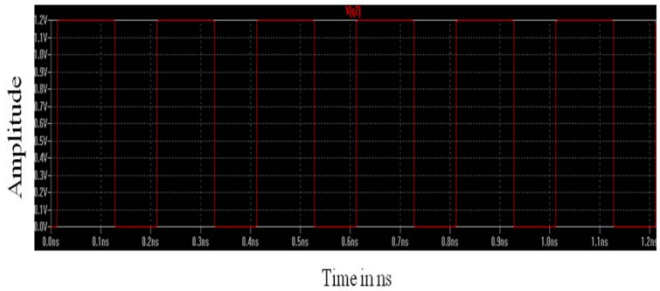


Fig. 7. Showing refrence signal and output signal with delay

In the fig.7 shows the waveform of input signal that is refrence signal and output signal with some delay which is employing to the phase frequency detector to produce two signals i.e. UP and DN output signals.

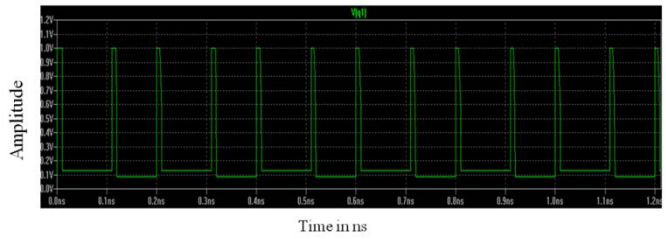


Fig. 8. Waveform of output signal from DN

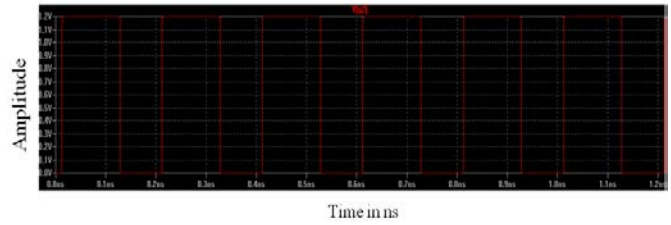


Fig. 9. Waveform of output signal from UP

In the fig.8 and fig.9 shows the waveform of output signals from DN and UP respectively corresponding to input signlas given to the phase frequency detector.

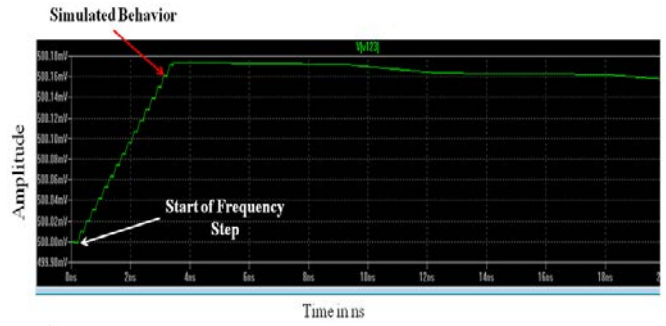


Fig. 10. Response of PLL design's control voltage during a 305.8 MHz frequency step.

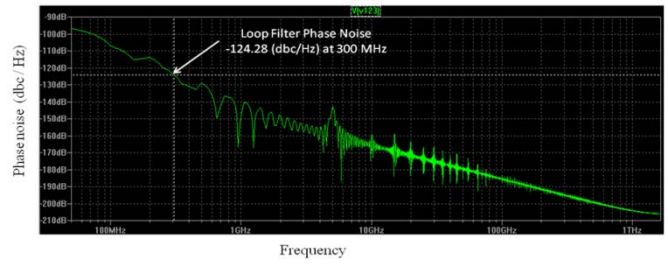


Fig. 11. Simulated Phase noise of loop filter stage

The tail of this graph is cut off, but the loop settled in about 3.47 ns, which is very close to the 4.1 ns predicted. The main difference between the simple estimate and reality is the fact that phase acquisition begins before the PLL actually reaches its final frequency value.

In fig. 11 shows the total phase noise including PFD with charge pump stage and loop filter stage which comes about -124.28 dbc /Hz at 300MHz which is less as compaired to some analog PLL.

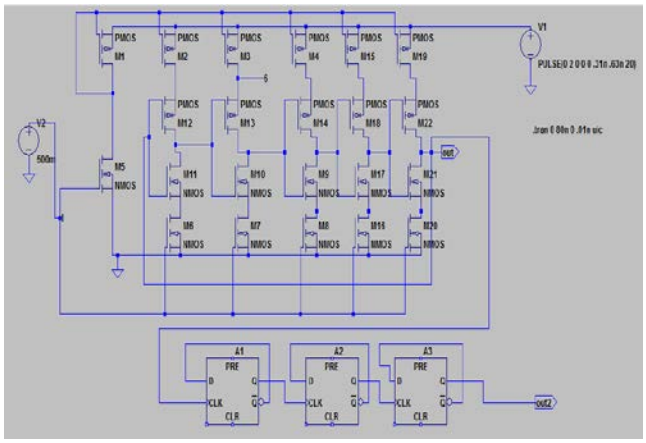


Fig. 12. Schematic of CSVCO and frequency Divider

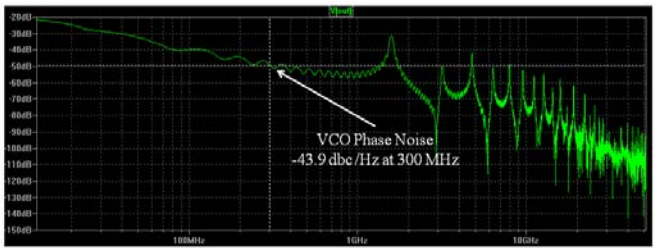


Fig 13. Simulated phase noise of CSVCO

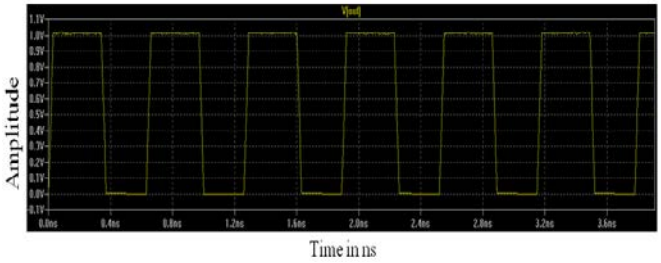


Fig .14. Simulated Output Voltage from CSVCO

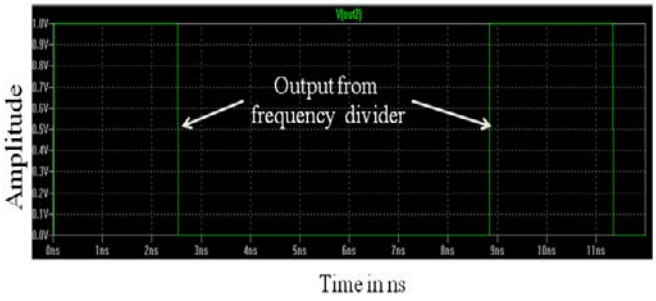


Fig. 15. Simulated output voltage from frequency divider circuit

The circuit includes 3 divide-by-two blocks in cascade to obtain a division of 8. The divide-by-two block consists of 3 cascaded static complementary D latches [1] connected within a negative feedback loop.

TABLE 1. PERFORMANCE SUMMARY OF DESIGNED PLL

	Power Supply (V)	Output Current(μA)	Output Power (μW)	Phase Noise dbc/Hz
Ref no 1	1.2	77	92.4	-89.6 at 500 KHz
Proposed Work	1.2	70	50	-43.9 at 300 MHz

VI. CONCLUSION

A low frequency inters- N PLL synthesizer is designed and simulated for low power applications. The PLL uses current starved VCO for achieving better performance over high frequencies and reduces power dissipation and current consumption by using CMOS technology. The VCO frequency range is 300 MHz to 1 GHz. A low power of 50 μW from 1 V supply and simulated phase noise is -43.9 dbc/Hz at 300 MHz.

VII. FUTURE SCOPE

In future the same PLL circuit is designed for all- digital PLL by replacing the VCO to DCO and makes them a fractional – N PLL frequency synthesizer by which the whole PLL system is converted into all digital PLL system. The power and current consumption is improved and further the system will ready for high frequency operations.

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