Implementation of SRAM Layout in 28nm Technology

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Abstract - This study presents an area efficient layout design of 1KB SRAM using 28nm as fabrication technology in CADENCE Virtuoso platform. The layouts were finally verified using the design verification checks such as DRC and LVS. Also, a comparison of the SRAM layout was done against the layouts designed using existing technologies. Technology nodes used are 28nm and 65nm.

Keywords: Bitcell , Core Array, DRC, LVS , Post-Decoder, SRAM.

I. INTRODUCTION

Semiconductor industry is exploiting every opportunity to reduce the size of expensive memories. Nowadays, with the rapid growth in communication and signal processing, the electronics industry has become aware of the needs of the consumer like substantial reduction in size and cost. As a result, Application Specific Integrated Circuits (ASIC) Designers are particularly interested in utilizing the SOC (System on Chip) designing systems, where close to 70 percent of the area of SOC is covered by Static Random Access Memory (SRAM) cells. Thus, SRAM scaling has become one of the greatest research areas to decrease the size and cost per function in microprocessors.

In this paper, we intend to discuss the design of a memory layout using 28nm technology and verify the results. The area of the layouts are then compared with the area of designs based on already existing technologies to further validate and appreciate the advantages of using 28nm technology.

II. ARCHITECTURE OF MEMORY

A typical block diagram of SRAM has been shown in Fig 2.1

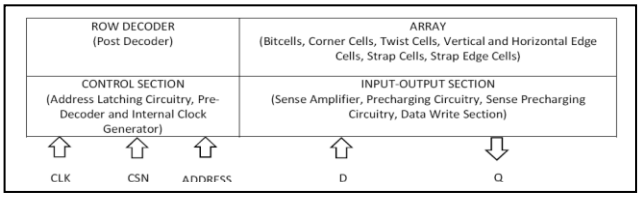


Fig. 2.1 SRAM Architecture with external pins

The layouts of blocks of SRAM implemented using 28nm technology are as below.

A. Control Section

It is the heart of the entire memory. This block generates all the controlling signals for the proper operation of the memory. Among the different generated signal, internal clock is the most important one. The present control block contains internal clock generator, address latching circuitry and pre-decoder part. This has been indicated in Fig. 2.2

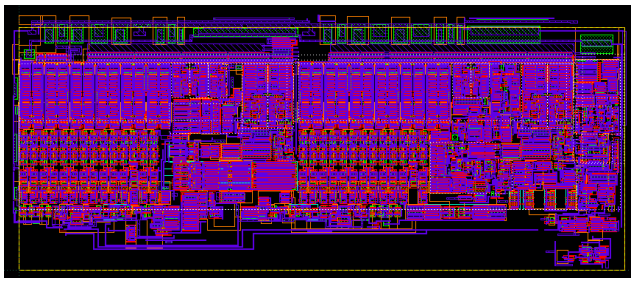


Fig. 2.2 Layout of Control Block in 28nm

B. Post-Decoder

Post-Decoder, also called Row-Decoder, consists of repeated instances of a combination of logic devices. It is used to select a particular row of Core Array. Refer Fig. 2.3.

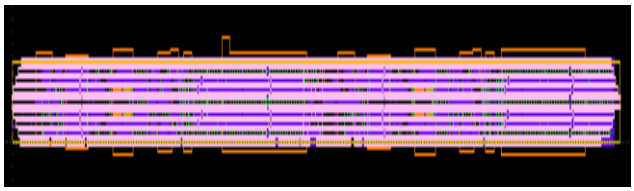


Fig. 2.3 Layout of Row-Decoder in 28nm

C. Input-Output Section (IO)

IO also called Data-Path, consists of sense amplifier to aid data reading from a particular bitcell. For large memory instances, sense amplifier helps in achieving speed. IO also consists of mux circuitry, pre-charge circuitry for pre-charging, write assist circuitry to aid in writing and write driver circuitry to take input from user to write data. The IO layout designed in 28nm has been given in Fig. 2.4.

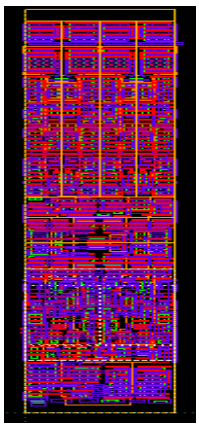


Fig. 2.4 Layout of IO in 28nm

Few sections of IO are as described below.

1) Sense amplifier

This is the most critical block in IO layout as the sense amplifier senses the differential voltage which is of very small magnitude and hence, even a minute mismatch in the layout designs of component transistors used in this particular block can lead to very inconsistent results.

Some ground rules while laying out a sense amplifier are:

- The critical device sets of M2 and that of M3 should be matched, refer Fig. 2.5. Hence they should be laid out using either common centroid or Interdigitized layout patterns.
- Guard rings shall be put around the critical PMOS and NMOS device sets.
- The coupling on the ST and SC nodes shall be identical. Refer Fig. 2.5.

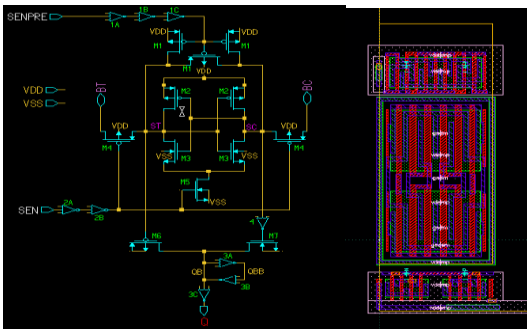


Fig. 2.5 Schematic and Layout of IO Sense Amplifier in 28nm

2) Pre-charge circuitry

Pre-charging is done for bit-line conditioning. The pre-charge circuit is used to charge the bit-lines to high voltage before the read/write operation. The pre-charge circuit consists of a pair of PMOS transistors along with an equalizer/balanced transistor connected between the two bit-lines to equalize their voltage levels. Fig. 2.6 shows the layout of Pre-charge circuit.

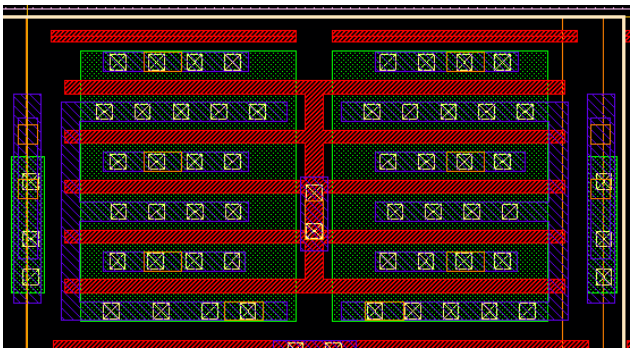


Fig. 2.6 Layout of Pre-charge circuitry in 28nm

D. Core Array

Bitcells are arranged in form of rows and columns referred to as the Core Array. Other than normal bitcells, Core Array also contains various other types of bitcells such as twist bitcells, horizontal edge bitcells (bit-line end cells) and vertical edge bitcells (wordline end cells) which are used to remove the design constraints of the memory and introduce equal environment for every bitcell. That is why they are called environment cells. Environment cells are not used to store data. Core Array consists of dummy column which consists of load cell and discharging cells. Refer Fig. 2.7 for layout of Core Array.

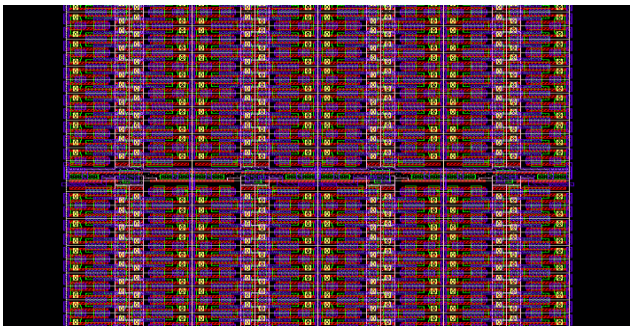


Fig. 2.7 Layout of Core Array in 28nm

Typical Bitcell and Strapcell layouts are described below.

1) Bitcell

A bitcell is the basic unit of memory architecture. It is used to store a single bit of data i.e. either '0' or '1'. 6T (six transistor) bitcell consists of two cross coupled inverters or simply a latch at its core and two pass transistors. These two pass transistors are used to access the data in the core of the bitcell. Fig. 2.8 illustrates the layout of 6T bitcell.

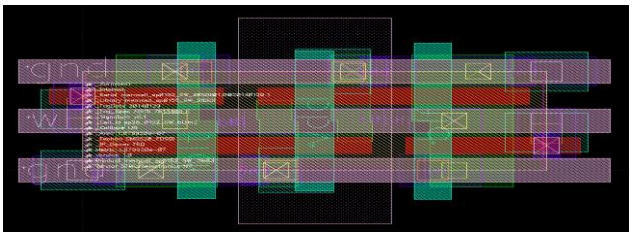


Fig. 2.8 Layout of 6T Bitcell in 28nm

2) Strapcell

Strapcells, consist of the corner and edge cells which can be horizontal or vertical straps based on the memory in use. The strap cells are used to provide substrate connections at the beginning and end of the array before the edge cells. Also, in cases, where the memory array is large, such that the substrate connections at the ends is not sufficient enough to avoid latch up, the strap cells are introduced in between the array at requisite distances. Fig. 2.9 shows the layout of Strapcell.

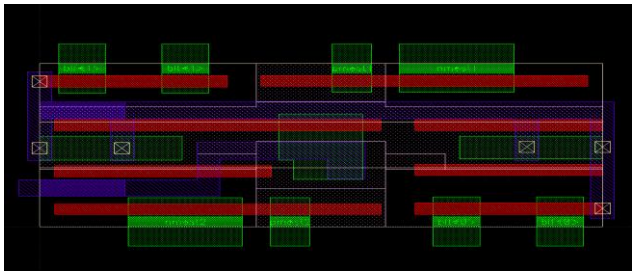


Fig.2.9 Layout of Strapcell in 28nm

III. LAYOUT DESIGN VERIFICATION

After the layouts were generated, the Design Rule Check (DRC) was run to ensure that there were no design rule violations. Fig. 3.1 shows the screenshot of a DRC window using Mentor Calibre. After ensuring that the design is free of DRC errors, schematics are generated based on import from leaf cell libraries and compiler generated verilog and netlist.

Fig. 3.1 Design Rule Check using Calibre

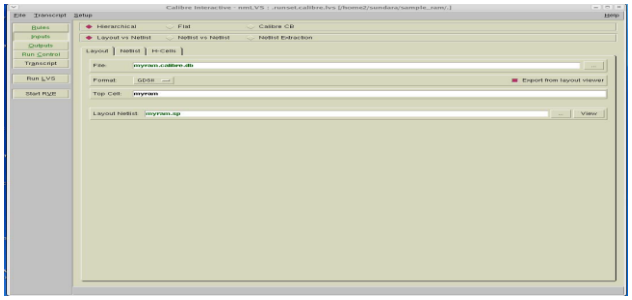
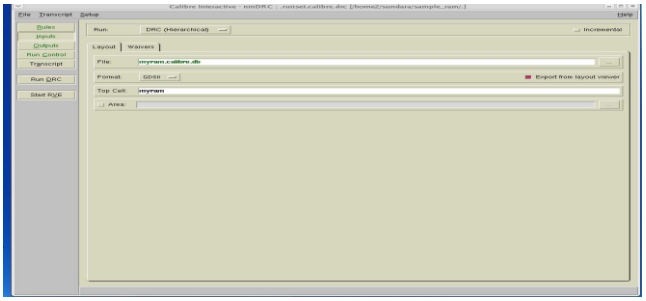


Fig. 3.2 Layout versus Schematic using Calibre

Layout Versus Schematic (LVS) check was run to ensure that there was consistency between layout and schematic. Fig. 3.2 shows the screenshot of LVS window using Mentor Calibre. After LVS check, parasitics are extracted resulting in generations of the netlist files that are needed for further design simulations.



IV. COMPARISON OF RESULTS

The area of each blocks of SRAM designed using 28nm technology has been compared with the corresponding blocks in 65 nm technology. The actual values of area of each blocks are listed below:

1) Control

Fig. 4.1 shows layout of control in 65nm.

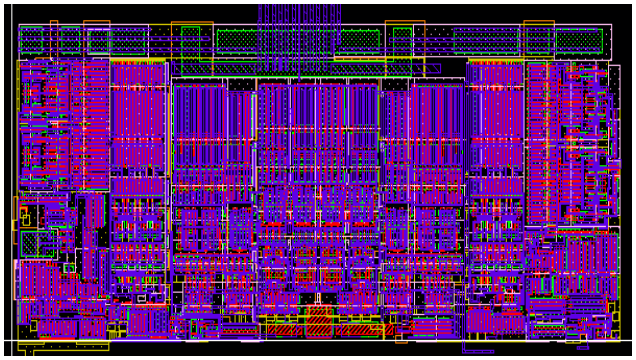


Fig. 4.1 Layout of Control in 65nm

The area of the control block in 65nm (refer Fig. 4.1) were found to be 1136.25µm^2 (50.59µm x 22.56µm), whereas that in 28nm (refer Fig. 4.2) was only 658.48µm^2 (40.647µm x 16.2µm)

2) Post decoder

Refer Fig. 4.2 and Fig. 4.3 for layouts of Row Decoder in 28nm and 65nm respectively.

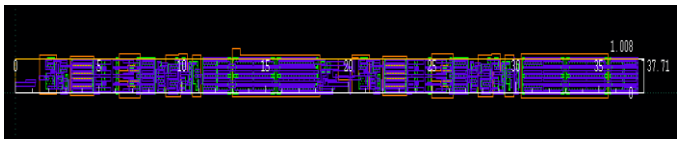


Fig. 4.2. Layout of row decoder in 28nm

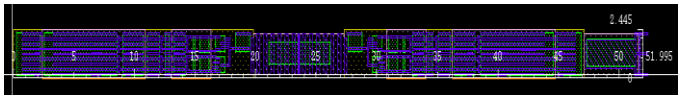


Fig. 4.3. Layout of row decoder in 65nm

The area of the post decoder in 65nm was found to be 127.13µm^2 (51.995µm x 2.445µm), whereas that in 28nm was only 38.011µm^2 (37.71µm x 1.008µm)

3) IO

On comparison of Input-Output Section of the SRAM blocks designed in 28nm and 65nm a reduction in area in 28nm was observed. Refer Fig. 4.4 and Fig. 4.5

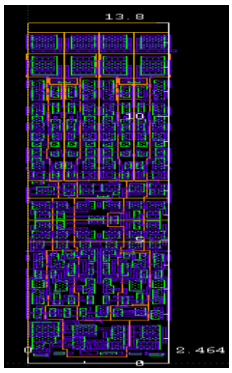


Fig. 4.4 Layout of IO in 28nm

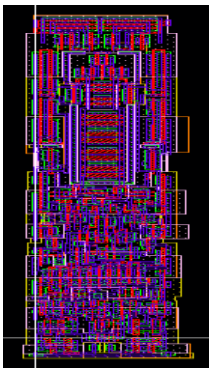


Fig. 4.5. Layout of IO in 65nm

The area of IO in 65nm was calculated as 104.75µm^2 (4.45µm x 23.54µm), whereas that in 28nm was only 34µm^2 (2.464µm x 13.8µm) which was very small compared to 65nm .

4) Core Array

The area of bitcell in 65nm was found to be 1.86µm^2 (2.02µm x 0.92µm) whereas that in 28nm is only 0.19µm^2 (0.746µm x 0.252µm). This value is very critical as the size of the SRAM depends on single bitcell area. The major portion of the SRAM is occupied by the Core Array. Therefore, reduction in the area of bitcell implies a huge reduction in area and thereby reduced size of the entire SRAM memory.

5) Top level layout of SRAM

The area of the layout design of 56x144 SRAM configuration in 65nm was calculated as 27612.48µm^2 (616.35µm x 44.8µm), whereas that in 28nm for the same configuration was only 12184.92µm^2 (398.2µm x 30.6µm).

V. CONCLUSION

1KB SRAM Memory Chip was designed using 28nm technology on CADENCE Virtuoso platform. Physical verifications were done using tools like Mentor Calibre. The size of the SRAM designed using 28nm was found to be considerably smaller than the one designed using 65nm. This substantiates the fact that as technology shrinks, more number of transistors can be accommodated in smaller area, thus giving way to a better SRAM Memory density and a huge reduction in size of the entire memory.

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