Modelling & Simulation of Multilevel Inverter with voltage Boosting Capacity

Suparna Buchke[1], Prof. Kaushal Pratap Sengar[2]

M. Tech Student (P.E.) TIT[1] , Professor EX Dept. TIT[2]

Abstract — Multilevel converters offer high power capability, resulting with lower output harmonics and lower commutation losses . Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry. This paper presents a new topology of the multilevel inverter with feature like output voltage boosting capability along with capacitor voltage balancing .The proposed multilevel inverter uses transistor clamped H-bridge (TCHB) with an bidirectional switch and four auxillary switches producing a boost output voltage . The single unit of new topology produces five-level output with output voltage double the input DC voltage where as a single unit of conventional H-bridge produces three-level ouput voltage similar to input DC voltage. The comparison has made between the proposed five-level inverter and conventional cascaded five-level inverter in terms of the output voltage , total harmonic distortion (THD) , No. of switching devices used etc. The analysis of the output voltage harmonics is carried out and compared with conventional cascaded H-bridge inverter topology. The proposed multilevel inverter topology is modelled using matlab/simulink. From the results the proposed inverter provides more output voltage.

Index Terms—Multilevel inverter, cascaded H-bridge, multicarrier phase width modulation, Transistor clamped inverter, cascaded neutral –point clamped inverter.

I. INTRODUCTION

There are various application varying from medium voltage to high voltage high power application which requires DC to AC conversion using multilevel inverters. The research on multilevel inverter is ongoing further to reduce the number of switching devices count to reduce the manufacturing cost, capacitor voltage balancing .The inverters with number of voltage levels equal to three or above than that are known as the multilevel inverters. Multilevel inverters are capable of producing high power high voltage as the unique structure of the multilevel voltage source inverter allows to reach high voltages with low harmonics without the use of transformers or series connected synchronized switching devices. As the number of voltage levels increases , the harmonic content of the output voltage waveform decreases. The synthesized multilevel outputs are superior in quality which results in reduced filter requirements[1]. There are three major multilevel voltage source inverter topologies neutral-point lamped inverter (i.e diode clamped) , flying capacitor (capacitor-clamped) and cascaded H-bridge multilevel inverter . There are also various other topologies which have been proposed and have successfully adopted in various industrial applications. The novel universal multi-carrier PWM control scheme is used .This paper mainly focuses mainly on the cascaded H-bridge inverter topology. The cascaded multilevel inverter has the potential to be the most reliable out of three topologies . It has the best fault tolerance owing to its modularity a feature that enables the inverter to continue operate at lower power levels after cells failure[2]-[3]. Due to the modularity of the cascaded multilevel inverter it can be stacked easily for high power and high voltage applications. The cascaded multilevel inverter mainly consists of several identical H-bridge cells which are cascaded in series from the output side. The cascaded H-bridge (CHB) may further be classified as symmetrical if the DC bus voltage is equal in all the series power cells and as asymmetrical if the DC bus voltage is not same for each power cell. The symmetrical CHB is more advantageous over the asymmetrical CHB in terms of modularity , maintenance and cost. In case of the asymmetrical CHB DC bus voltage is varied in each power as per the requirement to increase the voltage levels [2] ,[3]. In case of the symmetrical CHB the voltage level can be increased without varying the DC voltage with same number of power cells. The transistor clamped topology is popular now a days a provides provision to increase the output levels by taking different voltage levels from the series stacked capacitors [1],[3]. In this paper the new configuration of the (symmetrical H-bridge) single phase 5-level inverter is proposed which produces a five-level output voltage instead of three-level as in case of conventional H-bridge. Also this new proposed topology produces the boost output voltage in comparison to conventional H-bridge topology which requires two H-bridge cells producing the five-level output voltage but t equal to the input DC voltage .

II. PROPOSED INVERTER CONFIGURATION

The conventional H-bridge inverter consists of DC voltage for each H-bridge and only four switching devices. The value of the DC voltage in each bridge depends whether the configuration is symmetric or unsymmetric. Fig.1 shows the conventional H-bridge. The general block diagram for the proposed inverter is shown in fig.2 and the general configuration of the proposed inverter topology is shown in fig.4 which also represents a single cell which produces the five-level output with boost output voltage. It consist of total of four main controlled switches and five auxillary switches including an additional bidirectional

switch consisting of S11 and S11' in a single cell which is connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels (+2Vdc , +Vdc , 0 , -Vdc , -2Vdc) based on the switching combination . The switches S21,S31,S41,S51 forms the H-bridge and the remaining switches Sa1,Sa2,Sa3,Sa4 are auxillary switches connected in the same leg which plays a role in boosting the voltage and the input DC voltage is connected with positive terminal between the switches Sa1 and Sa2 and the negative terminal between the switches Sa3 and Sa4. The capacitor voltage divider is formed by C1 and C2.

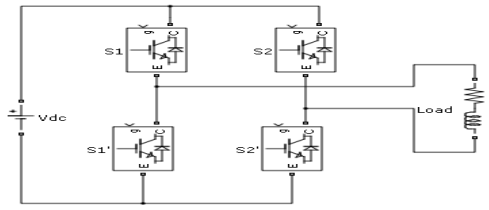

Fig.1 Conventional H-bridge

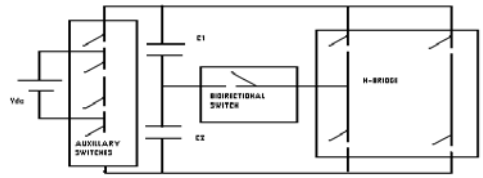

Fig.2 General block diagram of new topology

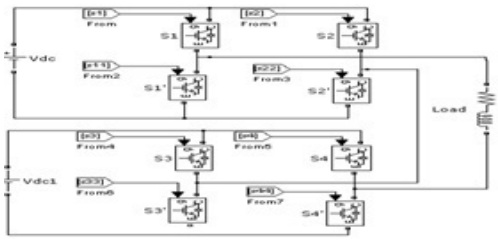

Fig.3 Single phase five-level cascaded H-bridge inverter

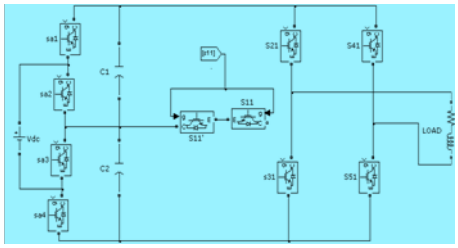

Fig.4 Proposed Single-phase 5-level multilevel inverter

Multilevel Inverter Type	Proposed Inverter	cascaded H-bridge	Diode clamped	Flying Capacitor Clamped
NO. of main switches	4	8	8	8
No. of auxillary controlled switches	5	0	0	0
No. of diodes	8	8	20	8
No. of capacitor	2	2	4	10

Table .1 Comparison between four different 5-level inverter topologies

The new topology achieves a 50 % reduction in the number of main power switches required, using only four controlled power switches instead of the eight required in any of the other three configurations. The auxiliary switch voltage and current ratings are lower than the ones required by the main controlled switches. Auxiliary devices (diodes and capacitors): the new configuration reduces the number of diodes by60% (eight instead of 20) and the number of capacitorsby 50% (two instead of four) when compared with thediode clamped configuration. The new configuration reduces the number of capacitors by 80% (two instead of 10) when compared with the capacitor clamped configuration.

III. OPERATION OF PROPOSED INVERTER TOPOLOGY

The working of the proposed five-level inverter topology is explained telling how the required five level output is produced

As:

1. Maximum positive output that can be produced is the double of the input DC voltage i.e 2Vdc which is produced when S21 is on connecting the load positive terminal to the load and S51 is on connecting the load negative terminal to the Vdc thus the total output voltage is 2Vdc. The output voltage level Vdc is obtained when Sa1 , S11 , S51 and Sa2 gets turned on other switches remaining off.
2. Maximum negative output is -2Vdc which is produced when switches S41 and S31 gets turned on connecting the negative and positive terminal of the load respectively to the input source. The negative level –Vdc is obtained when switches Sa1 , Sa3 , S11 , S41 are turned on other switches remaining off.

The detailed operation of the proposed topology can also be understand through the look up table . In the look up table 0 and 1 values are assigned to the switches for a particular voltage level. At any level of the output voltage the switches which are having value 1 means they are in

the ON state at that time and the remaining switches with the zero value are in the OFF state at the same instant of time. The look up table for the proposed inverter is given in the figure given below.

Voltage level	+2Vdc	+Vdc	0	-Vdc	-2Vdc
Sa1	0	0	0	1	0
Sa2	0	1	0	0	0
Sa3	0	0	0	1	0
Sa4	0	1	0	0	0
S11	0	1	0	1	0
S21	1	0	1	0	0
S31	0	0	0	0	1
S41	0	0	1	1	1
S51	1	1	0	0	0

Table.2 switching pattern for the proposed five-level inverter

IV. PWM CONTROL SCHEME

Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have the controlled output voltage []. There are variety of modulation techniques available. Basically the control technique can be classified as the pulse width modulation which is considered as the most efficient method. This PWM is further divided into various PWM techniques such as single pulse PWM, space vector PWM, multiple pulse PWM, phase displacement control []. For this proposed topology we are using the multicarrier based control technique which can be applied to all the topologies of the multilevel inverter. For any given number of levels in the output voltage the number of carrier to be used is given as N-1 Where N is the number of levels in the output voltage. Fig.5 represents the triangular shape carrier waveform and the sinusoidal reference signal showing the pulse width modulation technique used for the control. Simply a reference signal is taken which is a sinusoidal signal of 50Hz frequency and this reference is compared with the carrier signal which are the triangular wave .The modulation index we are using in this modulation technique is 0.95.The advantage of this scheme is that it offers the charge balance control in the input DC sources and voltage across the capacitor are also balanced []. Fig.8 shows the voltage across the two capacitors` which are equal in magnitude.

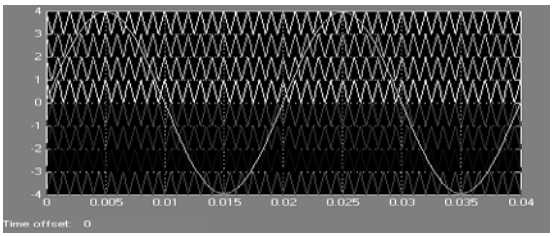

Fig.5 Multicarrier based PWM control scheme

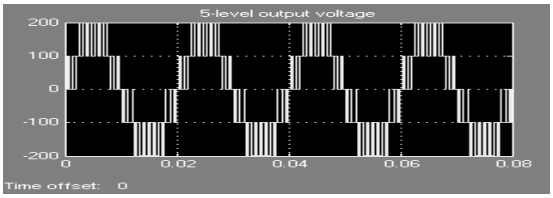

Fig.6 output voltage waveform of the single-phase 5-level cascaded H-bridge inverter using PWM

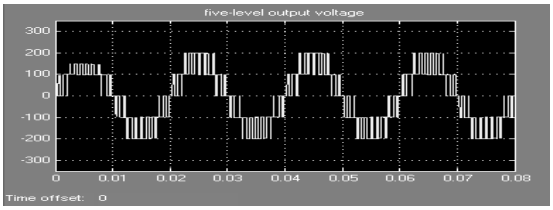

Fig.7 output voltage waveform of the proposed Single-phase 5-level inverter using PWM

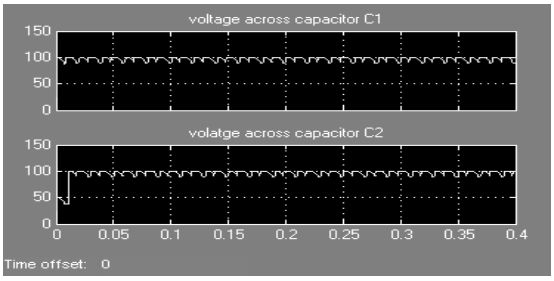

Fig.8 waveform of the voltage across the capacitors

V. COMPARISON OF PROPOSED MULTILEVEL INVERTER WITH CASCADED H-BRIDGE TOPOLOGY

The purpose of research for the multilevel inverter includes to get a quality power output with the reduced number of switching devices, balancing of the capacitors, reduced number of clamping diodes in order to reduce the overall cost of the multilevel inverter. In the proposed 5-level multilevel inverter topology the number of switches is only one more then the 5-level single phase cascaded H-bridge inverter. But the input DC voltage source required is half of the voltage source required in the conventional CHB. To produce the same output voltage the cascaded H-bridge has to use the two cells where as only one cell is required with the proposed topology. Fig.4 is showing the proposed single phase 5-level inverter which also represents a single power cell having input 100V DC voltage and the output ac voltage is 200V . The total harmonic distortion produced by the proposed inverter is 37.63% only , Fig.9 shows the

THD in % for single phase 5-level proposed multilevel inverter) which is very low as compared to the single unit of H-bridge inverter having THD of 70.99% , Fig.7 shows the THD in % for single H-bridge multilevel inverter which is 33.36% more than the proposed topology and if compared with conventional 5-level single phase cascaded H-bridge inverter which is having 37.51% THD which is 0.15% more , Fig.9 THD in % for single phase 5-level proposed multilevel inverter . In order to produce the nine levels in the output voltage the cascaded H-bridge requires three cells where as the proposed topology requires only two cells .

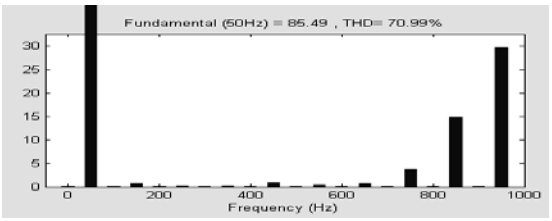

Fig.7 THD in % for single H-bridge multilevel inverter

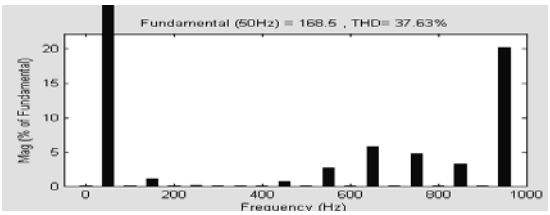

Fig.8 THD in % for single phase 5-level cascaded H-bridge multilevel inverter

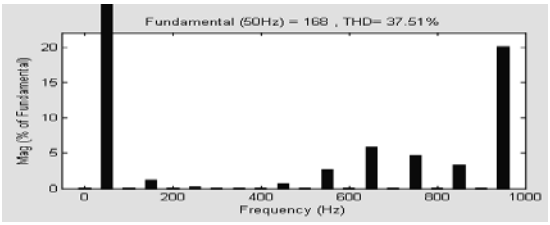

Fig.9 THD in % for single phase 5-level proposed multilevel inverter

VI. CONCLUSION

The proposed single phase 5-level multilevel inverter topology is much superior than the conventional 5-level single phase cascaded H-bridge topology in terms of the number of level in the output voltage, magnitude of the output voltage, total harmonic distortion (THD). Though the number of switching devices used is same but the input DC voltage magnitude required in the new multilevel topology is half of that required in conventional 5-level single phase cascaded H-bridge topology. The THD of the proposed topology is also less than the cascaded H-bridge inverter topology. In comparison with diode clamped and the flying capacitor type inverter of the same number of level there is a great reduction in the main power switching devices , diodes and the capacitors used .

References:

[1] Mahajan Sagar Bhaskar Ranjana,"MULTILEVEL INVERTER WITH LEVEL SHIFTING SPWM TECHNIQUE USING FEWER NUMBER OF SWITCHES FOR SOLAR APPLICATIONS",eISSN: 2319-1163,IJRET: International Journal of Research in Engineering and Technology,Volume: 04 Issue: 10,Oct-2015.

[2] Mr. D. Santhosh Kumar Yadav,"Analysis of Cascaded Multilevel Inverters with Series Connection of H-Bridge in PV Grid",International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463,Vol. 4 Issue 4, April-2015, pp: (101-106).

[3] Krishna Kumar Gupta,"Multilevel Inverter Topologies With Reduced Device Count: A Review",IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 31, NO. 1, JANUARY 2016.

[4] Ebrahim Babaei,"A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches",IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 62, NO. 2, FEBRUARY 2015.

[5] Vahid Dargahi, “A New Family of Modular Multilevel Converter Based on Modified Flying-Capacitor Multicell Converters",IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 30, NO. 1, JANUARY 2015.

[6] Sourabh Rathore, Mukesh Kumar Kirar and S. K Bhardwaj "SIMULATION OF CASCADED H- BRIDGE MULTILEVEL