Design of Various Analog Circuits using Differential Evolutionary Algorithm

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Abstract - Real world is analog in nature so design of optimized analog circuits is the need of the hour in order to make a pace development in the electronic era. Optimized analog circuit design is an important fraction of various analog and mixed signal circuits. Today the use of mixed mode integrated circuits is at its zenith. Analog circuits in CMOS technology have been borne to a great deal of complications due to various design challenges. This paper presents an efficient technique for adapting control parameter settings associated with differential evolution (DE) for various analog circuit . The DE algorithm has been used in many practical cases and has demonstrated good convergence properties. By adjusting the parameters of transistors through DE, the evolution can find the circuit which will satisfy our specifications. The outcome of the experiment for the so designed analog circuits shows that this is an accurate and promising way in determining the device sizes in an analog circuit. For circuit optimization C code of PSO algorithm has been integrated with Ngspice circuit simulator. The circuit is simulated using BSIM3v3 MOSFET models in TSMC 0.18 µm CMOS processes technology. The complete optimization system test setup is run on Ubuntu operating system.

Keywords: Optimization, DE Algorithm, Ngspice Simulator, 0.18 µm CMOS technology.

I. INTRODUCTION

Optimization of an electronic circuit is a technique used to select the circuit design factor values in such a way that the actual circuit performances meet the design requests. There are various optimization techniques have been reported in the past and the recent times for testing on benchmark functions and then used for various purposes. The gradient-based optimization methods [1] would generally deliver us with locally optimum solution. Convex optimization techniques [2] require excellent knowledge of circuit design to find globally optimum solution, which would be very challenging looking at the current state-of-the-art MOSFET models. The evolutionary algorithms [3] can be used to solve multimodal optimization problems to ascertain the solution space more strongly. These algorithms do not suffer from complications associated with the gradient-based and convex optimization methods. These algorithms do not involve awareness of circuit design and physical models. These algorithms also do not need to evaluate complex mathematical calculation even though they give global optimum solution. Holland has established genetic algorithm (GA) [4] with a motivation from biological evolution, has been reported several times for automatic analog circuit design. Few recent citations are also found in [3], [5]. Kennedy and Eberhart had projected particle swarm optimization (PSO) algorithm [6], [7]. They had been witnessed to give better accurateness compared to GA in most of the applications [8].Differential Evolution [8] [Storn and Price] is a design tool of optimization that is directly accessible for practical applications. In DE, each value of each variable is represented by a real number. The benefits of DE are its simple structure, ease of use, speed and robustness. DE uses mutation as a search mechanism and selection to direct the search toward the potential regions in the feasible region even if no information .is available. The basic theme behind DE is a new scheme for generating trial parameter vectors [9]. DE generates new parameter vectors by addition of the weighted difference vector between two population members to a third population. If the resultant vector yields a lower objective function value than a predetermined population member, the newly generated resultant vector replaces the vector with which it was compared. At last, the best parameter vector is evaluated for every generation to track the progress made during the optimization process. Thus DE algorithm has excellent convergence properties.

The rest of the paper is organized as follows: In section 2, working of DE algorithm has been described. Section 3 includes the implementation of various CMOS analog circuits.

II. WORKING OF DE ALGORITHM

DE is an algorithm uses NP variables as population of D dimensional parameter vectors for each generation. If no constraints are given about the problem, the initial population is chosen at random.DE generates new design variables by adding up the weighted difference vector between two population members to a third population member. If the resultant vector yields a lower objective function value than previous population member, the newly generated vector replaces the previous vector. In count, the best parameter vector is calculated for every generation in order to keep path of the progress made during the optimization process. DE proposes deviation in results with excellent convergence properties.

DE consists two arrays, each one holding population size NP and D dimensions, proposing real valued vectors. The first array holds the current vector population, while the second array holds vector population for the next generation. In each generation, NP competitions are carried to get the resultant composition of the consecutive generation. The vector differential $(X_{a,} - X_b)$ is defined by a pair of vectors $(X_{a,} X_b)$.When both the vectors $X_{a,}$ and X_b are chosen at random, their weighted difference is multiplied by some weighted factor and is used to obtain another random chosen vector $\acute{X_c}$. This process can be mathematically expressed as:

$$\acute{X_c} = X_c + F(X_{a,} - X_b) \quad (3.1)$$

The weighting factor F is a u constant supplied by the user in the optimal range of (0.5, 1), here 0.8 (DE, 2008) so as to increase the normalization of the values so generated in the composed vector. In consecutive generation, each first array vector X_i is aimed for crossover with a vector like $\acute{X_c}$ in order to produce a trial vector X_t.Uniform crossover is used with a crossover constant (CR), in the optimal range of (0.5, 1.0), here 0.5 (DE, 2008) which proposes the likelihood that the child vector gains the parameter values from the noisy random vector. Here the two conditions are followed – (i) When CR =1, each trial vector parameter is designed from $\acute{X_c}$. (ii)When CR = 0, at least one trial vector parameter should be from the target vector.

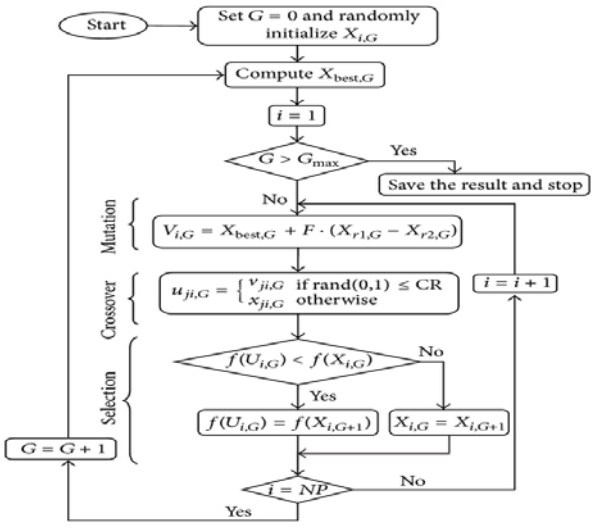

Figure 2.1 Flow chart of DE algorithm [12]

Now finally, the objective function relating the trial vector is compared with that of the target vector, and out of the two, whichever vector is having the lowest objective function value that vector would be selected for the next generation. This process is continued till the termination criterion of number of generations (MAXGEN) is met. It is also necessary that the difference in objective function values between two successive generations reaches a small value. Working of DE algorithm is being explained by flow chart as shown below.

III. ANALOG DESIGN CIRCUITS AND SIMULATIONS

A. CMOS VOLTAGE DIVIDER

Biasing necessities in analog CMOS design circuits liable to fall into two categories. Voltage references, for such things as cascade stages and comparators, and current references, for biasing amplifiers via multiple current mirror schemes, D/A convertors, etc. For some applications very simple arrangement are adequate.

Table 3.1 CMOS voltage divider desired specification achieved and result

Sr No	Desired Specifications(V)	Obtained Parameters (um)	Obtained Specifications (V)
1	V_{bias1} = 0.8	W1 = 0.165010	V_{bias1} = 0.7997221
2	V_{bias2} = 1.2	W2= 1000.000000	V_{bias2} = 1.201643
3	V_{bias3} = 1.7	W3 = 9.007360	V_{bias3} = 1.696074
-	-	W4 = 97.937816	-

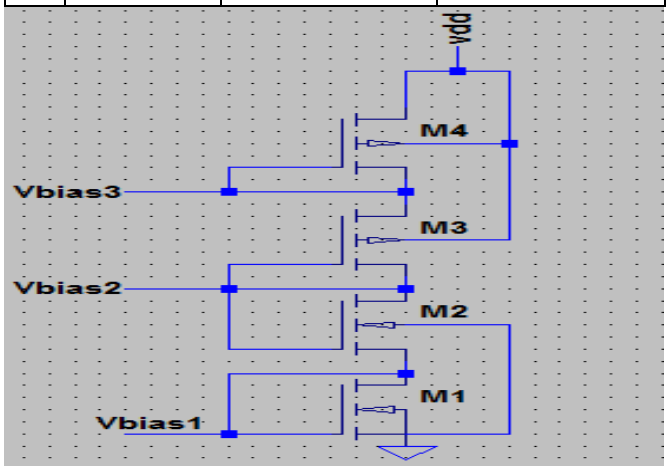

Figure 3.1 CMOS Voltage Divider

Figure 3.1 shows a simple voltage reference circuit based on an MOS transistor potential divider. Device dimensions are diversed to obtain the desired voltages and currents. This type of arrangement has the advantage that bias voltages obtained are directly related to the value of Vt on that particular die, and so there is a least danger of transistors of not being biased properly. A disadvantage is that there is a poor immunity to variations in power supply voltage.

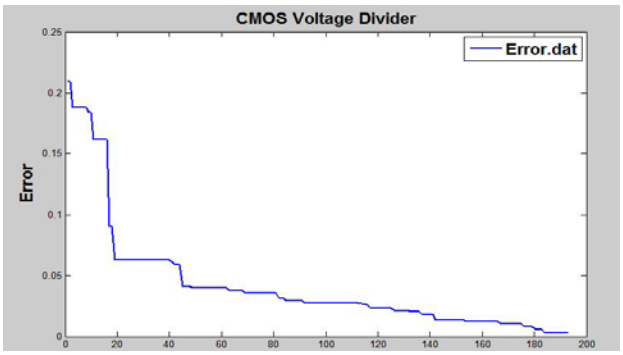

Figure 3.2 Plot of generations vs. error in CMOS voltage divider circuit

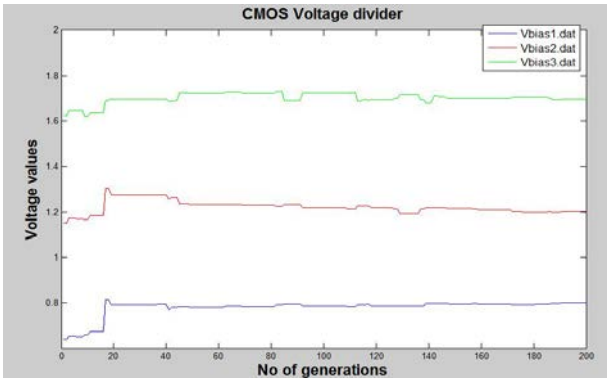

Figure 3.3 Plot of generations vs. $V_{bias1}, V_{bias2}, V_{bias3}$ in CMOS voltage divider circuit

Figures 3.2 and 3.3 shows the plot of specified error and obtained voltages respectively which are achieved when the circuit file is linked with the Ngspice simulator. The parameters range W1 to W4) is kept to be in the range of 0.1 to 1000 um. Also, these figures reveal that obtained parameters here (Voltages $V_{bias1}, V_{bias2}, V_{bias3}$) meet the desired specifications which can be matched with the values given in Table 3.1

B. Three stage Current Starved Voltage Controlled Oscillator

The three stage current – starved VCO is shown in Figure 3.4. Its working process is similar to ring oscillator. MOSFET's M2 and M3 operate as an inverter, while MOSFET's M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3, or alternatively, the inverter is starved for current. The MOSFET's M5 and M6 drain currents are the same and are set by the input control voltage. The currents ion M5 and M6 are mirrored in each inverter / current source stage. Attaining infinite input resistance is usually an easy part of the design. For the charge – pump configuration, the input capacitance of VCO can be added.

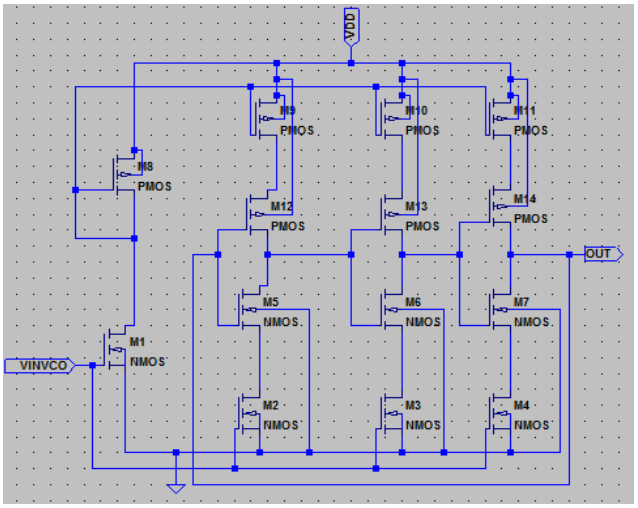

Figure 3.4 Three Stage Current – Starved VCO

Aim of this work is to design and optimize three stage current starved VCO circuit in order to achieve high linearity for specified frequency range. Here in this work VCO is designed and optimized with DE algorithm. The desired specifications along with the achieved results are given below. The range of the parameters (W1 to W7) is 1 to 1000 um.

Table 3.2 Three stage current starved VCO desired specification and achieved result

Sr. No.	Desired Specifications	Obtained Parameters (um)	Obtained Specifications
1	Oscillation Frequency = 400 Mhz	W1 = 869.564394	Oscillation Frequency = 400.0301Mhz
2	-	W2= 1000.000000	-
3	-	W3 = 1000.000000	-
4	-	W4 = 1000.000000	-
5	-	W5 = 1000.000000	-
6	-	W6 = 375.269488	-
7	-	W7 = 803.958389	-
8		K = 5.000000	-

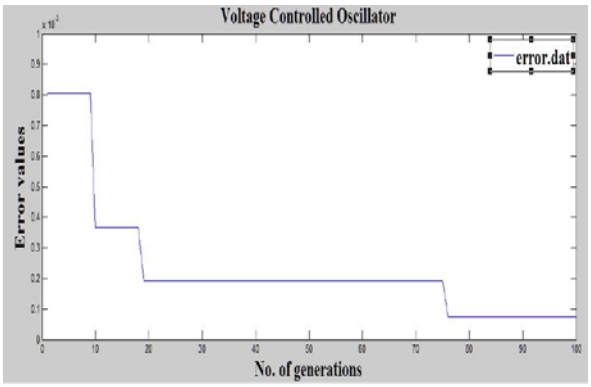

Figure 3.5 Plot of generations vs error in voltage controlled oscillator

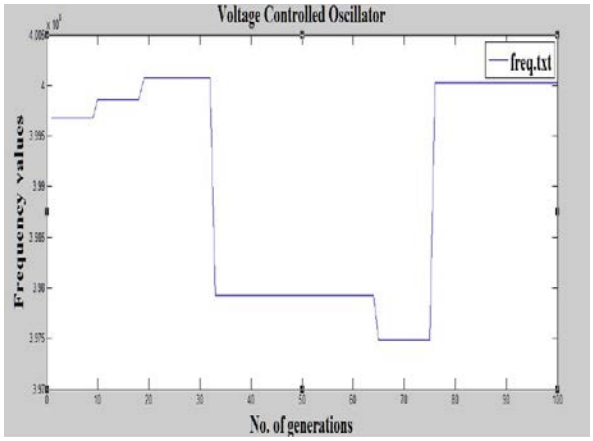

Figure 3.6 Plot of generations vs. frequency in voltage controlled oscillator

Figures 3.5 and 3.6 shows the plot of specified error and obtained frequencies respectively which are achieved when the circuit file is linked with the Ngspice simulator. Also, these figures reveal that obtained parameters here (frequency) meet the desired specifications which can be matched with the values given in Table 3.2.

C. COMMON SOURCE AMPLIFIER

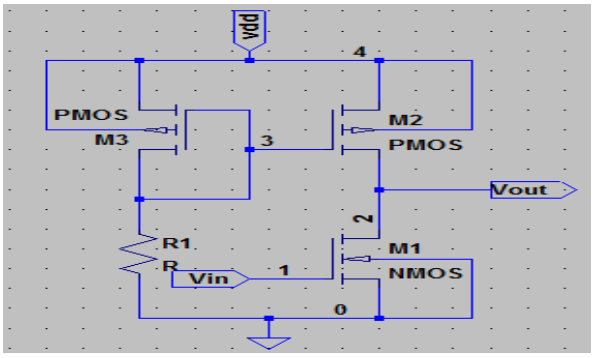

Figure 3.7 Common Source Amplifier

A common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, characteristically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common". In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit.

Since each of the input transistors carries a current of $I_{ss}/2$, the common mode level depends on how close $I_{ssD3,4}$ and $I_{ss}/2$. Suppose for example, that the drain currents of M2 and M3 in the saturation region are slightly greater than $I_{ss}/2$. As a result, in order to satisfy Kirchoff current law, both M2 and M3 must enter the triode regionso that their currents fall to $I_{ss}/2$.Table 3.3 Common Source Amplifier desired specification and achieved result.

Sr No	Desired Specifications	Obtained Parameters	Obtained Specifications
1	Gain = 10 dB	W1 =0.825986um	Gain =9.999957e+00dB
2	-	R1= 86.899451 kΩ	

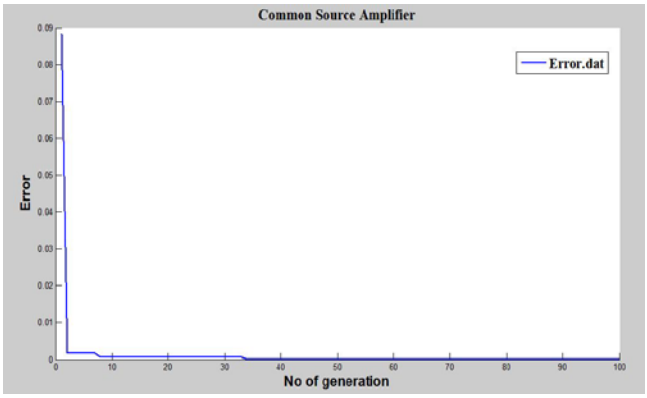

Figure 3.8 Plot of generations vs error in CS amplifier

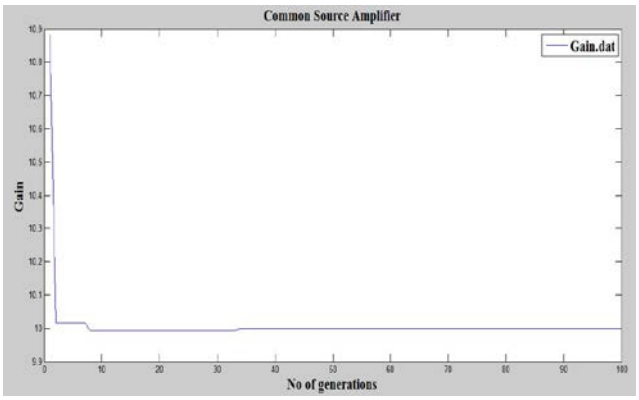

Figure 3.9 Plot of generations vs. gain in CS amplifier

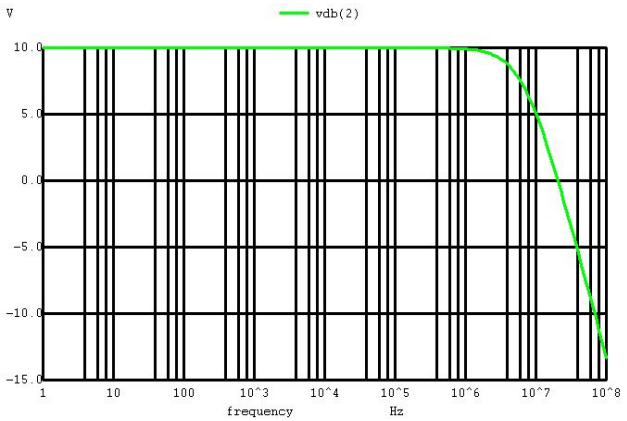

Figure 3.10 Ngspice simulation of frequency response of CS amplifier

Figures 3.8 and 3.9 shows the plot of specified error and obtained gain respectively which are achieved the circuit file is linked with the Ngspice simulator. Also, these figures reveal that obtained parameters here (gain) meet the desired specifications which can be matched with the values given in Table. Figure 3.3 shows the Ngspice simulation plot of gain in db versus frequency for CS amplifier.

D. CMOS Diffrential Amplifier With Current Mirror As Load

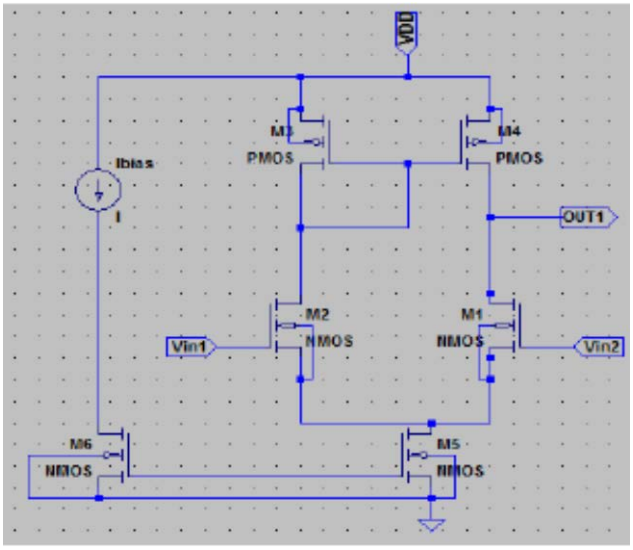

Figure 3.11 Schematic of CMOS Differential Amplifier

Differential amplifier is the most versatile circuit in analog circuit design which serves as an input stage to all op-amps showing great compatibility with all integrated circuits. Differentail amplifier can be characterized by its Common Mode Rejection Ratio (CMRR). CMRR is the ratio of differential gain to the common mode gain and it is ideally defined to be as infinity. Figure 3.11 shows the schematic diagram of Differential amplifier.

Above diagram shows that MOSFETs M1 and M2 are n-channel which are biased with a current sink connected to the sources of M1 and M2. This type of configuration of M1 and M2 is known as source – coupled pair. M3 and M4 are to show as to how current sink can be implemented.

Table 3.4 CMOS differential amplifier with current mirror load desired specification and achieved result.

Sr no.	Desired specifications	Obtained parameters	Obtained specifications
1	CMRR > 40 dB	W1= 8.782556um	CMRR = 44.64408
2	Gain > 25 dB	W2= 63.472698um	Gain= 2.384877e+07
3	PM> 45°	W3 = 54.162553um	PM= 90.36310
4	V_{os} < ±50 mV	I_{bias}= 54.162553uA	V_{os} = -0.0513407
5	Slew rate > 10 V/us	-	Slew Rate =26.08571(+ve) = 14.61205 (-ve)

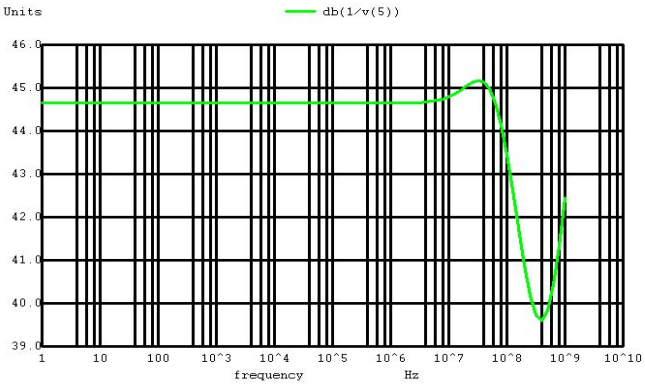

Figure 3.12 Ngspice simulation of CMRR of CMOS differential amplifier

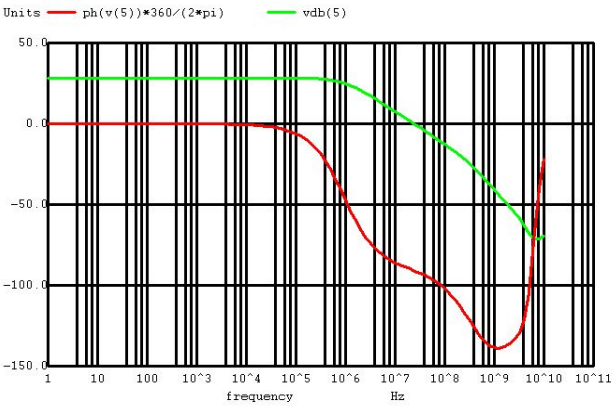

Figure 3.12 Ngspice simulation of gain (db) and phase of CMOS differential amplifier

Figure 3.12 shows the graph of CMRR (Common Mode Rejection Ratio) of the differential amplifier which is constant upto some frequency and the obtained value is . Also, it reveals that obtained parameters here (CMRR) meet the desired specifications which can be matched with the values given in Table 3.4.

Figure 3.12 shows the Ngspice simulation graph of gain (db) and phase of the differential amplifier.Also, it reveals that obtained parameters (gain and phase) meet the desired specifications which can be matched with the values given in Table 3.4.

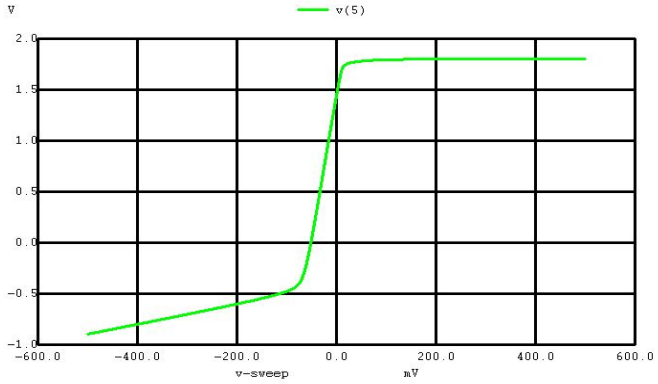

Figure 3.13 VTC of CMOS differential amplifier

Figure 3.13 justifies the Voltage Transfer characteristics of CMOS differential amplifier (Vos) and its value is 0.0513407 V.

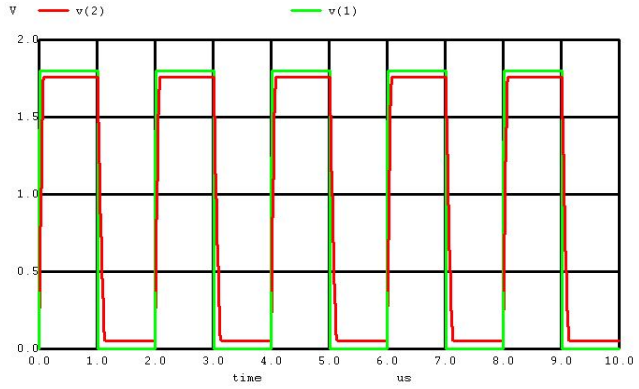

Figure 3.14 Ngspice simulation of slew rate of CMOS differential amplifier

Figure 3.14 shows the simulation of input/output of CMOS differential amplifier. This simulation is performed to measure positive and negative slew rate. here Positive slew rate is 26.08571 and negative slew rate is 14.61205 .

IV. CONCLUSION AND FUTURE WORK

In this paper, analog circuits are designed for optimization using TSMC 180 nm technology and the entire setup is being on Ubuntu operating system. DEalgorithm approach has been used to test various analog circuits to obtain the optimized design. Different specifications of the various analog circuits are previously defined in the entire optimization process and the results so obtained are matched to the desired specifications.

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