An Area-Efficient Carry Select Adder Design using CMOS Technology

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Abstract – Many opportunities were created for increasing the speed and reducing the area of any data processor which presented here because of the Design of High efficiency Carry Select Adders using SQRT (Square Root) technique.Adders are one of the extensively used digital components in digital integrated circuit design. Only CSLA is the fastest Adder which is used in many data processing processors which performs fast arithmetic operations. The basic operation is addition which is used in almost all computational systems. Hence, the efficient implementation and design of arithmetic unit needs the binary adder structure to be implemented in an equally efficient manner. A ripple carry adder has smaller area and it has also got less speed. A carry look Ahead adder is faster though its area requirements are quite high. BEC is the efficient novel carry select Adder proposed here actually provides good compromise between cost and performance and thereby establish a proper trade-off between time and area complexities. In the proposed work Tanner EDA tool is used for the designing of all adders containing Ripple carry adder, Binary to Excess One Convertor and Multiplexers. With the help of Multiplexer Circuit we can select the correct output result according to the logic state of the Carry-in Signal.

Keywords: Carry Select Adder, Ripple Carry Adder, and Binary to Excess one Converter, Square root Carry Select Adder, and Very Large Scale Integrated Circuits for Hardware Description Language, Hardware-sharing and Boolean Logic.

I. INTRODUCTION

In the upcoming years, the rising demand for high-speed arithmetic units in micro-processors, image processing units and DSP chips has cleared the path for development of high-speed adders as addition is a requisite operation in almost every arithmetic unit and also it acts as the basic building block for synthesis of all other arithmetic computations. To increase the convenience of the system, battery life, area and power are the critical factors of concern. Even in servers and personal computers (PC's), power dissipation is a key design parameter. In today's situation, design of area efficient and power efficient high speed logic systems are the one of the decisive areas of research in VLSI design. In digital adders, the speed of addition is restricted by the time required for the carry to propagate through the adder. In the present scenario, there is a vital need that computations should be performed using low power and an area efficient circuit that must operate at higher speed which is reachable with lesser delay because of which the efficient adder implementations becomes an inevitability. Depending on the parameters required such as area, delay and power consumption, several adders can be implemented which are been proposed. In this project, qualitative evaluations of the classified binary adder architectures are given. CMOS design of Ripple Carry Adders, Carry Select Adders and Carry Look Ahead adders are needed to emphasize the common performance properties which belong to their classes. In the following section, we give a brief description of the studied adder architectures. The leading class consists of the very slow ripple carry adder with the smallest area. In the second class the carry skip adder, carry select adders with multiple level have small area requirements and short computational times. From the third class the carry look Ahead adders and from the fourth class the parallel prefix adder represents the fastest addition schemes with the largest area complexities.

II. SYSTEM MODEL

In this section the ripple carry adder is constructed by cascading each single-bit full-adder. In the ripple carry adder, each full-adder starts its computation till the previous carry-out signal is ready. Therefore, the critical path delay in a ripple carry adder is determined by its carry-out propagation path. The critical path is the n-bit carry propagation path in the full-adder circuits. As the bit number n increases, the delay time of the ripple carry adder will also increase accordingly in a linear manner. In order to improve the shortcomings of the ripple carry adder the following figure shows how to remove the linear dependency between computation delay time and input word length of the carry select adders. The ripple carry adder is divided into m parts by the carry select adder (CSLA), while each part consists of a duplicated (n/m) per-bit ripple carry adder pair. This duplicated ripple carry adder pair is therefore needed to anticipate both possible carry input values, where one ripple carry adder is calculated as carry input value represented as logic zero level and another ripple carry adder is calculated as carry input value as logic one level. When the actual carry input is ready, either the result of carry zero path or the result of carry one path is selected by the multiplexer according to its carry input value. To anticipate both the possible carry input values in advance, the start of each m part ripple carry adder pair no longer needed to wait for the coming

of previous carry input. As a result, each m part ripple carry adder pair in the carry select adder can compute in parallel. In this way, the critical path of n bit adder can be reduced significantly.

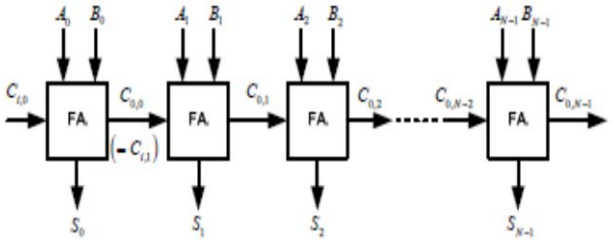


Fig. 2.1 The n-Bit Carry Ripple Adder Constructed By N Set Single Bit Full-Adder

III. PREVIOUS WORK

In the previous article related to low power & an area efficient CSLA published some new parallel FIR filter structures were represented which were beneficial to the symmetric convolutions where there were multiple number of taps for example 2 or 3. Here the conventional n-bit ripple carry adder design shows how the critical path is n-bit & the carry propagation path plus the one summation generation stage. Alternatively, the critical path is (n/m)-bit carry propagation path plus m stage multiplexer with one summation generated stage in the n-bit which is the carry select adder. Since m is much smaller than n and the delay in the multiplexer circuit is smaller than that in the full adder, the computation delay in the carry select adder is much shorter than that in the ripple carry adder. However, while implementing the adder with duplicated carry generation circuit it costs almost twice as compared to hardware and two times power consumption as compared with the ripple carry adder circuit.

Therefore this paper has proposed an area-efficient carry select adder by sharing the common Boolean logic term to remove the duplicated adder cells in the conventional carry select adder. In this way, it was shown here that we can save many transistor counts and achieve a low Power Dissipation as compared with the conventional carry select Adder, the speed is a little slower since the parallel path in our design is shorter. However, we can achieve lower area, lower power consumption, and low Power Dissipation. As compared with the ripple carry adder, the speed can be faster because some of the parallel architecture in the conventional carry select adder is retained. The delay time in our proposed adder design is also proportional to the bit number n however; the delay time of multiplexer is shorter than that of full adder circuit.

Consequently, our area efficient adder can perform with nearly the same transistor counts, nearly to the same power consumption, but with faster speed and lower Power Dissipation as compared with the ripple carry adders.

IV. PROPOSED METHODOLOGY

In this section all the arithmetic operations such as addition, subtraction, multiplication, and division are the basic operations which are to be implemented in digital computers using basic logic gates for example. AND, OR, NOT, NOR, NAND, EX-OR, EX-NOR etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication, subtraction and division .Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs Carry input which is the Carry output of the previous adder. This kind of adder is **a** Ripple Carry Adder, since each carry bit "ripples" to the next full adder. The first full adder may be replaced by a half adder. The block diagram of 16-bit Ripple Carry Adder is shown here below- author need to mention his simulation/experimental research model with neat block diagrams and flow charts.

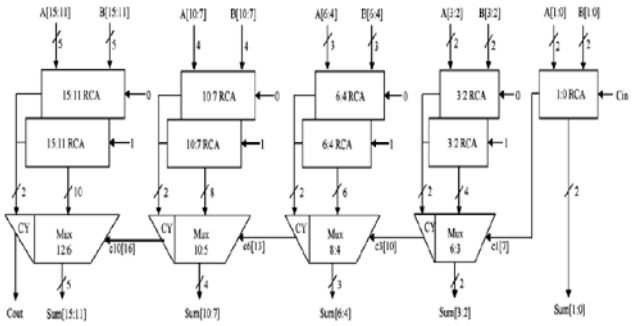


Fig 4: - Regular 16 bit Carry Select Adder using RCA

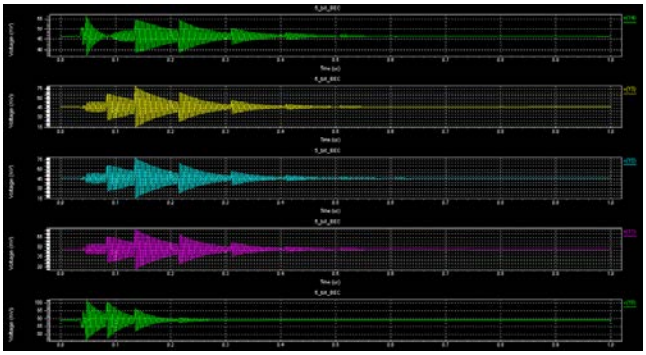
Delay and Area Evaluation methodology of CSLA, using ripple carry adder and CSLA using BEC-1 is as shown in the following table given below. In 16-bit CSA the area is increased as compared to regular CSLA and modified CSLA modified CSLA. In 16-bit SQRT CSLA moderate area is required as compared to CSA and CSLA using RCA. Delay is reduced by using 16-bit SQRT CSLA as compared to 16-bit CSLA using RCA .The n 16-bit SQRT CSLA moderate area is required as compared to CSA and CSLA using RCA. Delay is reduced by using 16-bit SQRT CSLA as compared to 16-bit CSLA using RCA

.The comparative values of Voltage, Static Current and power shows that the number of Multiplexers required will be same but the gate counts of the overall circuit will get reduced due to Binary to excess-1 convertor as it requires less number of gates.

V. SIMULATION/EXPERIMENTAL RESULTS

In this section it has been explained about the experimental/simulation results with graphs and appropriate tables. The following simulation results show the simulation result of 5- Bit BEC. The results are carried out at 1.2 Volt supply voltages and average power consumption and delay at sum and carry output and the findings.

SIMULATION RESULT OF 5-BIT BEC



DESIGN OF 16-BIT SQRT CSLA USING BEC

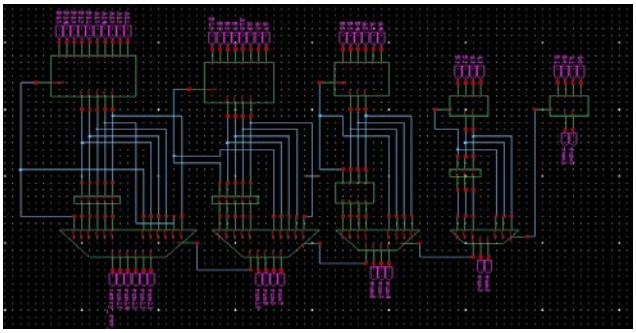


TABLE 1. COMPARISON IN TERMS OF DELAY/AREA

Sr. No.	Parameters	16-Bit CSLA using RCA	Modified 16-Bit CSLA using BEC
1.	Voltage(Volts)	0.8	0.8
2.	Static Current(Amp)	2.45	7.745
3.	Power(Watts)	1.963	6.196

VI. CONCLUSION

In this paper a proposed simple approach is shown that how Area and delay reduces of Square Root Carry Select Adder using Binary to Excess-1 architecture. The Ripple Carry Adder with Binary to Excess one Converter in the structure is a great advantage for reducing the number of gates. The results are as shown in comparison table which states that the modified 16-bit Square Root Carry Select Adder has a slightly large area for lower order bit which reduces for higher order bit and also delay is reduced to a great extent. Thus the result shows that using modified method the area and delay will decrease so it is a good alternative for adder implementations in many data processors.

VII. FUTURE SCOPES

The work can be extended up-to 64-Bit Adders. The research steps may be taken which leads further to optimize the parameters such as frequency, capacitance, length, width etc. The work can be extended to change the technology file. The efforts can be made to decrease the transistor counts so that the parameters like Power, Area and Delay might be changing. Research steps can be taken by using the other types of Adders like Carry Select Adder, Hybrid Adder etc.

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