Delayed Clock Pulse Triggered Modified Latch Low Power Shift Register Using GDI Technique

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Abstract - Now a day's, the main challenge in front of VLSI System designer are to design a low power area efficient integrated circuit. And the Shift register is basic functional unit in digital circuit and image processing such as digital filers, communication receivers and image processing ICs. So the performance such VLSI circuit dependents on the performance of the Shift register. And the shift register composed of series connected flip-flops. And the smallest flip-flop is suitable for shift register to reduce the area and power consumption. In this paper we use the pulse latch in place of flip-flop because a pulse latch is much smaller than flip-flop. The design and simulation of modified latch and Delayed clock pulse generator is done using Tanner EDA 13 TOOL in 35nm technology.

Keywords: Flip-flops, Pulse Latch, GDI (Gate Diffusion Input), Delayed clock pulse generator, Integrated Circuit (IC).

I. INTRODUCTION

The Shift Register is a type of sequential logic circuit that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock cycle, hence the name shift register. A shift register is a register in which binary data can be stored and shifted either left or right. The data is shifted according to the applied shift signal, often there is a left shift signal and a right shift signal. A shift register (shown in figure 1) generally constructed using flip-flops (i.e. edge triggered devices). Several D flip-flops may be grouped together with a common clock to form a register. Because each flip-flop can store one bit of information, a register with n D flip-flops can store N bits of information. But in recent flip-flops is replaced with pulsed latches for compacting the layout dimensions because pulse latch is smaller than a flip-flop. By using multiple non overlapping trigger signal timing problem between pulse latch is solved.

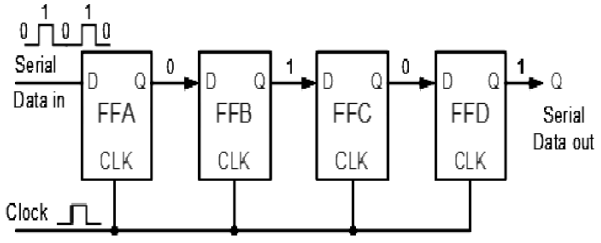
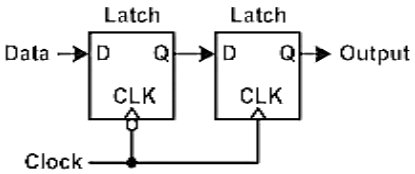


Fig. 1. Block diagram of Shift Register

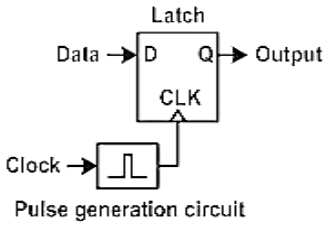
II. ARCHITECTURE

a. PULSE LATCH

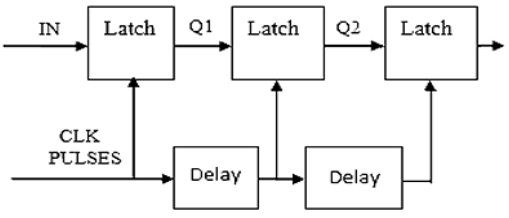
Pulse latch is used in place of master-slave flip-flop using two latches in figure 2.1 (a) and (b) which reduced the area and power consumption half of master-slave flip-flop. But due to timing problem pulse latch cannot be used in shift register. Delay should introduce either between latches or clock pulse for solving timing problem. It has two inputs data (D), clock (CLK) and a output (Q).



(a)



(b)



(c)

Fig. 2.1 (a) Flip-flop, (b) Pulsed Latch (c) Pulsed latch

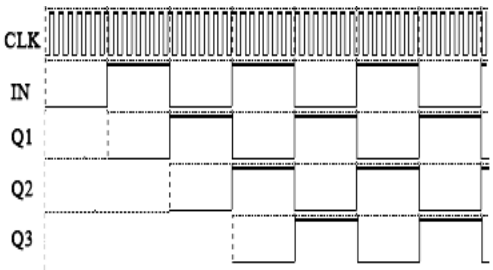
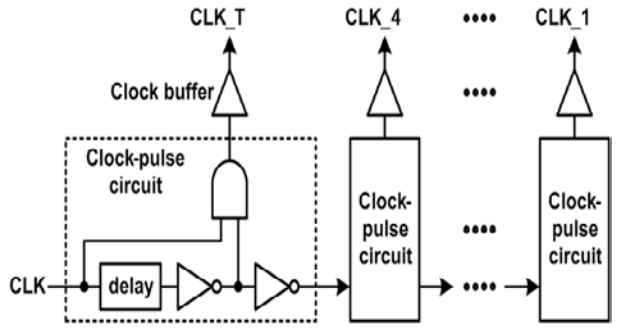


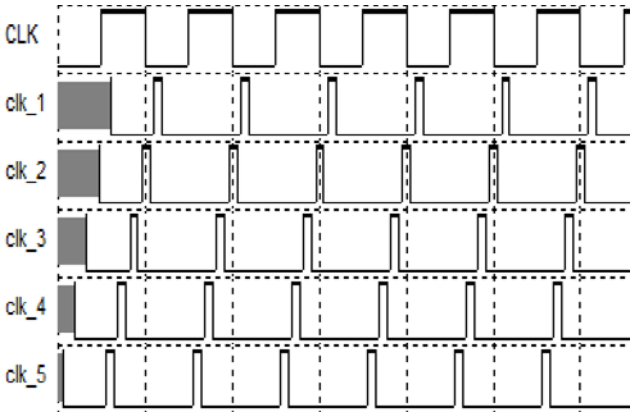
Fig. 2.2 Waveform of Pulsed latch with delay.

b. Delayed pulse generator

For multiple non-overlap delayed pulse clock generation requires non-overlapped Delayed clock pulse generator shown in figure 2.3 (a) with a source clock. The pulse width is chosen such that it facilities the transition. Data transition waveform shown in figure 2.2. Figure 2.3 (b) shows the waveform of Delay pulsed clock generator.



(a)



(b)

Fig. 2.3 (a) Delayed pulsed clock generator (b) Waveform of Delay pulsed clock generator.

III. PROPOSED METHODOLOGY

The modified latch uses two cross-coupled inverters in figure 3.1 which consist four transistors and update the data with two NMOS transistors N_1 and N_2. It have two differential data inputs D, Db and a clock signal CLK. When clock signal CLK is high both N_1, N_2 turns ON and the input data D, Db is updated. On the contrary when clock signal is low both N_1, N_2 turns OFF. It uses less amount of transistor than SSASPL.

Delayed clock pulse generator is implemented similarly shown in figure 2.3 (a) with some modification. In proposed delayed clock pulse generator mod-GDI technique is used for anding clock inputs for generation of non-overlapped delayed clock pulse. Figure 3.1 and figure 3.2 illustrate the schematic of proposed latch and Delayed clock pulse generator respectively. Both of these reduced the average power, static power, dynamic power and area.

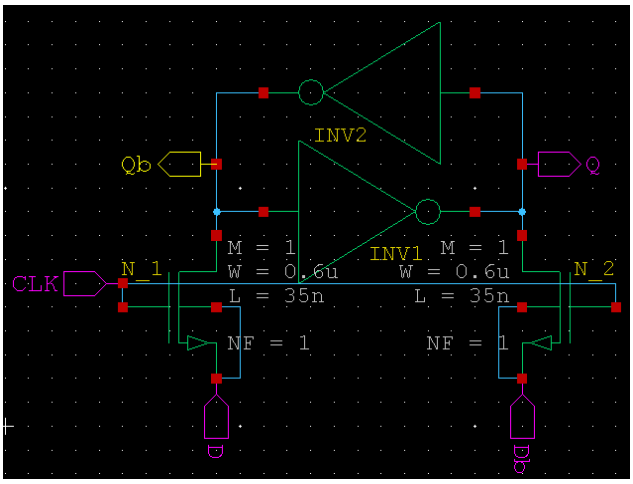


Fig. 3.1 Schematic of proposed Latch.

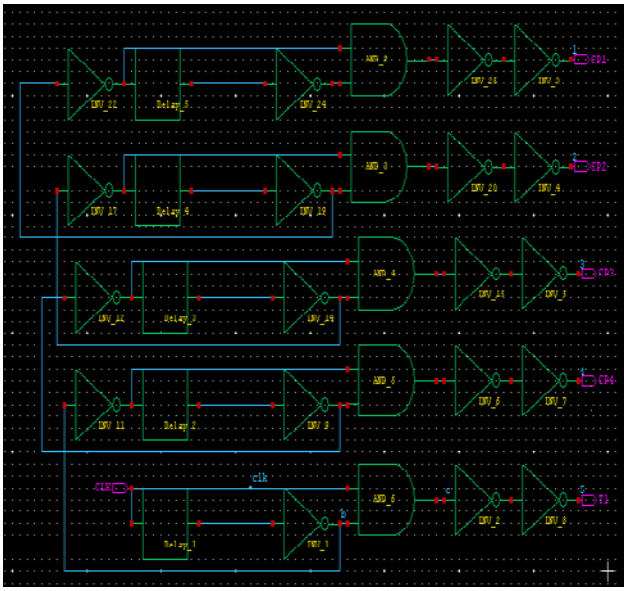


Fig. 3.2 Schematic of proposed Delayed clock pulse generator.

IV. RESULTS AND DISCUSSION

This paper describes the design and implementation of power efficient modified D-latch and Delayed clock pulse generator using GDI AND gate in 35nm technology using Tanner EDA 13. The table 1 and table 2 shows the performance parameter of Latch and Delayed clock pulse generator respectively. Figure 4.1 and figure 4.2 illustrates the input-output waveform of Latch and Delayed clock pulse generator respectively.

TABLE 1. PERFORMANCE PARAMETER COMPARISON OF LATCH.

S. No.	Parameters		SSASPL	Proposed Latch
1.	No. of Transistor	Total	7	6
		clock	1	2
2.	Total power consumption		3.3	0.62
3.	Power consumption of data path (uW)		2.57	0.58
4.	Power consumption of clock load (uW)		0.73	0.04

TABLE 2. PERFORMANCE PARAMETER COMPARISON OF DELAYED CLOCK PULSE GENERATOR.

S. No.	Parameters	Clock pulse generator	Proposed Delayed clock pulse generato
1.	No. of Transistor	14	10
2.	Power consumed by each clock pulse circuit (uW)	27.6	2.53

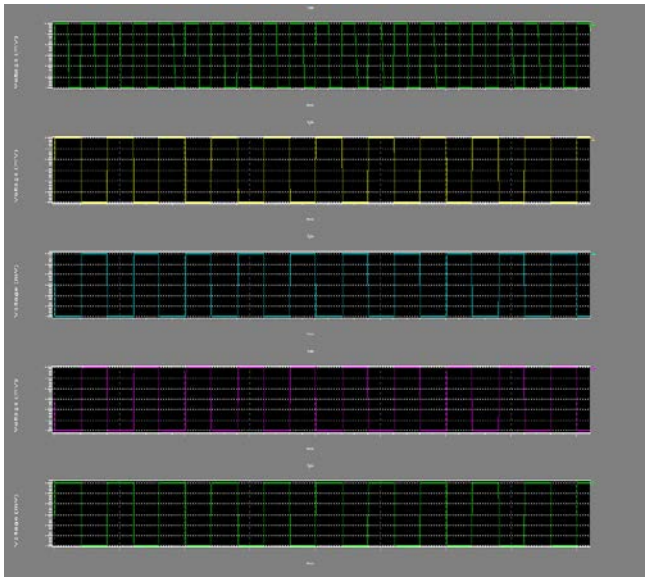


Fig. 4.1 Latch input-output waveform.

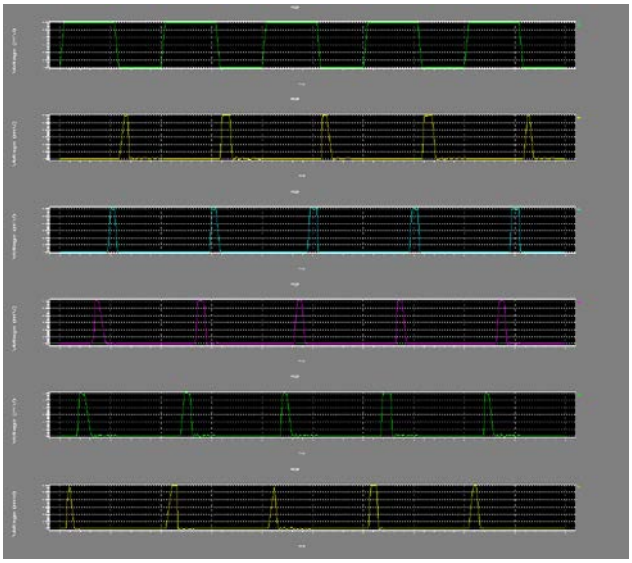


Fig.4.2 Delayed clock pulse generator waveform.

V. CONCLUSION AND FUTURE WORK

In this paper we have proposed power efficient modified latch and Delayed clock pulse generator using GDI AND gate in 35nm technology using Tanner EDA 13 Tool. Since our objective was power consumption for modified latch and Delayed clock pulse generator is found to be 0.62uW and 21.07uW respectively, hence we achieved our objective. In this paper we design modified latch without using MTCMOS. If design a latch with MTCMOS can leads to enhance overall performance by reducing leakage current.

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