A Novel High Noise Immune Dynamic Logic Design for Portable Devices

Deepak Kumar Singh[1] and Shweta Agrawal[2]

[1]*Research scholar,* [2]*Assistant Professor,*

Electronics and Comm. dept., SRCEM Banmore, Morena, India

***Abstract*—the huge functionality on the modern portable devices demands high speed signal processing. The dynamic logic provides area and performance efficient designs but exhibits poor noise immunity. Moreover, this noise immunity is further degrading with each technology due to scaling of the devices. Hence, technique is required to improve the noise immunity of the dynamic logic so that bulkier CMOS circuits can be replaced by the smaller dynamic circuits. This will result in significant reduction in the cost of device and simultaneously improve the performance of the device. This work explores the existing noise immunity techniques and presents a novel noise immunity improvement design. In order to evaluate the effectiveness of proposed technique, all these techniques are implemented in Tanner and extracted net list is simulated with 45nm PTM technology node. The simulation results show that proposed technique provides 2.98% higher noise immunity over the existing designs.**

Keywords: **Dynamic Logic, Noise Immunity, VLSI, Noise Margin.**

I. INTRODUCTION

The modern portable devices demand low power and area efficient design to perform complex tasks with the limited battery. The conventional static CMOS logic does not provide both the benefits as area of implementation is very high. The dynamic logic can improve the area and performance while maintaining the power budget [1].The dynamic logic exploits charge storage capability of the CMOS devices even after removal of the power supply [2]. The charge storage phenomena exist primarily due to various capacitances present in the internal nodes of the circuit. However, these stored charges at the soft nodes gradually leaks away after some time due to charge sharing problem and sub-threshold leakage current [3]. The major drawback of the dynamic logic is its poor noise immunity which demands noise immunity techniques to improve the robustness.

In the literature, significant efforts have been given to achieve high noise immune dynamic logic [4] that ranges from the traditional approach of simple keeper logic and pre-charging internal node to high performance delayed logic, Twin transistor technique etc. A keeper transistor [5] is a weak transistor which supplies a small amount of current to the dynamic node of the circuit. PMOS transistor's base is tied to the ground and is therefore always on. This is advantageous as the keeper makes up for the loss of charges at the dynamic node during evaluation phase and increases the noise tolerance of the circuit.

Novel low power noise tolerant high performance logic to improve the noise tolerance of the dynamic logic is reported in [4]. The paper presents immunity improvement technique using feed through logic (FTL). It improves the performance of the arithmetic logic which exhibits higher logic depth. The proposed technique removes the limitation of conventional FTL logic of charge sharing and improves the performance. The conditional clocking technique is proposed by Mazumdar et al [5] which comprises of two transistors M1 and M3 and an AND gate to conditionally clock the lowermost transistor MN2. The delayed logic comprises of an additional delay circuitry which provides sufficient delay between CLK and DCLK signals. MN1 has been used as a stacking transistor and no input or clock signals have been used to pre-charge any internal node in order to avoid additional capacitive loads. The rest of the paper is organized as follows:

Basics of dynamic logic are detailed in Section II. Whereas Section III, presents the existing noise immunity techniques and Section IV deals with the proposed high noise immunity design. Thereafter, Section V provides a comparative analysis of proposed noise immunity technique using simulation over existing techniques. Finally, Section VI deals with the conclusion and Section VII show any future work that may be investigated.

II. BASICS OF DYNAMIC LOGIC DESIGN

Dynamic Logic Design and Challenges

Large number of transistors in static CMOS circuits increases silicon area. Also the CMOS logic exhibits more delay and power consumption due to the presence of large node capacitances in VLSI circuits. The dynamic CMOS logic circuits [1] offer significant advantages as compared to their static counterparts. The generalized architecture of the dynamic logic is shown in Fig. 1.

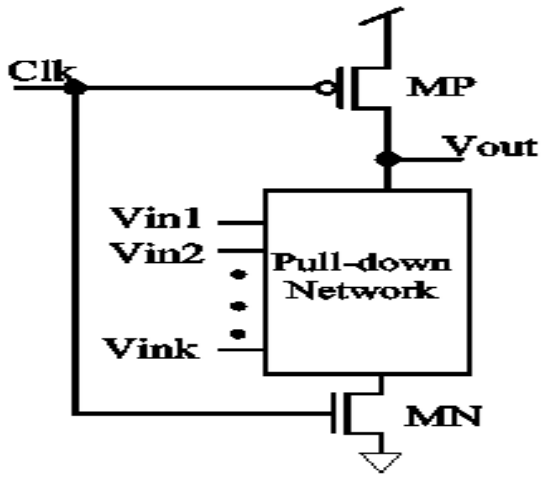

Fig 1: Circuit diagram of dynamic logic

Dynamic logic operation [6] is based on first pre-charging the internal node and then evaluating the node depending on the combination of the inputs applied as shown in Fig. 2. Pre-charging the output node starts when the clock signal is low which ensures that PMOS transistor is ON and NMOS transistor is OFF. This stores logic '1' at the output node. However, evaluation starts when the clock signal is high, thereby making the PMOS OFF and NMOS ON. During evaluation phase, the output node may remain either at logic '1' or may discharge to logic '0' depending on the input combination.

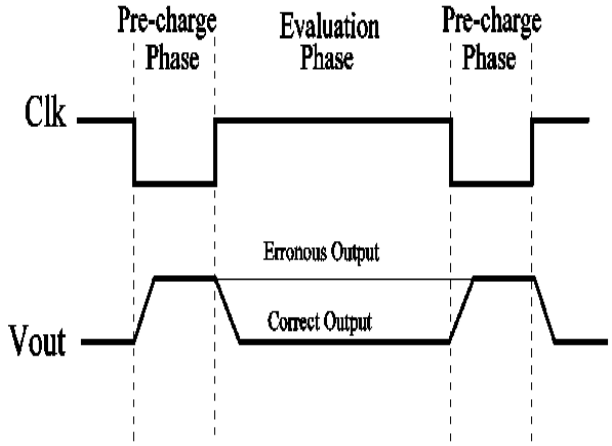

Fig. 2: Pre-charge and evaluation phase in dynamic logic

Moreover, due to the rapid scaling of CMOS devices, threshold voltage is also scaling with the supply voltage. This is a severe concern as the reduction in threshold voltage directly affects the noise immunity of the circuit more in dynamic logic. This is due to the fact that the switching threshold depends on the threshold voltage (V_{th}) of the MOS transistors in the pull down network (PDN) as compared to $V_{dd/2}$ in the static circuit [7]. In other words, the noise margin of the dynamic logic reduces significantly which in turn degrades the faithful operation of the circuit.

Domino Logic

Domino logic is the practical design implementation of dynamic logic in multistage designs where a static inverter is added at output node as shown in Fig. 3.

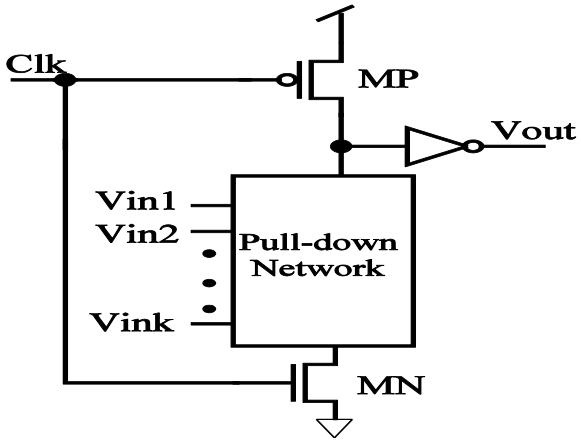

Fig. 3: Generalized domino CMOS Logic

In the domino logic, the inverter can at most make only one transition i.e. from logic 0 to logic 1 during the evaluation phase. This makes it suitable for multistage operation whereby all the input transistors of the subsequent stages are turned off during the pre-charge phase as the inverter output is logic 0 during that phase. Limitations of domino CMOS logic:

- It can only be used to implement non-inverting structures and if required, inversion needs to be carried out by using conventional CMOS logic.
- Charge sharing between the intermediate nodes of NMOS logic block and the output node may cause erroneous output during evaluation phase. Charge sharing is a noise that affects the performance of dynamic CMOS logic circuits as explained in the next section.

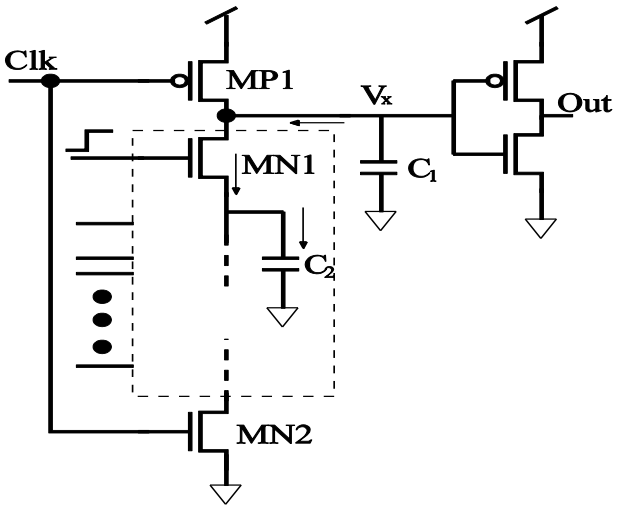

Fig. 4: Charge sharing phenomena in domino logic

Charge Sharing

Charge sharing is the major cause of noise in dynamic logic in which output node shares it charge to intermediate logic node charge. As shown in Fig. 4. The redistribution of charge reduces the amount of charge at the output node which in-turn reduces the voltage level and the output node may false change its state.

Let the output node charge with capacitance C1 is shared with logic intermediate node capacitance C2. Therefore, after charge sharing, the output node voltage is:

$$V_x = V_{dd} * \left[{}^{C_1}/_{C_1 + C_2} \right] \quad (1)$$

$$= {}^{V_{dd}}/_{(1 + {}^{C_2}/_{C_1})} \quad (2)$$

The node voltage becomes half if both capacitances are of equal size. This significantly reduces noise immunity.

III. PREVIOUS WORK ON NOISE IMMUNITY TECHNIQUES FOR DYNAMIC LOGIC

This section presents detailed review on different noise immunity techniques.

Keeper Logic

In this noise immunity improvement technique an additional transistor is connected to provide small current to the output node of dynamic logic [8]. node and increases the noise tolerance of the circuit.

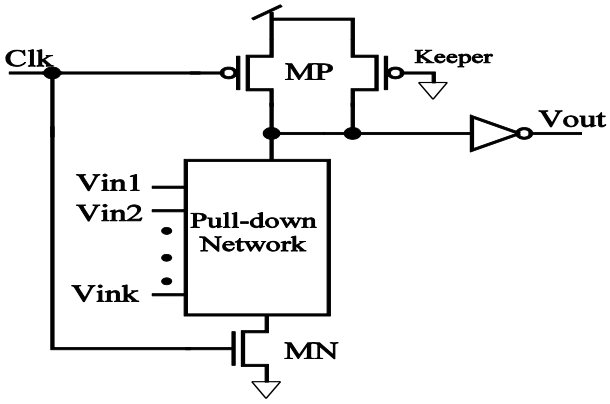

Fig. 5: A simple keeper topology

The PMOS gate is tied to the ground and is therefore always on as shown in Fig. 5. This is advantageous as the keeper makes up for the loss of charges during evaluation phase at the dynamic

Delayed Clocking Technique

As proposed by Mazumdar et al. [9], an additional delay circuitry which provides appropriate delay between the original clock (CLK) and delayed clock (DCLK) signals is connected as shown in fig. 6. During pre-charge phase, the dynamic node is charged to logic high. As shown in fig. 7, DCLK remains low in stage I and transistor MP1 is on and MN1 is off which prevents the charge sharing at this stage. During stage II the CLK becomes '1' which turn ON transistor MN1 which in turn initiates the evaluation phase. At this stage, however, the delayed clock is still low keeping the transistor MN2 off and ensuring that the charge at dynamic node is maintained. At stage III, DClk goes high ensuring that the output node is evaluated depending on the input combination. This stage is defined as the transparency window during which an input combination can evaluate the output node. The width of transparency window is adjusted by the delay circuitry to provide a better noise immunity.

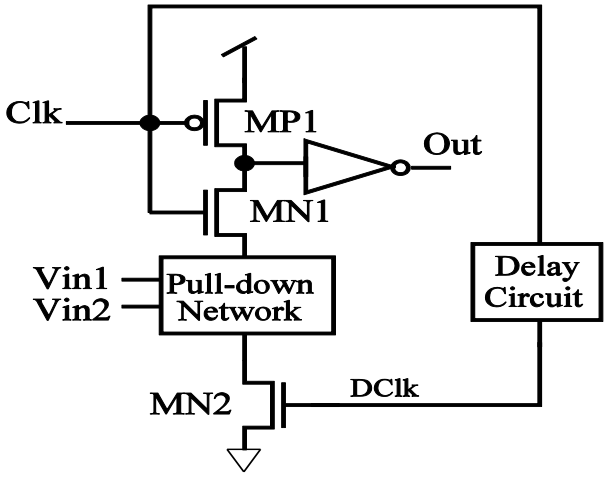

Fig. 6: Delayed Clocking Technique

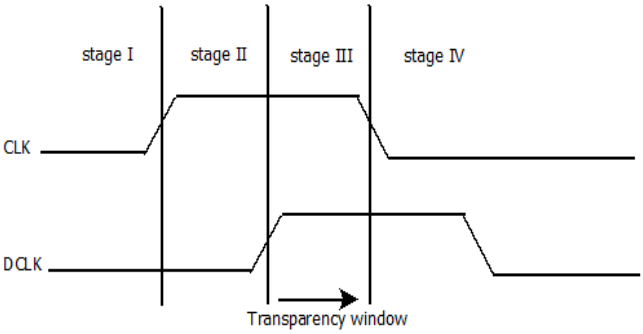

Fig. 7: Different stages in delay logic

Mirror Technique

As presented by Wang [10] two identical NMOS circuits in series are used for evaluation and both these circuits receive the same set of inputs as shown in fig. 8. In between the identical nets, an additional transistor M3 is connected which is driven by the output node of the circuit. Output node is charged to logic high during the pre-charge phase through transistor M1. This results in charging the common node V_X to value $V_{DD} - V_{tn}$.

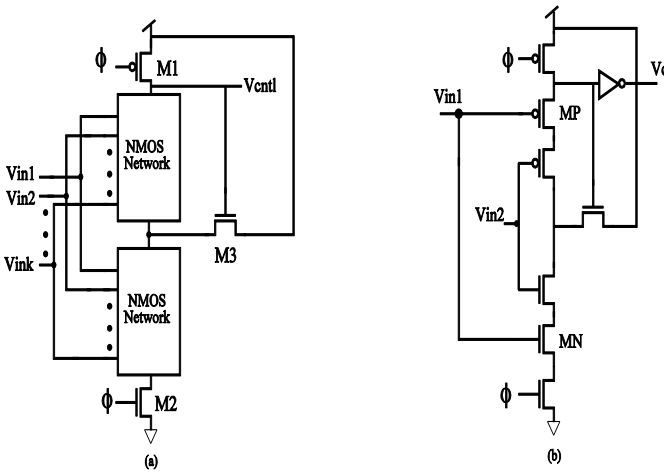

Fig 8: Mirror Technique (a) Block diagram, and (b) AND gate implementation.

The phenomena of body effect raise the switching threshold of the uppermost evaluation network. However, the use of additional NMOS network adds delay to the signal propagation. This emphasizes on careful sizing of transistors in the NMOS evaluation network. Also, the use of a large number of transistors consumes more silicon area for implementing a wide fan in dynamic circuit.

Twin Transistor Technique

A new method of to make the dynamic circuits immune to

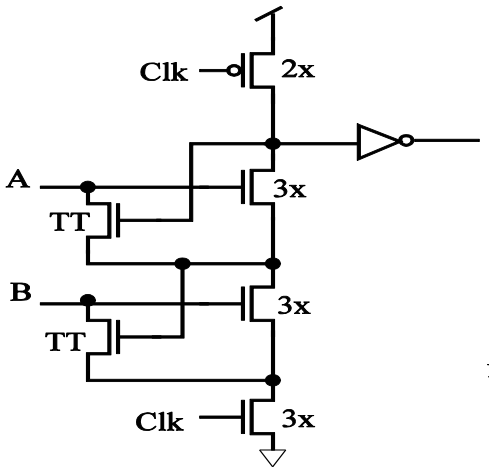

Fig. 9: Twin transistor technique

noise fluctuations was introduced by Ganesh et al [11]. A two input AND gate implementation of the circuit is shown in Fig. 9.

The use of an additional transistor in a cross-coupled manner is called the Twin-transistor. This arrangement increases the switching threshold of the input transistor and thus increases the noise immunity by raising its source voltage. This configuration also mitigates the charge sharing problem and charging of the internal nodes is invoked only when the input combination in the pull-down network leads to a potential charge sharing problem. However, the use of additional transistor at the input of the circuit increases the internal node capacitance and thereby the delay of the circuit which is to be traded-off by increasing the size of the transistors in the pull-down network. This again leads to a compromise between delay and area of the circuit.

Mendoza Technique

A new noise tolerance improvement technique as shown in Fig. 8 which improves the noise immunity of the TSPC and domino logic significantly is proposed by Mendoza et al. [12].

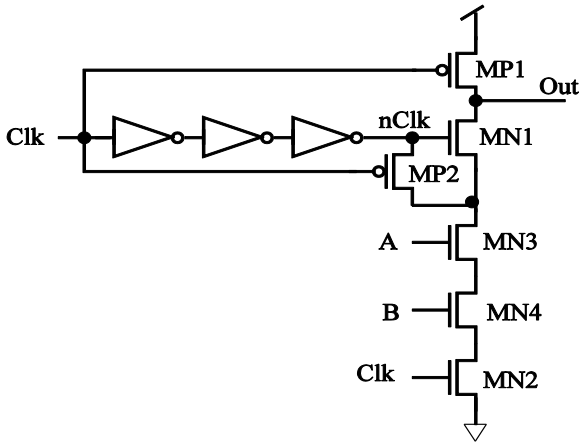

Fig. 10: Mendoza Technique

In this diagram an NMOS (MN1) is inserted between pre-charge node and pull-down network. This transistor is driven by the delayed clock which is generated by considering a chain of inverter (three cascaded connected inverters). Moreover, a PMOS transistor MP2 is added between delay clock input and the pull-down network. This PMOS is driven by the clock supply.

This technique pre-charges the intermediate node and thus reduces the charge sharing problem. The increased potential at the internal node provides the staking effect that results in reduced leakage thus improves the noise immunity.

IV. PROPOSEDHIGH NOISE IMMUNITY DESIGN

This section presents the proposed high noise immunity design followed by its working principle.

Proposed design

The proposed technique as shown in Fig. 11 has been named as Conditional Node Clocking (CNC) technique. In this technique one transistor (MN4) conditionally clocks the internal node Qint through the output node (V_{out}) via an inverter (Inv2). This circuit provides improved noise

immunity without significant increase in area, power and delay metrics. Further the proposed technique does not require multi-threshold or any change in the pull-down network for internal node charging. However, an NMOS (MN3) has been employed to mitigate the effect of charge sharing. The proposed design can be easily employed in the existing dynamic logic designs. Further, the proposed noise tolerant design requires only one additional inverter and two MOS over the domino logic to improve the noise immunity.

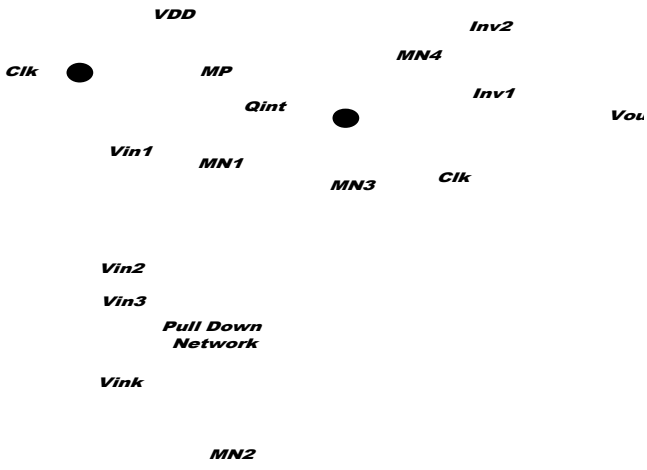

Fig. 11: Proposed noise immunity technique

Working principle

The proposed noise immunity circuit charges the internal node (Qint) only when there is charge on the internal node and the clock is high i.e. during evaluation phase. During the pre-charge phase MN4 remains in off state and the circuit behaves like simple dynamic logic. Moreover, during the evaluation phase, if the node is pre-charged, the charge leakage due to various sources is compensated by the current through MN4. Also, the problem of charge sharing is done away with by using MN3 which feeds the source terminal of first input MOS (MN1). This happens only when clock and the internal node Qint is high which raises the source potential of the first input MOS (MN1) through MN3 during the evaluation phase. Thus, during evaluation if the internal node is to remain high, then MN3 helps in maintaining the charge level at the internal node. The proposed circuit significantly improves the noise immunity without much delay/power overhead as it requires onlyone additional inverter and two MOS over the domino logic. The simulation results in the next chapter show the efficacy of the proposed technique over the existing noise immunity techniques.

V. SIMULATION RESULTS AND ANALYSIS

In order to evaluate the efficacy of the proposed noise immunity technique, the proposed and existing designs are implemented on Tanner and simulated with 45nm technology file [13].

Simulation Environment

To evaluate the design metrics, all the existing designs are implemented in Tanner 14.1 with similar transistor sizing. The 2 input NAND gate is utilized and implemented with dynamic logic employing different noise immunity improvement techniques.

Simulation Results

The schematic of 2-input NAND gate implementation of Keeper technique, Mirror technique and Twin transistor technique on Tanner are shown in Fig. 12, Fig 13 and Fig 14 respectively. Whereas, the proposed noise immunity is shown in Fig. 15.

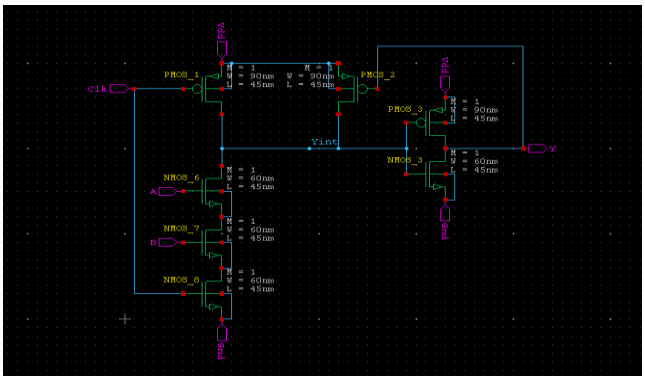

Fig. 12: Schematic Keeper technique

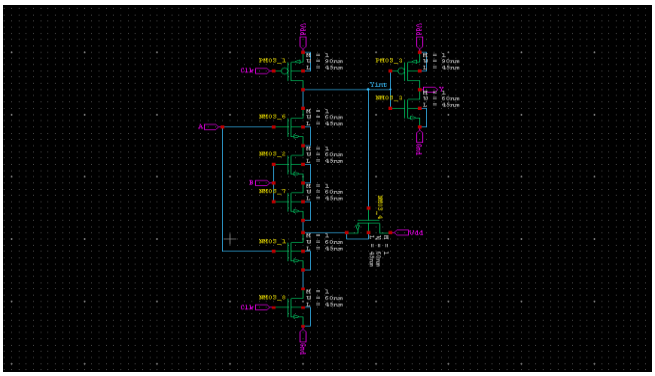

Fig. 13: Schematic Mirror technique

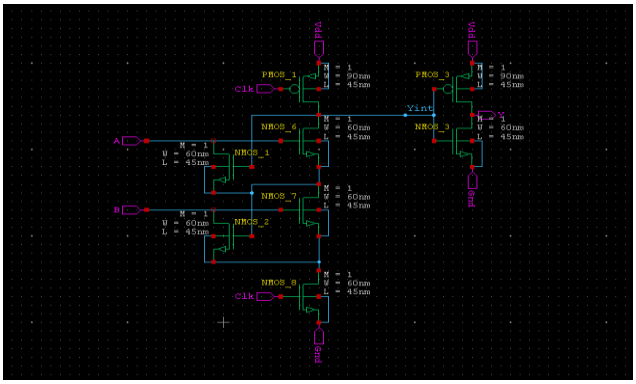

Fig. 14: Schematic Twin transistor technique

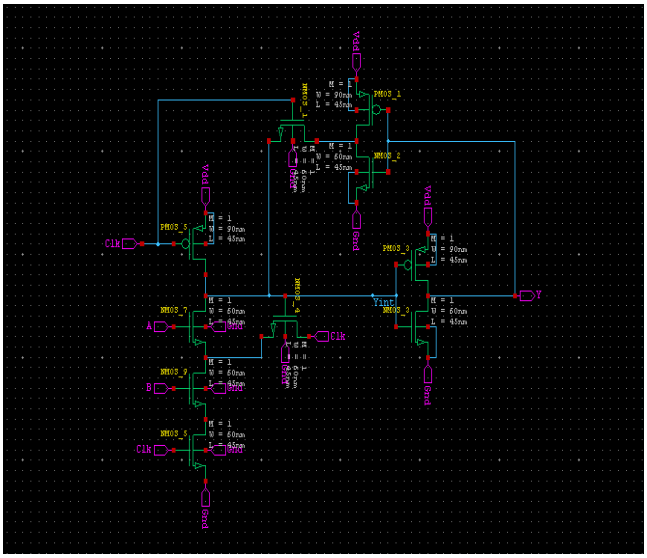

Fig. 15: Proposed noise immunity circuit

The schematic for the above-mentioned logic are implemented and spice net lists are extracted. The various noise immunity techniques implemented on Tanner are simulated to compute design metrics.

Further, noise of different amplitude is supplied at the input and corresponding output is computed to measure the noise tolerance. A noise pulse with increasing pulse width (increasing time of applied noise) and increasing value of noise (increasing the amplitude of the noise) is applied and the flip in the output node is observed. A point at which node value changes, the value of noise pulse width and amplitude is measured. These values are used to compute the noise threshold energy (NTE) and average noise threshold energy (ANTE) as shown in Table 1.

Table 1: Comparison of noise immunity techniques.

Immunity techniques	Performance parameters			Noise Immunity	
	Area (#Tran)	Power (nW)	Delay (ns)	Noise Immunity (ANTE)	Avg. noise Voltage
Keeper technique	7	69.4	0.163	0.88	0.61 V
Mirror Technique	9	52	0.17	0.88	0.61 V
Twin Transistor Technique	8	48.4	0.166	0.98	0.67 V
Proposed technique	10	90.8	0.188	1.033	0.69 V

It can be observed from the results in Table 1 that the proposed technique provides highest noise immunity at the cost of little poor design metrics. The area and power overhead of the proposed and the different existing designs are shown in Fig. 16 and Fig.17, respectively.

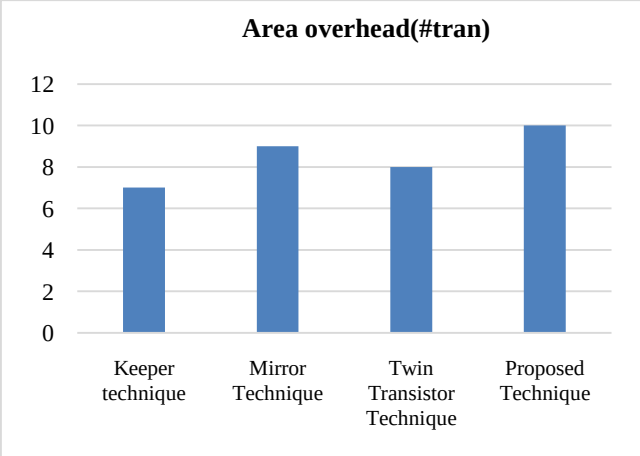

Fig. 16: Area overhead comparison

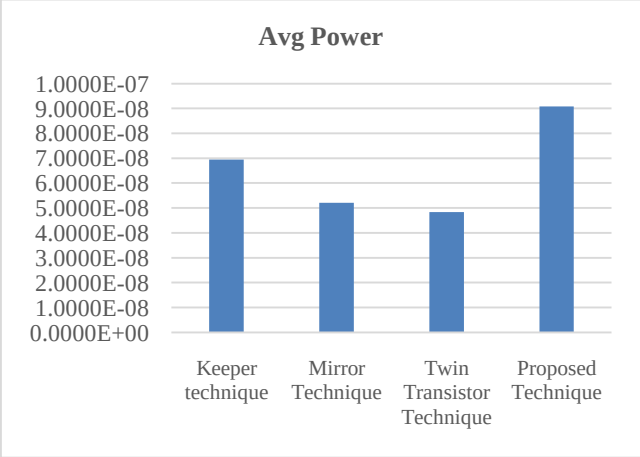

Fig. 17: Comparison of power overhead

The measured noise immunity (ANTE) comparison is shown in Fig. 18. It can be seen from the figure that proposed approach provides highest noise immunity over other existing design techniques.

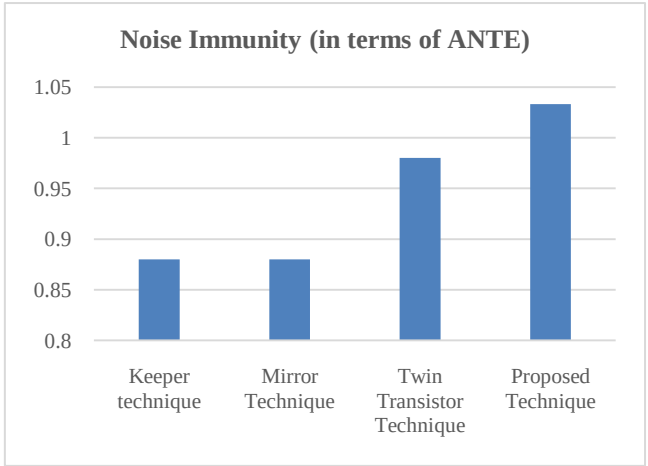

Fig. 18: ANTE for different techniques.

VI. CONCLUSION

The poor noise immunity of the dynamic logic reduces its usage in different portable devices. Therefore; it requires technique to improve the noise immunity of the dynamic logic. This paper presents a novel high noise immunity technique that improves the noise immunity of the dynamic logic significantly. To evaluate the efficacy of the proposed noise immunity technique, all the different existing noise immunity techniques are implemented in Tanner and extracted netlist is simulated with 45nm PTM technology node. The simulation results show that proposed noise immunity technique improve the noise immunity by 2.98% over the best known existing design.

VII. FUTURE SCOPE

Future work includes the design of architectural level approach to mitigate the effect poor noise immunity of the dynamic logic. This architecture may be for example one that detects the error if occurred due to noise and then correct it. In this way we can achieve the overall correct result without failure. Further an analysis of circuit level techniques over the architectural level techniques can be done to find out an optimum design that provides high noise immune dynamic logic. Also, the design metrics of the proposed technique may further be investigated to reduce the area/power overhead.

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