DSRC based FM0/Manchester Encoder-Decoder Implementation on FPGA

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Abstract- The DSRC (dedicated short-range communication) technique is used to associate for tending rising techniques. It used to push the intelligent installation into our existence. By both the FM0 and Manchester codes the DC-balance and enhancement of signal irresponsibleness is effectively adopted, that is the standard for DSRC (dedicated short-range communication). The limit of VLSI Very Large Scale Integration (VLSI) design which we are using in paper used for coding-diversity between the FM0 and Manchester codes which going to seriously limit the potential to complete the reused design. This paper use SOLS (similarity-oriented logic simplification) technique which is used to remove the limitation of the design. The similarity-oriented logic simplification (SOLS) technique is used to improve the utilization of hardware at some rate which presents the FM0 and Manchester encodings technique. In this paper the capability of coding will fully support the dedicated short-range communication (DSRC) which is the standard of America, Europe, and Japan. This paper is not exclusively developed the complete reused Very Large Scale Integration (VLSI) design, though furthermore it exhibits economical performance which compared with the existing works.

Keywords: Dedicated short-range communication (DSRC), Manchester encoder, Miller encoder, SOLS technique, VLSI architecture, FM0 encoder, FPGA.

I. INTRODUCTION

The binary (0, 1) data in the Manchester coding all of the bits are arranged in the exacting sequence. For half duration of the input signal the high voltage is represented as bit '1' and inverted signal will be sending for the next half cycle. In the Manchester format when we are transmitting '0', a low voltage will send for the first half cycle of the signal, and a high voltage will send for the next half cycle of the signal. When the sending of data is in continuous form, the high signals or continuous low signal (e.g.:11110000) is very difficult to calculate the number of 1s and 0s in that data, Because there is no changes in that data from high to low or low to high at particular time period (Here time period is 4xT, where T is the time duration for a single pulse). The detection of that type of data is only possible when we are calculating the duration of the signal time. To overcome this type of problem we use the Manchester format. When we code the signal in the Manchester format the data will always be change the signal from high to low or low to high for each of the bit of the signal. As a result, in the Manchester format the possibility of rate of occurrence of an error in the signal is very low. So it is easy in Manchester format at the receiver to detect the error in the data. It is a collectively conventional digital data encoding technique for the signal.

The DSRC (dedicated short range communication) is the procedure used for one way or two way medium range communication. The dedicated short range communication (DSRC) architecture is briefly classified into two categories: automobile-to-roadside and automobile-to-automobile. In automobile-to-automobile, the dedicated short range communication (DSRC) enables the sending of message and broadcasting the automobile. The focuses of automobile-to roadside are on the IT (intelligent transportation) service, such as ETC (electronic toll collection).The dedicated short range communication (DSRC) architecture having the transceiver. As shown in the figure 1.1 the microprocessor is used to transfer the instruction to RF front end and the baseband processing. The RF front end of the microprocessor is used to transmit and receive the wireless signals from antenna. The baseband processing is responsible for different type of process such as error correction, modulation, encoding and synchronization of the signals. The transmitted signal is in the form of the arbitrary binary (0, 1) sequence.

It is very difficult to obtain the dc-balance from the FM0 and Manchester which provides the transmittion of signal and then it provides the dc-balance. The similarity oriented logic simplification (SOLS) techniques have two methods: (a) Area compact retiming and (b) Balance logic operation sharing. The area compact retiming is used for reducing the transistors count. The balance logic operation sharing is used for combining the FM0 and Manchester encoding.

The architecture system of dedicated short range communication (DSRC) transceiver is shown in Figure 1.1 The upper part dedicated for transmission and bottom parts are dedicated for the receiving. The transceiver is classified into three modules: baseband processing, microprocessor, and RF front-end. The instructions of microprocessor interpret to schedule the tasks of baseband processing and RF front-end from media access control.

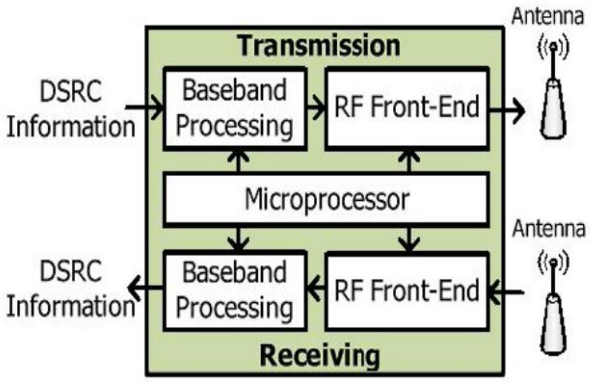

Fig. 1.1 System architecture of DSRC Transceiver

The baseband processing is dependable for of the error correction, modulation, and encoding and clock synchronization. The RF front end used to transmits and receives the wireless signal through the antenna.

II. LITRATURE REVIEW

The architecture of very large scale integration (VLSI) of FM0 and Manchester encoders are reviewed as follows [1] proposed by using SOLS technique which is fully reused the Very Large Scale Integration (VLSI) architecture for both FM0 and Manchester encoding. Some parameters are proposed some method to works as maximum operating frequency, TSMC, Power consumption etc. [2] is used to introduced the input of MUX−1which causes the logic-fault of the coding. This type of problem is solved by using the XNOR with the inverter.

The work in [3-6] presents review paper to estimate the different forms of Dedicated Short Range Communication (DSRC) system which is based on both the FMO and Manchester encoding by using SOLS technique. It also compares thees techniques with the any other techniques. [7, 8] proposed by using SOLS technique which is fully reused the Very Large Scale Integration (VLSI) architecture for both FM0 and Manchester encoding. The SOLS technique improves the utilization of hardware at the rate from 57.14% to 100% for both FM0 and Manchester encodings technique.

[9] proposed a system to minimizing the problem of coding-diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. Area compact retiming and balance logic operation sharing are the two core techniques that are used to eliminate the limitation on hardware utilization by reducing the number of transistor and by combining the resources of FM0 and Manchester encodings. This paper is realized in 180nm technology with outstanding device efficiency. The power Consumption is 29392.843nW for Manchester encoding and FM0 encoding.

Design in [10] proposed to overcome the technique of utilization of hardware by using the SOLS technique of the Very Large Scale Integration (VLSI) which is used to design the DSRC (dedicated short-range communication). The utilization of hardware by SOLS technique improves the rate of utilization from 14% to 100% for each FM0 and Manchester encodings. [11] proposed a method of utilization of VLSI (very large scale integration) architecture which is used for the reduction of power by using both the FM0 and Manchester encoding. The power consumed is 0.72 mw for Manchester encoding. For Manchester encoding the consumption of power is 0.72 mw. [12-15] the paper presents the diversity coding technique between the FM0 and Manchester encoding. By the SOLS technique the hardware improvement rate is of 57.14% to 100% for both the techniques of FM0 and Manchester encodings.

Paper [16] presents the dedicated short-range communication (DSRC) standards typically adopt both FM0 and Manchester codes encoding technique for succeeding the dc-balance and enhancing the signal irresponsibleness. This paper is not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works. [17, 18] proposed the SOLS technique used to removes the limitation of the utilization of hardware by two core techniques: area compact retiming and balance logic-operation sharing. The technique of Area-compact retiming reduces the hardware problem like number of transistors and by the other technique of balance logic operation sharing the help for identifies the logic components which can be efficiently combines the FM0 and Manchester encoding technique.

III. CODING PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

FM0 code and Manchester code describe the Coding principles as follows-

In this discussion, the input data and the clock data signal are reduced as C, and X, respectively. The coding principles of FM0 and Manchester codes are discussed by the above parameters are as follows. A. FM0 Encoding in shown in Figure. 3.1, for each X, the FM0 code which consists of two parts: (a) one for former-half cycle of CLK A, and (b) the other one for later-half cycle of CLK, B. FM0 coding principle is listed as the following three rules-

1) If X is logic-0, then there is a transition between A and B.

2) If X is logic-1, no transition is acceptable between A and B.

3) Among each FM0 code the transition is allocated and no matter what the X is.

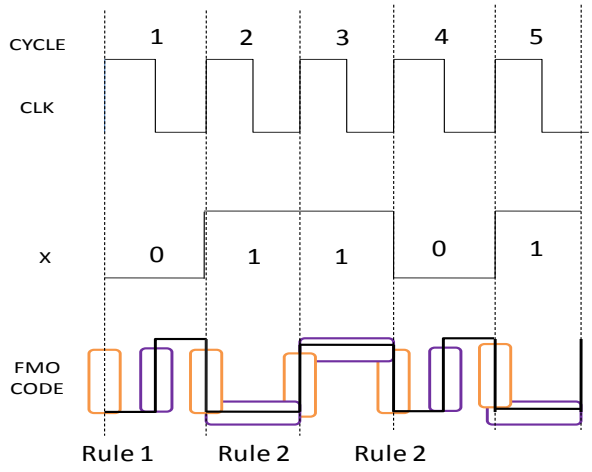

Fig.. 3.1(a) Example of FMO Encoding

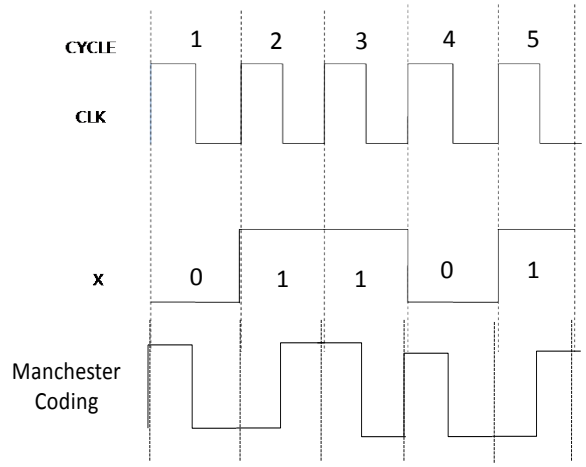

Fig. 3.1(a).Example of Manchester Coding

The example of FM0 coding is shown in Figure 3.1. In first cycle, X is logic-0; thus, a transition occurs in FM0 code, according to rule 1. For effortlessness, these types of transitions are initially setup from logic-0 to -1. According to the rule 3, transitions are allocated with each FM0 code, and thus the logic-1 is change to logic-0 at the starting of the cycle 2. According to the rule 2, the logic-level is holds without any transition in complete cycle of 2 for the X of logic-1. Thus, the each cycle of FM0 code can be derived with the three rules that are mentioned earlier. The encoding of the Manchester code is realized with the XOR operation between input signal and clock. The encoding of the Manchester always encodes and used to produces a transition between the centers of each cycle.

The hardware architecture of the FM0 and Manchester encoder is shown in Figure 3.2. The upper part is shown by the FM0code and then the bottom part is shown as the Manchester code. In code of FM0 are DFF1 and DFF2 which are used to store the state code of the FM0 code. It also uses mux_1 and NOT gate is used in the code of FM0. For the FM0 code is Mode=0. For Mode=1has the output in Manchester code and this type of code developed only for the data to be XOR with the clock signal.

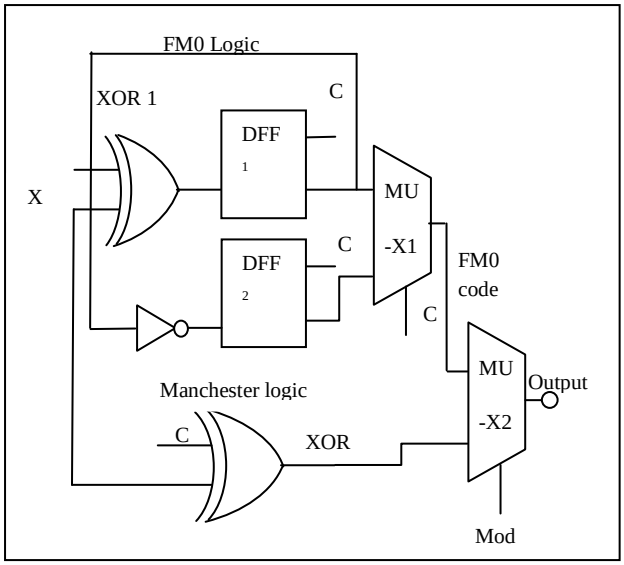

Fig. 3.2 Hardware Architecture of FM0/Manchester Encoder

The utilization of hardware is defined at the rate of the HUR and it is represented by the following equation.

$$HUR = (AC / TC) * 100 \% \quad (1)$$

Where, AC- Active Components and TC- Total components. The active component defines the components that work in both FM0 and Manchester code generation.

IV. FMO AND MANCHESTER ENCODER USING SOLS TECHNIQUE

By the SOLS technique it removes the limitation of the utilization of hardware by two core techniques: area compact retiming and balance logic-operation sharing. The technique of Area-compact retiming which reduces the hardware problem like number of transistors and by the other technique of balance logic operation sharing the help for identify the logic components which can be efficiently combines the FM0 and Manchester encoding technique.

- *Area compact retiming*

For FM0 each state code is stored in DFFA1and DFF2. The transition of the state code is depends on the previous

state of 1(t-1) instead of the both 2(t-1) and 1(t-1) as shown

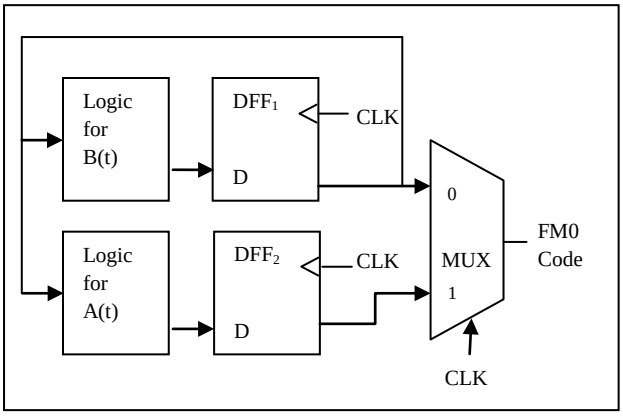

Fig. 4.1 Area Compact Retiming

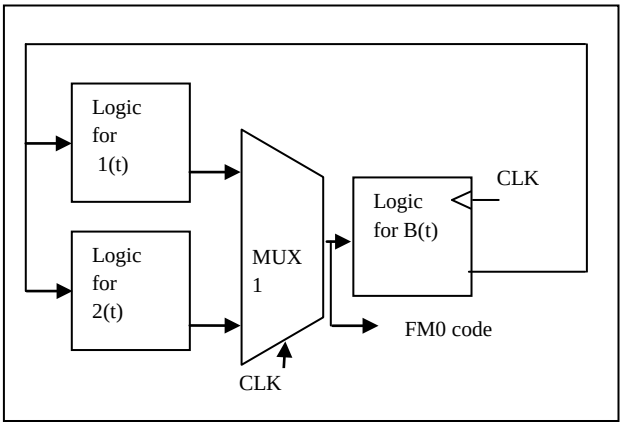

Fig. 4.2 FM0 Encoding Without Area Compact Retiming

The earlier state is shown as the 2(t-1) and then the state 1(t-1). Then the current state is shown as the 2(t) and then the state 1(t).

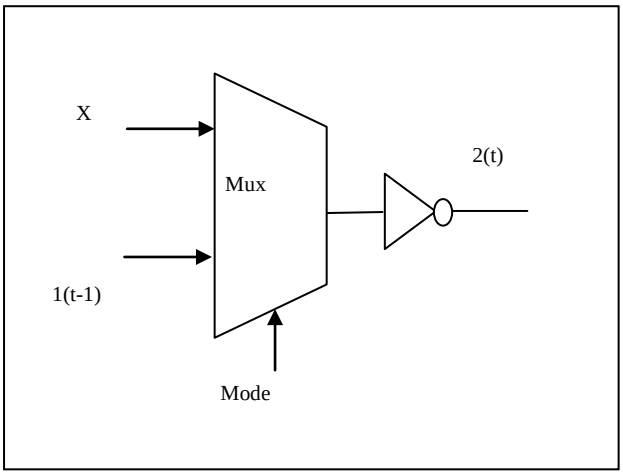

Fig. 4.3 Hardware Architecture of FM0/Manchester Encoder Multiplexer

The encoding of the FM0 requires the single which are having the 1-bit flip-flop for storing the previous value as 1(t−1). If we remove DFF2 directly then non synchronization between 2(t) and 1(t) causes the logic fault of FM0 code. For avoiding the logic-fault, relocate DFF1after the MUX−1 at the right. In that design DFF1 is understood as the positive-edge trigger flip flop. At the each logic cycle, FM0 code, comprise 2 and 1, which is derived from the logic 2(t) and of the logic of 1(t), respectively. The FM0 code is switched between 2(t) and 1(t) during the MUX−1 which is controlled by the CLK signal. It directly updated Q of DFF1 from the logic 1(t) with 1-cycle latency. When the CLK is at the logic-0, the 1(t) is passed through MUX−1 to the D of DFF1. Then, positive-edge of the upcoming CLK updates it to the Q of DFF1. The for the Q of DFF1 timing diagram is reliable whether for the DFF1 is relocated or not. The state 1(t) is passes through the MUX−1 to the D of DFF1. The positive-edge of the upcoming CLK is updating the Q of DFF1. The Q of DFF1 timing diagram is reliable whether the DFF1 is relocated or not.

- *Balance logic operation sharing*

The encoding of the Manchester is derived by using the XOR operation. The equation of the XOR gate is given below-

X XOR CLK = X + CLK

The concept of sharing the balance logic-operation is used to integrate the X into 1(t) and X into 2(t). Both FM0 and Manchester logics have some common points of the multiplexer such as logic with the selection of clock, the diagram for the balance logic operation sharing given the following as shown below-

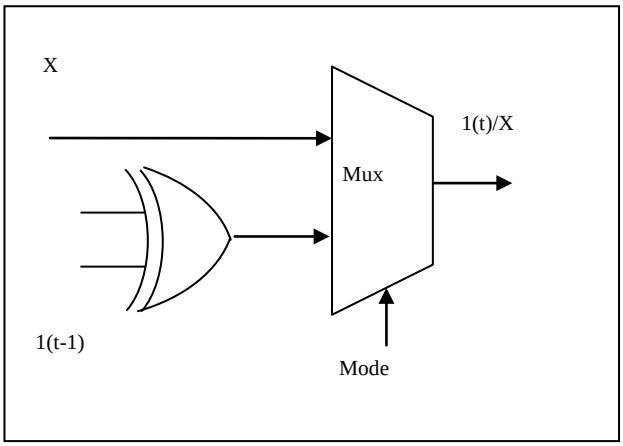

Fig. 4.4 Balance Logic Operation Sharing

Here, the Output of the FM0/Manchester defined by the MUX Mode. If output of FM0 is Mode =0 and when Mode=1 then the output is Manchester.

The 2(t)/X' is derived from the inverter 1(t − 1), and X. The logic 2(t)/X' share the same inverter, and before the multiplexer the inverter is placed to switch the operands of

1(t − 1) and X. The Mode of the MUX used to indicates either of the FM0 or of the Manchester encoding. The same concept can be also applied to the logic for 1(t)/X.

However, the drawbacks of the architecture exhibit the HUR of this architecture which is limited because XOR is dedicates the FM0 encoding, and this is not shared with encoding of Manchester. The X can also be interprets as the X 0, and therefore the operation of XOR are shared with the FM0 and Manchester encodings. Here the multiplexer of the design should not responsible to switch the operand of 1(t−1) and logic-0. The architecture shares the XOR operation for both 1(t) and X, and thereby it increases the HUR.

V. SIMULATION AND SYNTHESIS RESULTS

The present design is simulated and synthesized using Xilinx ISE Tool. The simulation based Block Diagram and the RTL Schematic diagrams of FM0-Manchester Encoder design are shown in Figure 5.1 and Figure 5.2 respectively.

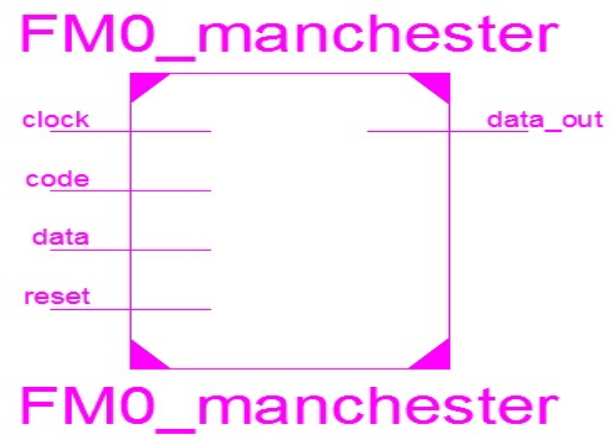

Fig. 5.1 Block Diagram of FM0/Manchester Encoder

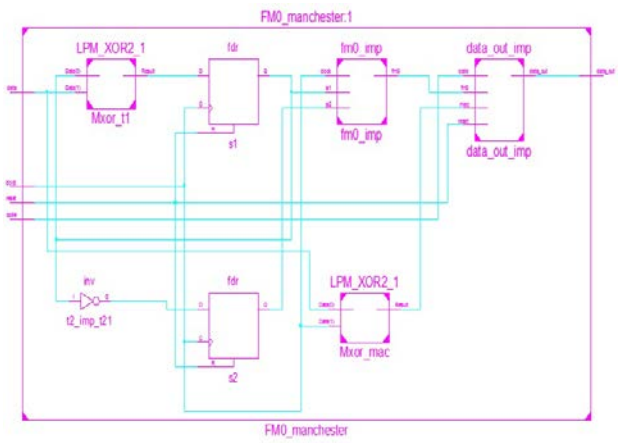

Fig. 5.2 FM0/Manchester Encoder

The waveform simulation diagram of the encoder design is shown in Figure 5.3.

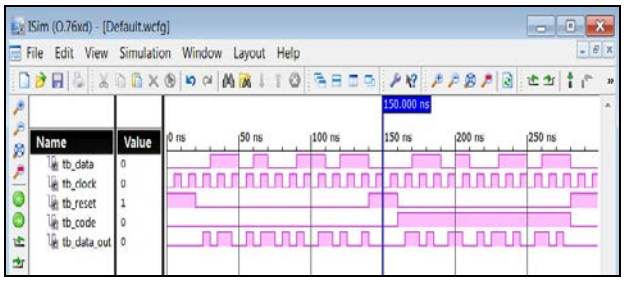

Fig. 5.3 Hardware Architecture of FM0/Manchester Encoder

The encoder design is implemented on Xilinx Spartan3 FPGA. The hardware includes FPGA Kit, LCD 16x2 Display and Push-button board. Fig- 5.3 shows the arrangement of the implementation kit setup and Figure 5.4shows reset mode operation display on LCD.

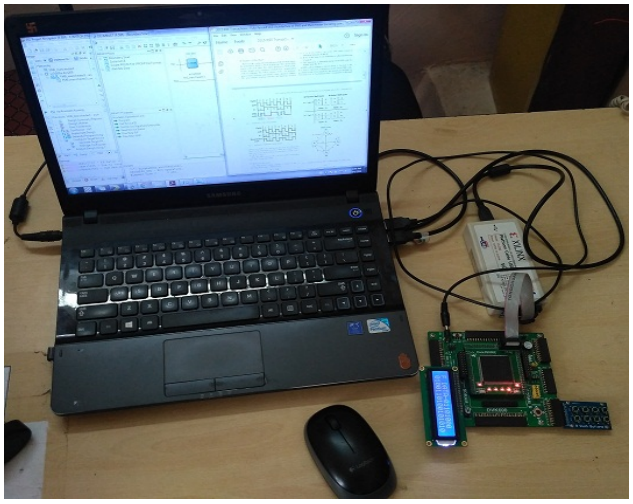

Fig. 5.4 Hardware Setup of FM0/Manchester Encoder

The hardware based design simulation is performed on various input values. An example with input value “01101000” is shown for both FM0 and Manchester operational modes in Figure 5.5 and Figure 5.6 respectively.

Fig. 5.5 Hardware Architecture of FM0/Manchester Encoder

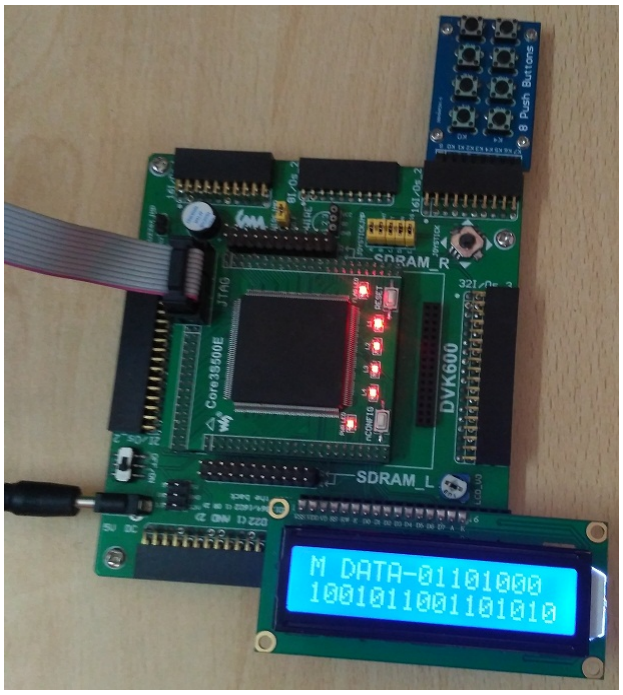

Fig. 5.6 Hardware Architecture of FM0/Manchester Encoder

The FPGA based hardware utilization summary of the implemented Encoder design is presented in Table I and Table II respectively. The hardware utilization is presented for software simulation based design and hardware implementation design.

Table 1. Hardware utilization summary of fm0-manchester encoder (software design simulation)

Spartan-3E XC3S500E-4PQ208	Total	FM0-Manchester Encoder	
		Used	%
Slices	4656	2	0
Flipflops	9312	2	0
LUTs 4-Inputs	9312	4	0
Bonded IOBs	158	5	3

Table 2. Hardware Utilization Summary of FM0-Manchester Encoder (Hardware Design Simulation)

Spartan-3E XC3S500E-4PQ208	Total	FM0-Manchester Decoder	
		Used	%
Slices	4656	299	6
Flipflops	9312	244	2
LUTs 4-Inputs	9312	441	4
Bonded IOBs	158	23	14

A comparative analysis of the hardware utilization of the design in the present work with some of the existing works is presented in Table III.

Table 3. Comparative Analysis of present design based on Hardware Utilization

Reference	Present Work	[19]	[15]	[19]
Device	Xilinx FPGA Spartan3	Xilinx FPGA Spartan2	Xilinx FPGA	Xilinx FPGA Spartan2
Slices	2	5	2	1
Flipflops	1	4	2	2
LUTs 4-Inputs	3	10	3	2
Bonded IOBs	5	4	5	3

VI. CONCLUSION

By the use of the SOLS technique it removes the limitation of the utilization of hardware by two core techniques: area compact retiming and balance logic-operation sharing. The technique of Area-compact retiming which is used to reduce the hardware problem like number of transistors and by the other technique of balance logic operation sharing it help for identifying the logic components which can be efficiently combined in both FM0 and Manchester encoder. The results are used to show the utilization of the hardware. This work develops the Very Large Scale Integration (VLSI) architecture for both the FM0 and Manchester Encoding for area improved design.

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