Input Vector Monitoring Concurrent BIST Architecture Design for a Multiplier

Kritika Sharma[1], Aman Saraf[2]

[1]*M Tech Research Scholar,* [2]*Research Guide, Department of Electronics and Communication Engineering,*

Radharaman Institute of technology, RGPV, Bhopal, India

Abstract - Testing of VLSI chip is done at many places by different types of people. Testing should verify correctness of design and the test procedure. When a new chip is designed and fabricated for the first time. The testing may even take place in the design laboratory rather than in a factory and it frequently needs the involvement of the design engineer. Some god chips turn out to be the result of successful verification. A successful verification also signals the beginning of production i.e large scale manufacturing. These are usually used by designers of the systems that will use the design. In factory, mostly the fabricated chips are tested. Finally these manufactures chips are again tested to ensure quality before it is received by the customer. This is also known as inspection testing (or acceptance testing) and is conducted either by the user or for the user by some independent testing house. While testing, a part of the circuit (having the fault) is replaced with a corresponding redundant circuit part (by re-adjusting connections), in case any fault is found. BIST is testing a circuit every time before they startup. This paper presents central concepts of testing of VLSI circuits by BIST.

Keywords: IJSPR Off-Line Testing, On-Line Testing, Self-Testing Input Vector Monitoring, Pre-Computed Test Set, Error Detection.

I. INTRODUCTION

Built-in self test (BIST) is a technique that constitutes a class of schemes that give the capability of performing high fault coverage at-speed testing, whereas simultaneously they rest the dependence on expensive external testing equipment. Consequently, they represent an attractive solution to the problem of testing VLSI devices. BIST techniques are typically classified into online and offline. There were two modes normal and test, the architectures operate in either normal mode (during which the BIST circuitry is idle) or test mode is Offline architecture. The inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV) for the entire duration. Hence, to perform the test, the standard operation of the CUT is slowed down and, consequently, degraded performance of the system in which the circuit is included obtain. To figure out that a technique is proposed to avoid such conditions is Key vector monitoring simultaneous with BIST. These architectures test the CUT at the same time with its normal operation by exploiting input vectors appearing to the inputs of the CUT; here is the condition, if the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response The CUT has *a* inputs and *b* outputs and is tested comprehensively; hence, the test set size is $N = 2a$. The technique can operate in either normal or test mode, depending on the value of the signal labelled *T/N*. Normal input vector is the driver that that drives the inputs of the circuit which is to be tested this is to be done at the time of normal mode. A is a input which is driven to the concurrent BIST unit (CBU), this input A is compared with active test set. When there is any similarity between A and any one of the vectors in active test set, we say that hit has occurred. Shown by fig.1 this is the condition in which A will be removed from the active test set after that the signal response verifier enable is given to enable the *m*-stage of the RV to capture the CUT response. The condition occurs when all the input vectors have performed hit, then the contents of RV are examined.

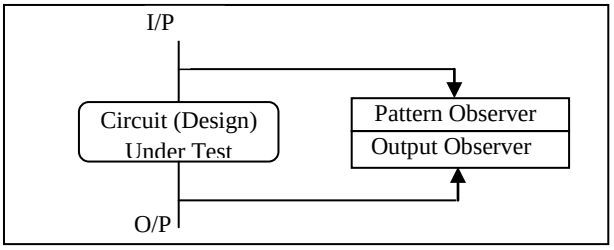

Fig.1. Online testing block

CBUs output denoted by TG [*n*:1] is the driver of the inputs of the CUT during the test mode.

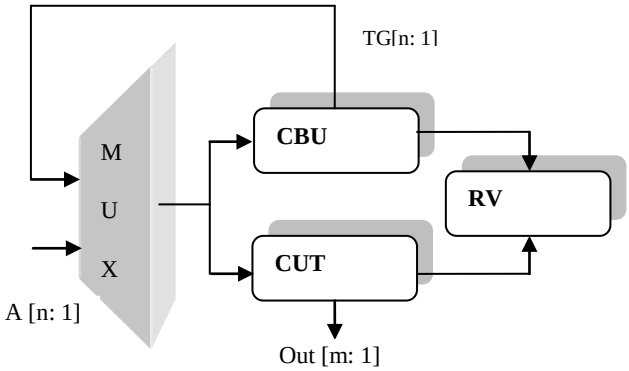

Fig.2. Input vector monitoring concurrent BIST architecture.

The concurrent test latency (CTL) of input vector monitoring is the mean time (counted either in numbers of clock cycles or units of time) required to complete test performance while the circuit performance in normal mode. Test Pattern Generator (TPG) is a method utilize

by the BIST to generate the required test patterns which are applied to the number of inputs of the Circuit under Test (CUT). In brief, an input vector monitoring concurrent BIST is proposed, which will compares favourably to the previously proposed schemes in order to the hardware overhead/CTL trade off. The block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig.2

II. LETERATURE REVIEW

In reference [1, 4, 5, 7, 11, 18] a novel input vector monitoring concurrent BIST architecture is presented which is based on the use of a SRAM-cell like structure for storing the information, whether an input vector has appeared or not during normal operation. In reference [2, 13, 14, 17] the work is performed for avoiding performance degradation of a system by proposing a novel input vector monitoring concurrent BIST technique for combinational circuits termed R-CBIST. Reference [3] proposed a RAO-DDR technique for faults detection at the duration of system operation. This technique not only locate the fault but also capable to correct the faults. Reference [6] proposed model can be extended by incorporating shortages, discount and inflation rates. In addition demand can be considered as a function of price, quality as well as time varying. Reference [8] presents a Modified BIST based on the utilization of SRAM cell like structure which stores the information about whether an input vector appears or not in normal operation. BIST schemes provide an attractive solution for the problem which arrives during testing VLSI devices.. Reference [9,15] proposed method is three weight pattern generation pseudorandom built-in-self-tests (BIST) method to achieve complete fault coverage in BIST applications by reducing number of vectors. Weighted sets are 0, 0.5, and 1 have been used generate test pattern generation and achieve low testing time less power consumption. Reference [10] proposed technique, a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of CAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. Reference [12] a novel input vector monitoring concurrent BIST architecture has been presented, based on the use of a SRAM-cell like structure for storing the information of whether an input vector has appeared or not during normal operation. Reference [16] proposed a method for fault monitoring using input vector concurrent BIST based on SRAM-cell used to store information at normal operation. The proposed method is a weighted Pseudo-random built-in-self-test (BIST) scheme utilized in order to drive down the number of vectors to achieve complete fault coverage in BIST applications. Reference [19] proposed a novel input vector monitoring concurrent BIST architecture based on the use of a SRAM-cell like structure for storing the information. This paper presents BISD and BISR scheme to perform the fail pattern identification and repairing of the fail pattern in the test cubes. Reference [20] presents a modification i.e. Multiple Hardware Sig nature Analysis Technique (MHSAT), Order Independent Signature Analysis Technique (OISAT), RAM-based Concurrent BIST (R-CBIST), Window-Monitoring Concurrent BIST (w-MCBIST), and Square Windows Monitoring Concurrent BIST (SWIM). The proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL.

III. CONCURRENT BITS ARCHITECTURE

Built-in self-test (BIST) techniques include a charismatic solution to the problem of testing VLSI devices as they are composed of a class of schemes that provide the potentiality of performing at speed testing with high fault coverage, and also at the same time they reduce the reliance on expensive external testing equipment. BIST schemes are either offline or online. Offline architectures operations are divided into normal mode (during which the BIST circuitry is idle) or test mode. In test mode, the inputs that are generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV). Hence, the normal operation of the CUT is conked to perform the test and, therefore there is degradation of performance of the system in which the circuit is included. Input vector monitoring concurrent BIST techniques have been proposed to avoid this performance degradation. These architectures test the CUT simultaneously with its normal operation by exploiting input vectors appearing to the inputs of the circuit under test. If the incoming vector belongs to a set called active test set, the RV is enabled to capture the CUT response. Refer to the block diagram of an input vector monitoring concurrent BIST architecture is shown in Fig. 3.

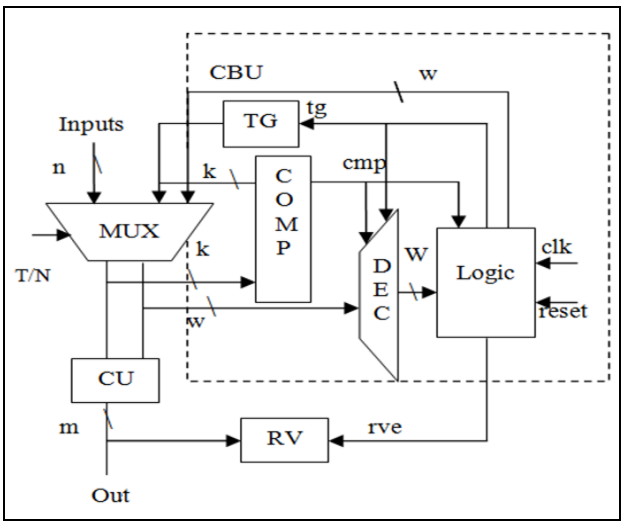

Fig.3 Generalized Architecture of IVM BIST

IV. PROPOSED METHODOLOGY

Figure 4 shows the proposed architecture of IVM with BIST the block contained in this architecture were two MUX that produces the output depends on the mode if the mode is normal it selects the normal vectors, if the architecture performs in test mode MUX selects TA, TB as its inputs. This architecture depends on two mode i.e., normal mode and test mode, a 4 bit multiplier block that generates the 4 bit product output, a test pattern generator that comes in work when test mode is activate, another block is IVM BIST control unit role of this unit is to produce a decoded value to be checked and final block is response verifier that compares the output of 4 bit multiplier and the IVM BIST control unit output. If the values don't match then it will show that there are errors that have to be corrected. RV is enabled when the output of the decoder and the 4-bit multiplier does not match. The architecture performance depends on two modes named as normal or test mode. The functionality of the system and named as *T/N*.

If the value of T/N is 0 systems operates in normal mode and the inputs of multiplier driven by normal input vector i.e., A and B are the inputs. The outputs of multipliers are provided to the 4-bit multiplier and it generates an output by multiplying the inputs. At the same time the output of the MUX is given to the IVM BIST control unit that also decodes the actual output. And check is performed by response verifier. This unit only activated when the output of the IVM BIST control unit and the output of the 4 bit multiplier doesn't match. If there is no error, both the outputs are same then product output is obtained.

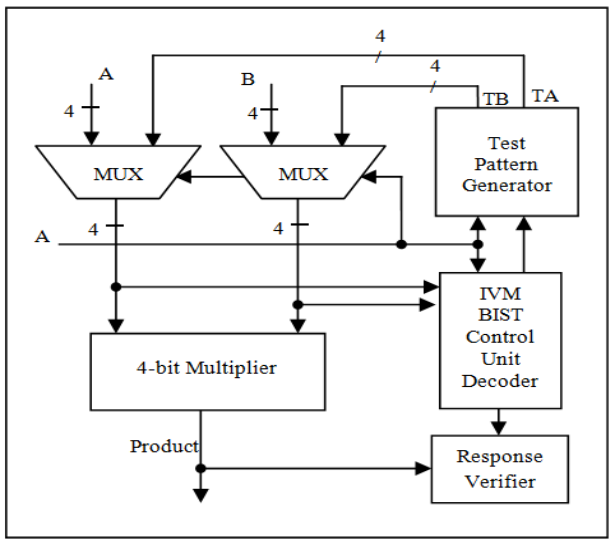

Fig.4. Proposed Architecture

If the value of T/N is 1 system operates in test mode and the input selected by the multiplier driven by the test pattern generator i.e., TA and TB. And this test pattern generator is controlled by IVM BIST control unit. The procedure is same MUX selects TA, TB and given to the 4 bit multiplier that generates an output and this output is then compares with the IVM BIST control unit value at response verifiers and follow the same explained above.

The generation of this concurrent BIST test pattern includes the following steps:

- The number of bits generated per pattern is restricted to some limit. Generation to some extent particular test set with minimum no of bits as possible.
- Target efficiency is achieved by selecting the patterns from this test.
- Comparison is done in appropriate manner by selecting output values.
- Continuously monitor the input output value Generate by the BIST control unit and the 4-bit multiplier.

V. SIMULATION AND SYNTHESIS RESULTS

In this session the simulation and results were shown figure 5 shows RTL block of IVM-BIST multiplier with BIST, and .Figure 6, 7, 8 and 9 represents the synthesis Simulation Waveform IVM multiplier with BIST in normal mode and in test mode with or without hardware fault respectively. And Table I represent hardware utilization summery of 4-Bit multiplier design and Table II represents IVM-BIST based multiplier design.

Table i. Hardware utilization summary of 4-bit multiplier design.

Spartan-3E XC3S500E-4PQ208	**Total**	**4-Bit Multiplier**	
		Used	***%***
Slices	4656	18	0
Flipflops	9312	0	0
LUTs 4-Inputs	9312	31	0
Bonded IOBs	158	20	10

Table ii. Hardware utilization summary of ivm-bist based multiplier design

Spartan-3E XC3S500E-4PQ208	**Total**	**IVM-BIST Architecture**	
		Used	***%***
Slices	4656	56	1
Flipflops	9312	9	0
LUTs 4-Inputs	9312	108	1
Bonded IOBs	158	20	12

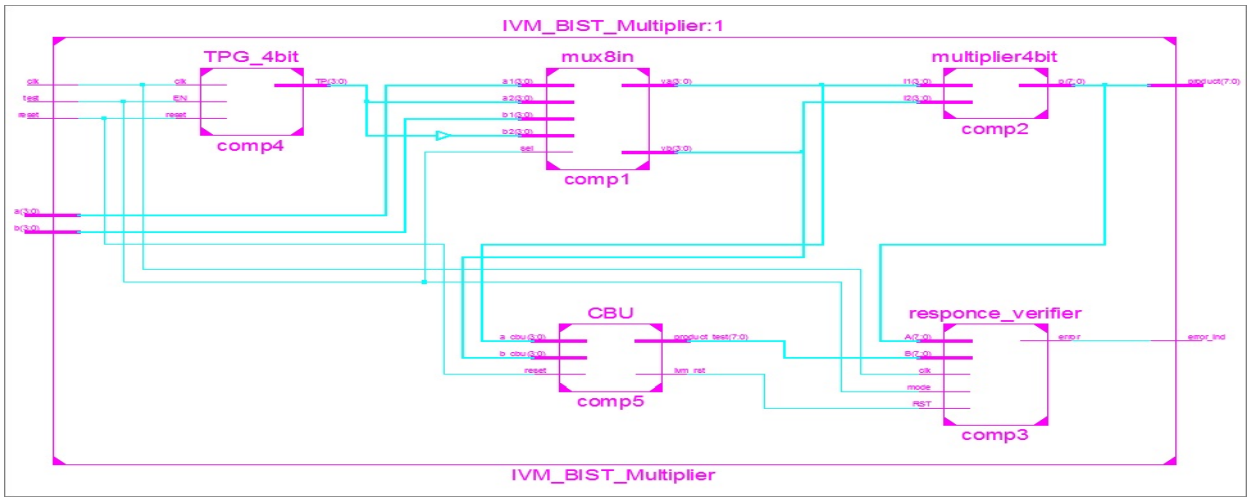

Fig.5. RTL of IVM main block with BIST

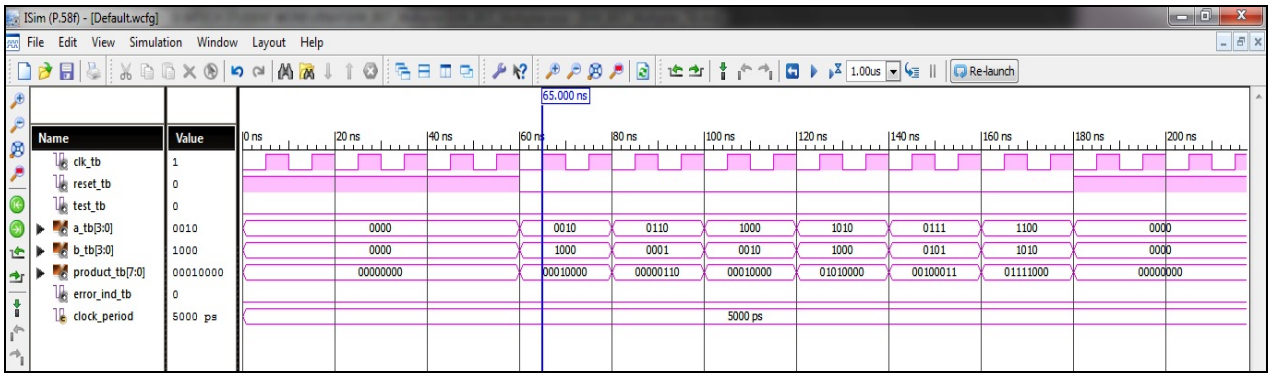

Fig.6. Simulation waveform of IVM-BIST-Multiplier normal mode

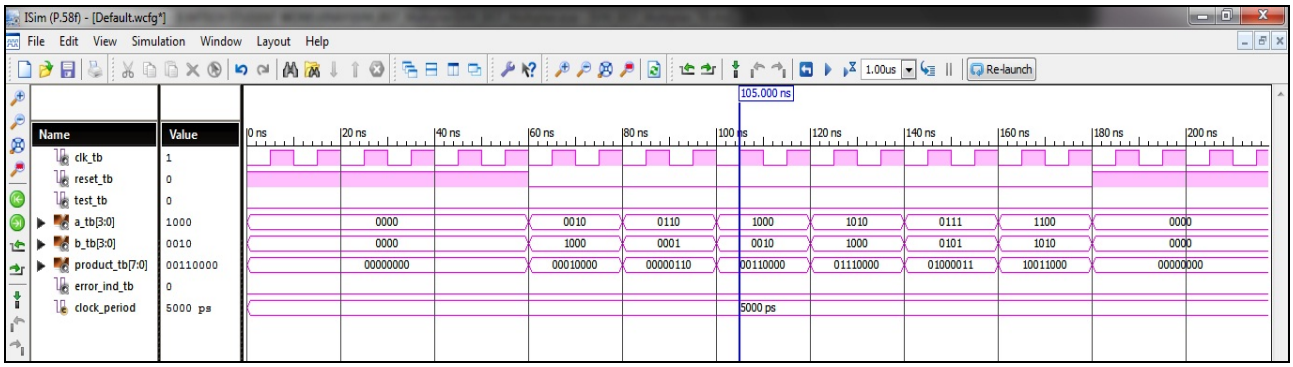

Fig.7. simulation waveform of IVM-BIST-Multiplier normal mode (with hardware fault)

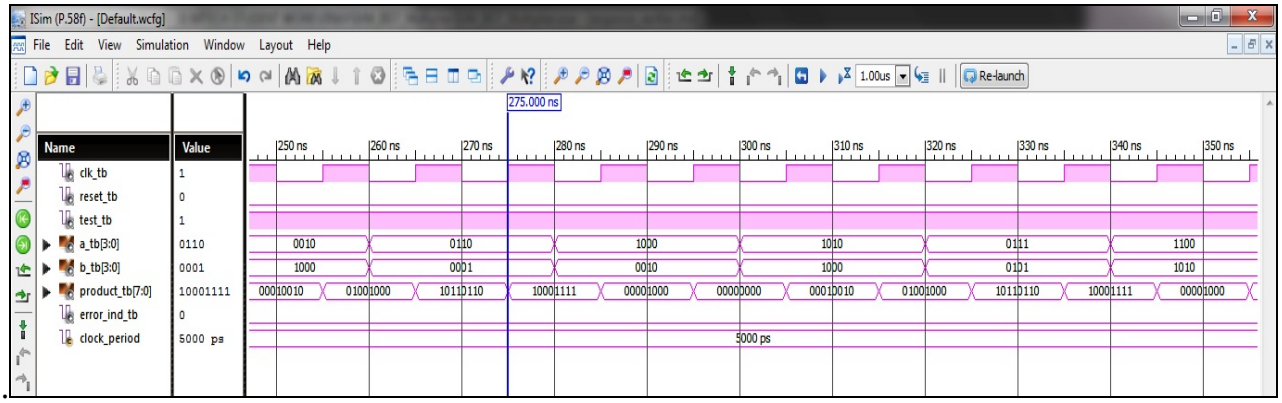

Fig.8. simulation waveform of IVM-BIST-Multiplier Test mode.

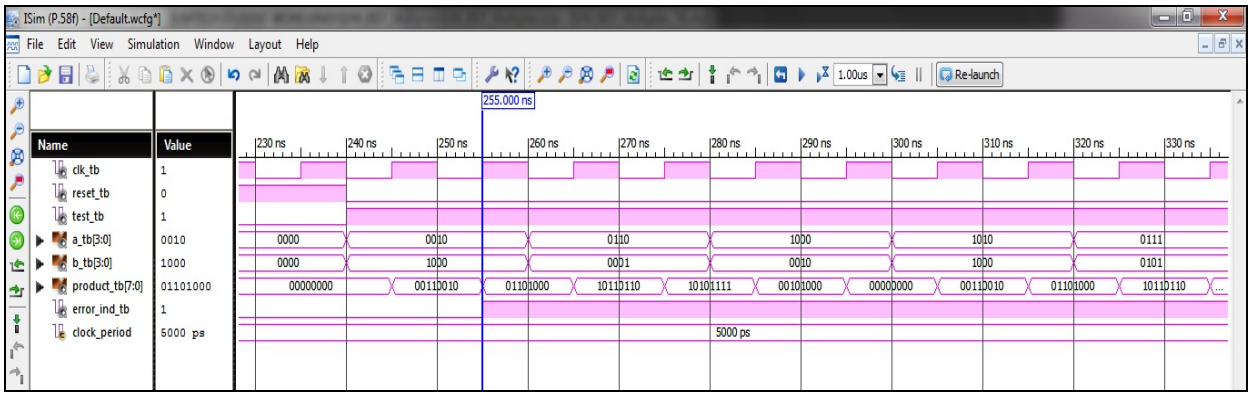

Fig 9. Simulation waveform of IVM-BIST-Multiplier Test mode (with hardware fault)

VI. CONCLUSION

For the problem of testing VLSI devices, BIST schemes provide an attractive solution. Input vector perform testing during the circuit normal operation, while monitoring concurrent BIST schemes, without imposing a need to set the circuit offline to perform the test. They can circumvent problems appearing in offline BIST techniques. For the class of testing schemes, the evaluation criteria are the hardware overhead and the CTL, when the circuit operates in its normal mode. CTL is the time required for the test to complete. This brief includes a input vector monitoring concurrent BIST architecture. The basis is the usage of a SRAM-cell like structure to store the information data, whether an input vector has appeared or not during normal operation. With respect to the hardware overhead and CTL, the proposed scheme is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques. We have mainly introduced new methods to implement and use of saboteurs and mutants into VHDL models in this project. It has been observed that the new models of saboteurs prevent some of the problems that they previously had like automatic insertion. Moreover, the new models have been implemented in a way that, by reducing the number of signals that is required to manage bidirectional saboteurs, they diminish the hardware overhead. Another enhancement is that they allow injecting of more fault models as compared to prior models. The key advantage of the new proposal is to implement mutants. The application of these saboteurs and mutants is to example circuits at gate level and register level.

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