# Development of Delay Efficient Aging Aware Multiplier using Modified AHL

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***Abstract - The designing of a multiplier with better device utilization will facilitates the various digital device to overcome from the high density of logic on the integrated devices. The integrated device suffers with NBTI and PBTI due to CMOS semiconductor properties and it affects the working of different logic operations and in the same context here we have taken multiplier for consideration and working to develop delay efficient multiplier with aging aware design using adaptive hold logic which is modified in this work to reduce effective delay to speedup circuit logic. After synthesis of proposed architecture the overall delay of the device is 12.2ns which is 50% lower than the existing architecture delay i.e. 24.965ns. In the synthesis outcomes it is clear that the modified approach for delay efficient multiplier design is faster than the previous architectures.***

***Keywords - AHL, Multiplier, Aging Effect, NBTI, PBTI, Delay Efficient.***

## I. INTRODUCTION

It is surely understood that silicon based innovation for radiation solidified space gadgets is a few innovation eras behind its business partners; this is outlined in figure: 1.1. So while in a matter of second's solidified gadgets in the 90 - 65 nm hub are in the innovative work stage, business industry is tending to the formative issues identifying with 22 nm gadgets. A positive outcome of this postponement is that the dependability lifetime, a present issue in the business, has not yet affected the universe of space based gadgets. As silicon based innovation advances, expanded gadget execution is being accomplished by both scaling of transistor highlight sizes furthermore by the presentation of new materials whose impact on gadget unwavering quality might be generally obscure. In the previous case the scaling of entryway oxide thicknesses underneath 2nm without the relating lessening in supply voltage brought about expanded oxide electric fields and upgraded spillage streams. Intensified with the fast increment in new materials and inalienable danger of dependability misfortune, scaling brings about expanded influence scattering coming about because of the thickness of dynamic gadgets in a given chip zone. Control dissemination is notable to bring about expanded operational temperatures prompting more quick deviation of gadget qualities (edge voltage move, transporter portability) and interconnect disappointment because of instruments, for example, electromigration. On account of temperature improved gadget trademark variety, one of the prime instruments in metal-oxide-semiconductor field impact transistor (MOSFET) p-channel gadgets is the negative predisposition temperature flimsiness (NBTI). Different creators have proposed that this corruption component might be prevailing in cutting edge, emphatically sub-Micronics innovation. What's more, an equal impact in n-channel MOSFET gadgets has been watched and named positive predisposition temperature unsteadiness (PBTI) which comes about because of hoisted temperature and positive inclination concerning substrate. It has been more than once appeared, in any case, that trademark moves because of PBTI are significantly not exactly the movements saw in NBTI. Accordingly, it is broadly acknowledged that the hidden physical instrument behind the wonder of NBTI results in the era and catching of positive charge. The root of this positive charge stays being referred to and has caught the enthusiasm of analysts everywhere throughout the world.

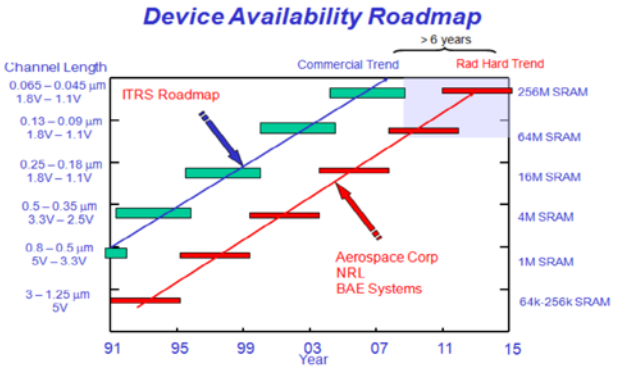


Figure: 1.1 Device Availability Roadmap comparing the radiation hard trend to the commercial trend

From point of view of circuit lifetime, PBTI and NBTI result in unbalanced corruption of the n-channel and p-divert MOSFETs since in size NBTI>PBTI as it were. The asymmetry incited creates timing issues that can eventually prompt rationale upsets. This is clear by investigation of the full square law demonstrate for source deplete current in a MOSFET

$$Ids = (W/L)\ M,eff\ Cox\ [\{Vgs - (V_{tho} + AV^{th})\}Vds - 1/2Vds2] \quad (1.1)$$

Where W is the channel width, L the channel length and Cox the gate dielectric stack capacitance. eff is the effective mobility of the inversion channel carriers (holes(p) or electrons(e)). In the p-channel devices, +ve charge is trapped somewhere in the gate dielectric effectively making the threshold voltage ($V^{th}$) more negative. From Equation 1.1, an increase in | ($V^{th}$ + $AV^{th}$ ) I will result in a decrease in Ids for a given $V_{gs}$.. Coupled with the fact that the delay time for signal arrival in a CMOS circuit is inversely proportional to the source-drain current (Ids) of the transistor, the effect of NBTI will be to increase the delay time. As for the n-channel devices, the $V^{th}$ remains essentially constant and thus an increased spread in signal arrival times is created. This degradation of the timing paths can potentially lead to logic upsets and ultimately circuit failure.

In the light of the past discourse one may have expected that proof of a dependability lifetime issue because of such instruments as NBTI in cutting edge CMOS innovation would have as of now had a significant negative effect on the business. Be that as it may, it has not and the clarification for this rotates around two attributes of the business. The first is that business items are progressively supplanted following a couple of years of utilization (i.e. before destroy) and in this way strict lifetime prerequisites, for example, the old day in and day out for a long time are redundant. Furthermore, the most pessimistic scenario, consistent operation situation is occasionally seen in present day hardware and one must consider, for eg.,

The obligation cycle which can drastically decrease the gadget "on time"? Given that the qualities of watched caught charge unwinding wonders happening in NBTI , one can reason that nature accidentally works in lessening the general size of corruption. For instance, tests on 65 nm innovation delivered by one of the world's chief producers of microelectronics (TSMC) brought about a DC lifetime of 0.2 years and an AC lifetime of 10 years [4]! Be that as it may, the unwavering quality of cutting edge CMOS innovation is a noteworthy reason for worry in the space business where certain satellite applications require operational lifetimes ~ 10 - 15 years. Among the different systems adding to dependability misfortune in satellite hardware, for example, electronic unwavering quality (NBTI and PBTI), and the impacts of light by means of aggregate ionizing measurements and additionally single occasion bombshell, NBTI is the minimum comprehended and keeps on producing the most concern. It is critical that a more profound comprehension of the root and nature of NBTI be accomplished. The space business will plainly develop to more propelled innovations and gadget unwavering quality will turn into the essential variable constraining the lifetime of a satellite.

Although the starting point of NBTI is not comprehended, it seems clear that it is personally identified with the material science of the entryway cover/semiconductor interface and unquestionably, progressively, to the way of the intricate oxide utilized as the door encasing. In more propelled creation forms higher dielectric consistent (K) entryway encasings are being acquainted all together with empower thicker dielectric movies to be utilized. Take note of that to first request the spillage current changes reverse exponentially with the dielectric thickness (tox) [5] and that the door capacitance C <x K/W. Thus, similar door capacitance can be accomplished utilizing higher K movies which are thicker. In any case, it has been watched tentatively the utilization of high-K movies upgraded NBTI and therefore debased lifetime steady quality results. In the easiest case, this is accepted to be the outcome from expanded charge trap thickness in complex oxides. In any case, the genuine picture turns out to be significantly more confused when we consider the procedure steps required in the formation of the door stack. Initial one begins with a thin (~ ~1 nm) SiO2 layer on the Si substrate, this is trailed by an option dielectric, for example, HfSiO which might be then nitride to shape HfSi ON. This procedure won't bring about a straightforward HfSi ON/Si entryway stack yet more probable at any rate HfSi ON/Si ON/Si having at least two significant confounds interfaces (HfSi ON/Si ON and Si ON/Si) and two "mass" dielectrics, HfSi ON and Si ON, with their own particular charge catching imperfection destinations. The subsequent many-sided quality of the entryway stack in no time anticipates distinguishing proof of the correct nature and area of the traps as well as their spatial dispersion. Then again, contrasting the charging and unwinding energy of a gadget with a straightforward SiO2 entryway dielectric to a gadget with a "high K" door dielectric can offer important knowledge into the physical system of NBTI.

Perhaps a standout amongst the most difficult angles in the investigation of NBTI is the way that estimation systems differ significantly starting with one research bunch then onto the next making cross referencing of research results extremely troublesome. Despite the fact that it seems far-fetched right now, at last a nonexclusive convention for the estimation of push initiated limit voltage debasement should be set up. As we will examine in detail, in our own particular approach we focus on the decrease of error coming about because of caught charge unwinding by managing the stretch all through the test. This is accomplished by measuring the adjustment in source-deplete current with time Ids(t) while keeping up a focusing on voltage on the door and deplete contacts. The gadget limit voltage move $AV^{th}$ can then be separated from the fragmentary current change Ids/Idso Bearing as a main priority certain approximations which we will approve in a later part, the consequence of this persistent push

estimation will be appeared to be a decent representation of the full impact of caught charge on the edge voltage in the DC stretch mode. This ends up being a urgent bit of data when attempting to build up a superior comprehension of the material science, yet may not be the best technique on which to base a dependability lifetime indicator show. Building a solid lifetime indicator equation will require cautious examination of the circuit operation conditions and in addition innovation particulars.

## II. SYSTEM MODEL

The interest for frameworks with elite has expanded hugely, driving the move of CMOS innovation towards all the more profoundly scaled nanometer include sizes. While more noteworthy on-chip gadget incorporation inside similar chip zone offers higher processing abilities, highlight measure scaling likewise brings about a corresponding lessening in the probability that the created chip, at the postsilicon arrange, meets the details created in the outline stream before manufacture, at the presilicon organize.

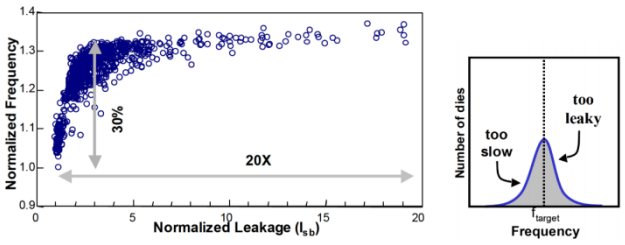


Figure 2.1: (a) Variability in frequency and leakage in about 1000 fabricated dies, and (b) deviation in the frequency of dies from the targeted frequency specification, courtesy Intel

This deviation is essentially owing to the impacts of varieties (process, natural, and maturing), which have become bigger with contracting highlight sizes. This represents a significant test to accomplish a concurrent conclusion on the triple measurements of execution: solid registering, high throughput, and low power.

As a delineation of the effect of process parameter varieties, Figure: 2.1(b) demonstrates the impact of process inconstancy with contracting highlight sizes on the recurrence and spillage of manufactured chips. The dissemination of recurrence along the y-hub is plotted against standardized standby spillage along the x-pivot for around 1000 passes on (microchips) manufactured with 0.18^m innovation. Because of variety in transistor parameters, chip spillage and recurrence endure with around 20x and 30% variety from the base to the greatest, individually. This pattern is further outlined through Figure: 1.2(b), which demonstrates the deviation of chip recurrence of the considerable number of bites the dust from the focused on recurrence particular. A portion of the kicks the bucket is too moderate, and others, in spite of being quicker, are excessively broken. With all the more profoundly scaled innovation hubs, such variations are becoming more prominent, as depicted in Figure: 1.2, which shows that the variability in performance in the sub-65nm regime is much higher than at the 0.18^m technology node.

Variations in ecological variables, for example, temperature can influence the planning basic properties, for example, deferral and slew. Figure: 2.1(a) demonstrates the floor plan of IBM Power4 server [4], with its warm profile in Fig. 2.2. The warm profile demonstrates that over the little chip, the temperature angle can be obviously high, and can bring about various undesirable impacts in the processor [10], for example, expanded spillage and clock skew. This thusly unfavorably influences the chip execution, because of which a significant division of the aggregate number of adequate bites the dust may neglect to accomplish the recommended execution goals.

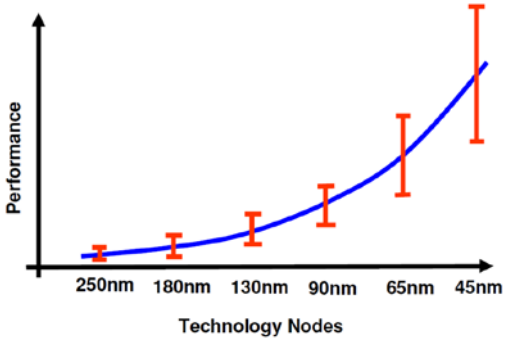


Figure 1.3: Increase in variations due to shrinking feature sizes, courtesy.

Similarly, maturing varieties in circuits because of predisposition temperature shakiness (BTI), hot transporter infusion (HCI), and time subordinate dielectric breakdown (TDDB), cause the circuit postponement to corrupt after some time. For instance, Fig. 2.2 demonstrates the fleeting variety in deferral because of BTI of a MCNC benchmark des, with time along the x-hub and postponement in picoseconds along the y-pivot, for a time of 10 years. For a 32nm Predictive Technology Model (PTM) [11] based design, the degradation in this delay is about 24% for des, and causes functional failures early in lifetime (by violating the clock period, Tclk) without adequate delay guard bands. The effects of aging, as with those of process variations, are more significant with more deeply scaled CMOS technology nodes.

## III. PROPOSED ARCHITECTURE

In the proposed aging – aware reliable multiplier design. Presented the overall architecture and functioning. the

architecture is simulated on result has taken from the Xilinx platform.

*Proposed Architecture*

The description of proposed architecture is given below.

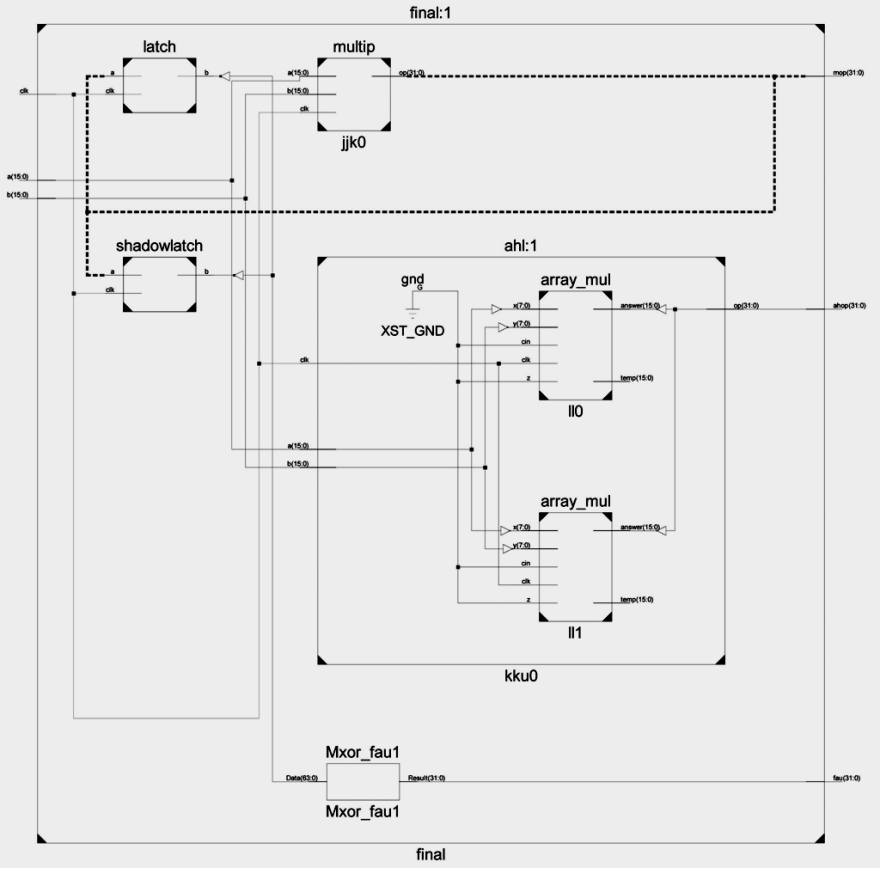


Figure: 4.1 RTL Schematic of Proposed Architecture .

Figure 4.1 shows the proposed architecture reliable aging-aware multiplier hold logic (AHL).which includes two inputs of m bit (m is a positive integer ) and two out puts , in the proposed architecture as illustrated in figure 4.1 the RTL schematic diagram .

There are 4 sections in a proposed architecture having a latch, a shadow latch, a flip flop and two arrays of multipliers 0 and 1 correspondingly. The outcome has taken from a hop(31.0).,a(15.0) and b(15.0)are the inputs .

## IV. SYNTHESIS OUTCOMES

The simulation of experiments are conducted in Xilinx IDE.

*Device Utilization*

With the help of Xilinx device utilization summery is shown in figure 5.1

```
Device utilization summary:
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Selected Device : 6slx100tfgg484-3

Slice Logic Utilization:
 Number of Slice Registers:   350  out of 126576  0%
 Number of Slice LUTs:        240  out of 63288   0%
 Number used as Logic:        240  out of 63288   0%
```

Figure : 5.1 Device Utilization Summery

*Timing summery*

In figure 5.2 timing details of device in nanosecond (ns) which shows the time taken to execute logic.

Table 5.1: Performance Comparison of Proposed Architecture with Existing Architecture with SPARTAN 3

| Parameters | Proposed Architecture | Existing Architecture |
|---|---|---|
| Delay | **12.2 ns (Approx 50% improvement)** | 24.965 ns |
| Slices | 199 (25%) | 167 (21%) |
| 4 input LUTs | 350 (22% ) | 292 (19%) |
| Bonded IOBs | 129 (104%) | 66 (53%) |

Table 2: Performance Comparison of Proposed Architecture with Existing Architecture with SPARTAN 6

| Parameters | Proposed Architecture | Existing Architecture |
|---|---|---|
| Delay | **8.499 ns (Approx 50% improvement)** | 17.962 ns |
| Slices LUTs | 240 | 190 |
| Bonded IOBs | 129 | 66 |
| Power | 81 mW | 81 mW |

```
Timing Details:
---------------
All values displayed in nanoseconds (ns)
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             2   0.447   0.845  kku0/ll1/xx17/x (kku0/ll1/xx17/x)
     LUT3:I0->O           1   0.205   0.000  kku0/ll1/FA2/(kku0/ll1/FA2)
     FD:D                     0.102          kku0/ll1/FA2/carry
    ----------------------------------------
    Total                     1.599ns (0.754ns logic, 0.845ns route)
                                      (47.1% logic, 52.9% route)
==========================================================================
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            1   1.222   0.579  a_0_IBUF (a_0_IBUF)
     INV:I->O             9   0.206   0.829  kku0/ll1/xx1/(kku0/ll1/xx1/a_inv)
     FDR:R                    0.430          kku0/ll1/xx1/x
    ----------------------------------------
    Total                     3.266ns (1.858ns logic, 1.408ns route)
                                      (56.9% logic, 43.1% route)
==========================================================================
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q              2   0.447   0.616  kku0/ll1/FA56/carry (kku0/ll1/FA56)
     OBUF:I->O                2.571          ahop_15_OBUF (ahop<15>)
    ----------------------------------------
    Total                     3.634ns (3.018ns logic, 0.616ns route)
                                      (83.0% logic, 17.0% route)
```

Figure: 5.2 Timing Summary

The performance evolutions and comparison is shown in table 5.1 and 5.2 with proposed architecture to existing architecture table 5.1 shows comparison with SPARTAN 3 and table 5.2 shows comparison with SPARTAN 6.

## V. CONCLUSION AND FUTURE SCOPE

The synthesis of aging aware delay efficient multiplier design using modified adaptive hold logic is explained and synthesized in this work. The results show the delay outcomes of the architecture with existing results and improved results. The comparative analysis of synthesis results clearly concludes that the proposed 16 bit architecture 50% faster than the previous architecture and it is better prone to NBTI and PBTI effects which slow down the calculations of digital circuits. So that for the future up gradation in logic circuits proposed multiplier design will be useful to speed up the calculations and save time. This architecture can also be upgraded using logic and architecture level optimization approaches for future evolution.

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