# Review of HIGH Performance Turbo Decoders for Wireless Sensor Networks

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***Abstract- This survey paper presents various decoders for wireless sensor networks. Also reviewed many algorithms used for decoding purposes. Turbo codes have been recognized as a milestone in the channel coding theory. These are a class of error correcting codes that come closer to Shannon's limit than any other class of error correcting codes. Due to their outstanding error-correcting capabilities, turbo codes have been highly appreciated in wireless communications as well as in encoding and decoding algorithms. It mainly focuses on turbo decoder that is appreciable for wireless sensor networks. To reduce overall energy consumption, constant Log-MAP algorithm is used for decoding.***

***Keywords— Energy-Efficient, Error Correcting Code, Log MAP Algorithm, Turbo Codes.***

## I. INTRODUCTION

Error correction codes are essential components in digital communication like data encoding and decoding and data storage systems to ensure robust operation of digital application. In 1993, Berrou et al invented turbo codes which is very popular forward error correction codes because of their near-optimal performance (near Shannon limit) [1].It have been adopted in mobile standards such as 3GPP LTE and other wireless communication systems.

Turbo codes are a class of error correcting codes that come closer to Shannon's limit than any other type of error correcting codes. Turbo codes have been recognized as a milestone in the channel coding theory. Due to their outstanding error correcting capabilities, turbo codes have been highly appreciated in wireless communications as well as in encoding and decoding algorithms. Wireless Sensor Networks (WSNs) are more energy constrained, since the sensors are operated for extended periods of time, a they are relying on batteries that are small, inexpensive and lightweight. In environmental monitoring WSNs for example, even though employing low transmission duty cycles and low average throughputs of less than 1 M bits/sec [2], the sensor energy consumption is dominated by the transmission energy Ebtx (measured in J/bit). For this reason, turbo codes have recently found application in these scenarios, since their near-capacity coding gain facilitates reliable communication when using reduced transmission energy Ebtx. Even if the transmission energy of turbo codes is less, it is offset by turbo encoders (typically negligible) and turbo decoder energy consumption. Therefore, turbo codes designed for energy constrained scenarios have to minimize the overall energy consumption. In 1974, Bahl, Cocke, Jelinek and Raviv presented the decoding algorithm based on a posteriori probabilities which was later on known as the BCJR, Maximum a Posteriori (MAP) or forward-backward algorithm. The MAP algorithm was not used in practical implementation for the last 20 years. The situation changed with the advent of turbo codes in 1993. The process of

turbo-code decoding starts with the formation of a posteriori probabilities (APPs) for each data bit, which is then followed by choosing the data-bit value that corresponds to the MAP probability for that data bit. Upon receiving a corrupted code-bit sequence, the process of decision making done with APPs allows the MAP algorithm to determine the most likely information bit to have been transmitted at each bit time. The BCJR algorithm can be applied in different techniques. By employing LUT-log MAP algorithm even if it works with high throughput

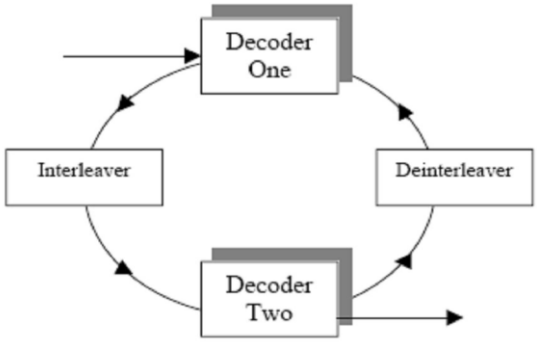


Fig. 1 Turbo encoder.

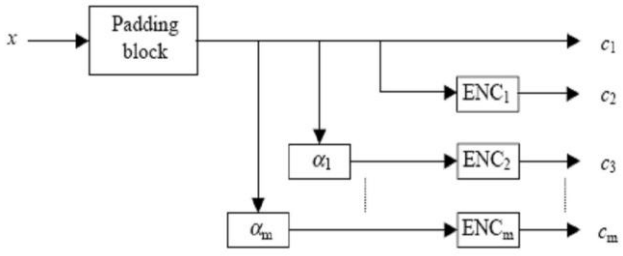


Fig. 2. Turbo Encoder

scenarios and results in best BER performance it is found to be most complex algorithm. It requires more memory and more number of values to be stored in lookup table. The Max-log MAP algorithm works with energy constrained scenarios and having least complexity but it is having worst BER performance.

The input of the TC encoder is a data block *x*, with *k* information bits. To this information sequence the padding block appends *v* (memory size) tail bits, which then yield the sequence *c*1. This sequence of bits is then fed in parallel into *m* parallel sets

of interleavers (αi) and encoders [7]. The aim of the interleaver is to scramble the sequence *c*1 before feeding the output of the padding block into other constituent encoders [5].

For turbo codes, the Soft Output Viterbi Algorithm (SOVA), and the Log-MAP decoding algorithm can be used as they produce soft-bit estimates. The Log-MAP decoding scheme is the modified version of the MAP decoding scheme and is computationally less complex than the original MAP decoding algorithm. However, due to the push for strikingly low bit error rates, the MAP or the Log-MAP has been most commonly used in turbo codes since they are based on the optimal decoding rule. In contrast, the SOVA is an approximation to the MAP sequence decoder and will have a slightly worse bit error performance. Though SOVA suffers from performance degradation as opposed to the Log-MAP decoding rules, it has much reduced complexity.

This motivated for the employment of constant-log MAP algorithm. This works with less memory, with 2 element LUT and performance and complexity lies between log MAP and max-log MAP algorithm. This work focuses on hardware implementation of turbo encoder and decoder that employs constant-log MAP algorithm.

Turbo encoder comprises of a parallel concatenation of two convolutional encoders, and both the encoder structure comprise of m number of memory elements. The information bit is fed to the upper convolutional encoder. This encodes the data to give parity bits. Also the information bits are interleaved and fed to the lower convolutional encoder which encodes the data to give parity bits. The two encoders generate completely different data sequence. The output of the turbo encoder is systematic (data) bits, parity output from the upper (uninterleaved) encoder and parity bits from lower (interleaved) encoder. The encoded data sequence is send through the channel where the data sequence is affected by noise. Then it is fed to the turbo decoder. The input to the decoder is Log-likelihood ratio (LLR). Both the decoders work with the constant-log-MAP algorithm. To obtain the LLR values for each data bit, certain parameters like α, β and γ are calculated. This calculation is based on the max* operation in the algorithm. The decoder works iteratively. The output from one decoder is given as input to the other decoder and this is repeated. The iterative concept solves the complexity of the decoding by enhancing the exchange of the a-priori (level of confidence) information from one decoder to the other. Finally, high confidence decoded data is obtained. The rest of the paper is organized as follows. Section 2 deals with related works, Section 3 shows the comparative analysis based on the review, Section 4 concludes the paper.

## II. RELATED WORK

Robertson P et al (1997) presented a comparison between log-MAP, max-log MAP and soft output Viterbi algorithm (SOVA) [3]. The comparison shows that SOVA is 0.7dB inferior to log-MAP and max-log-MAP lying in between SOVA and log-MAP. The comparative analysis is done for these algorithms in terms of number of additions, multiplication and look-up tables.

Gross W.J et al (1998) developed a simplified MAP algorithm suitable for the implementation of turbo decoder [4]. The simplification eliminates the need for a ROM or multiplexor-tree lookup table and replaces it with a constant value. The results show that the performance of turbo decoders is not adversely affected by this simplification.

Worm A et al (2000) presents a VLSI high speed MAP architecture with optimized memory size and power consumption for decoding the turbo codes [5]. The log-MAP and max log-MAP algorithm is used. Memory size is reduced by minimizing the FIFO memory size. For maximum throughput a fully pipelined architecture is considered. The area decreases by up to 11% and power consumption by up to 15% in case of a Log-MAP decoder and for a Max Log-MAP decoder, even an 18% area decrease and a 20% power decrease.

Wang Z (2002) introduced a variety of area efficient parallel turbo decoding schemes [6].Turbo decoders inherently have large decoding latency and low throughput because of iterative decoding. To reduce the latency and increase the throughput, high-speed decoding schemes are employed. So for that techniques like segmented sliding window approach and two other area-efficient parallel turbo decoding schemes .Comparison on storage requirements, number of computation units, and overall decoding schemes are made. Also in order to reduce the storage bottleneck partial storage of state metrics approach is also presented.

In 2003, Elassal M et al proposed a method to decrease the power consumption of turbo decoder [7]. In turbo decoder, decoding is done by iteratively exchanging the extrinsic information. In this proposed method the iteration is

terminated when the extrinsic information exceeds a particular threshold and then a predefined value is terminated. This reduced memory access for inter leaver and state metrics and thus power was reduced. 25% reduction of power consumption with energy per bit to noise power spectral density ratio Eb/No= 1.5 dB is achieved compared to conventional architecture.

Kwak J et al (2003) designed VLSI architecture for an efficient turbo decoder with parallel architecture to achieve high-throughput [8]. For 100% processing element utilization, a dividable interleaving method is proposed, in which it not only solves the memory conflict problem in extrinsic information memory, but also reduces the memory required for interleaver. It mainly consists of parallel decoding architecture using block partition method by maintaining the superior BER performance of MAP-based decoder.

Elmasry M et al (2004) designed rate 1/3, 8-state log-MAP turbo decoder architecture [9]. The simplified log-MAP algorithm is used for the component soft-in soft-out decoder (SISO). Several logic and architectural level techniques are applied through the design process to reduce power consumption, area and increase throughput of the turbo decoder Parallelism, quantization, resource sharing, logic reduction and normalization are applied to reduce area, power and throughput. 0.18µ CMOS technology is used [9]. The developed turbo decoder has a core area of 0.6mm2, clock frequency of 100MHz, power consumption of 63mW and energy efficiency of 2.5n J/b/iteration.

Tiwari M et al (2005) proposed the sliding window approach as a means for reducing memory requirements and decoding latency of MAP based SISO decoder [10].Optimal single-port memory sub-banking structure that supports very high throughput and low SISO decoding latency for a given sliding window configuration presented. The contributions include derivation of the optimal memory sub-banked structure for different SW (sliding window) configurations, also the study of the relationship between memory size and the energy consumption for different SW configurations and study of the effect of number of sub-banks on the throughput/decoding latency for a given SW configuration.

Atluri I et al (2005) formulated the implementation of a low power Log-MAP decoder with reduced storage requirement and based on the optimized MAP algorithm that calculates the reverse state metrics in the forward recursive manner [11]. The new low power derivatives of this decoder through a variation in the percentage of memory savings are presented. Three low power architectures of the Log-MAP decoder not employing the sliding window technique have been developed and post layout power savings of approximately 44%, 40% and 36% with respect to the conventional implementation have been observed. In 2008, Shah S presented a comparison between Viterbi decoder and turbo decoder. It shows that iteration decoders perform better than Viterbi decoders [12]. The trade-off between BER and (energy per bit to noise power spectral density ratio) Eb/No will always exist in the wireless communication world. This helps in reducing the transceiver power. The modulation techniques and BER performance of Viterbi and turbo decoders are compared. BER for Viterbi is 1.36 x 10-5; whereas for turbo decoder the values are 3.09 x 10-8, 8.00 x 10-8, and 4.35 x 10 -8 for number of iteration = 2, block size = 512; number of iteration = 8, block size = 512; and number if iteration = 8, block size = 2048respectively. The results show that turbo decoder is more powerful than Viterbi decoder with ~103 times improvements in BER.

Arai H et al (2009) proposed block-interleaved pipelining (BIP) architecture for high-throughput and energy efficient WiMAX turbo decoders [13]. Conventional sliding window (SW) BIP turbo decoders suffer from many warm-up calculations and large memory size when the number of pipeline stages is increased. This architecture results show that more than 50% of the warm-up calculation was reduced and necessary memory size became constant. The BIP WiMAX turbo decoders have implemented with 4 pipeline stages in the area of 3.8mm2 using a 0.18 µm CMOS technology. The chip achieves 45Mbps/iteration and 3.11nJ/b/iteration at 99 MHz operation.

Reddy P et al (2010) proposed a low power technique for turbo decoding implementation [14]. The digital base band implementation, high performance, energy efficiency, flexibility and low power are major requirements for channel decoding. The proposed techniques help meet the major requirements. The optimization techniques show an interesting gain in normalized energy efficiency between 4% and 54%. This approach can be extended for turbo decoder implementations in terms of area and throughput.

Martina M et al (2010) proposed the framework for the design and simulation of network-on-chip (NoC) based turbo decoder architectures [15]. Several parameters in the design space are investigated, like, network topology, the rate at which messages are sent by processing nodes over the network, parallelism degree and routing strategy. The result shows that the most suited topologies to achieve high throughput with a limited complexity overhead are generalized de Bruijn and generalized Kautz topologies. NoC based turbo decoder also reduces communication bandwidth by inhibition of unnecessary extrinsic information exchange.

Abughalieh N et al (2011) presented two error correcting techniques that suits the limited resources of the nodes in the wireless sensor networks such as Parallel Concatenate and the Serial Concatenate Turbo coding techniques [16].

It needs the benefits of increasing the data rate in WSNs by reducing the spreading rate. Results show that Serial Concatenation Turbo Codes shows better performance than the Parallel Concatenation Turbo Codes.

In 2012, Condo C et al focuses on one of the most important baseband processing units in wireless receivers that is the forward error correction unit, and proposes a Network-on-Chip (NoC) based approach to the design of multi-standard decoders [17]. This proposed architecture supporting the whole set of turbo and LDPC codes with higher throughput. BCJR algorithm is used. This design achieves a worst-case throughput higher than 70 Mb/s at the area cost of 3.17 mm2 on a 90 nm CMOS technology.

In 2012, Adiono T et al presented a design of turbo decoder VLSI architecture based on 3GPP-LTE standard [18]. In order to reach the LTE peak data rate of 326.4 Mbps, Max-log-MAP radix-4 decoding algorithm and parallelization of the MAP decoder are used in this work. The data dependency between each MAP decoder and hazard that comes from the usage of parallelization is explained. The modification made on the data flow and architecture of the branch/transition metric cache memory to increase the concurrency of parallelization method and to eliminate the hazard is introduced. Proposed design has a maximum throughput of 347.8 Mbps and FPGA implementation shows that the system can reach maximum frequency of 102.57MHz. Studer C et al (2012) analyzed on the silicon-area, energy-efficiency and throughput associated with SISO-MAP decoders based on the algorithm developed by Bahl, Cocke, Jelinek, and Raviv (BCJR) [19]. Developedradix-2 and radix-4 architectures for high-throughput SISO-MAP decoding of convolutional code's having 4, 8, 16, 32, and 64 states and presented corresponding implementation results in 180 nm, 130 nm, and 90nm CMOS technology. To achieve high throughput at low si(silicon)-area and power consumption, methods like windowing, modulo normalization and partial maximum sharing is employed.

Shrestha R et al (2013) explained sliding window approach for the Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm used in the design of MAP decoder [20]. High speed architecture for MAP decoder is an essential entity for the design of high throughput turbo decoder which is widely used in the recent wireless communication standards. The proposed MAP decoder architecture is implemented on field programmable gate array (FPGA) and the decoder operates at a maximum frequency of 346MHz.The method reduces the latency of the decoder in comparison with conventional method. The hardware result showed that the proposed decoder has high throughput suitable for 3G and 4G technologies. Li L et al (2013) proposed a framework that can be employed at an early design stage to estimate the processing energy consumption of the turbo decoder architecture [21]. This method reduced overall energy consumption that is transmission energy and processing energy. BCJR algorithm is used. By considering both the transmission energy consumption Ebtx and the decoding energy consumption Ebpr have to be considered right from the commencement of the design .The importance of optimizing the turbo codes at an early design stage is discussed.

Zhang K et al (2013) introduced the fixed-point implementation of LTE turbo decoder with Max-Log-MAP algorithm [22]. Also modular arithmetic was introduced to the state metric calculation and the scale process was introduced for extrinsic information calculation. With small hardware complexity, the resource overhead was reduced, and the working speed was improved. The result shows that the decoding performance is much better than traditional Max-Log-MAP algorithm and close to the Log-MAP algorithm, with a small degradation less than 0.1dB.

Carlo C et al (2013) designed a reconfigurable architecture for both turbo and LDPC codes decoding [23]. A reconfigurable NoC-based turbo/LDPC decoder architecture was developed and showing that wide flexibility can be achieved with a small complexity overhead. Results show that tailoring the proposed architecture to the WiMAX standard leads to an area occupation of 2.75mm2 and a power consumption of 101.5mW.

Li L et al (2013) proposed low-complexity energy-efficient Turbo decoder architecture [24]. Turbo codes have recently been considered for energy-constrained wireless communication applications, since they have low transmission energy consumption. However, for reducing the overall energy consumption, Look-Up-Table-Log-BCJR (LUT-Log-BCJR) architectures having low processing energy consumption are required. The proposed architecture achieves a low area and hence a low energy consumption. In this approach the LUT-Log-BCJR algorithm is decomposed into its most fundamental ACS operations. The architecture was validated by implementing an LTE turbo decoder and 71% energy reduction was achieved.

Roth C et al (2014) developed a new method for achieving parallel turbo decoding for peak throughput and wide range of code rates [25]. Algorithm used is sliding window SISO MAP or subblock parallel turbo decoding algorithm. Also it introduces a new approach that allows for a systematic throughput comparison between different SISO-decoder architectures, considering the trade-offs in terms of window length, throughput and error-rate performance into account. An analysis of existing architectures clearly shows that the latency of the sliding-window SISO decoders causes diminishing throughput

gains with increasing degree of parallelism. In order to remove this parallel turbo-decoder predicament, they proposed a new SISO-decoder architecture that leads to significant throughput gains and better hardware efficiency compared to existing architectures for the full range of code rates.

Martina M et al (2014) proposed a simplified n-input max* approximation algorithm for very low complexity turbo decoder hardware architectures [26]. The results show that the proposed architecture is simpler by 30%, on average, than the constant log-MAP in terms of chip area with the same delay. However, when applying scaling to the extrinsic information, the proposed algorithm achieves almost same Log-MAP turbo code performance for both binary and double-binary turbo codes, without increasing the implementation complexity.

Shrestha R et al (2014) presented an ungrouped backward recursion technique for the computation of backward state metrics [27]. MAP decoder based on this technique can be extensively pipelined and retimed to achieve higher clock frequency. The state metric normalization technique is employed in the design of an add-compare-select-unit (ACSU). This has reduced critical path delay of the decoder architecture. Turbo decoders with 8 and 64 parallel MAP decoders in 90nm CMOS technology is also designed and implemented. VLSI implementation of an 8 parallel turbo-decoder has achieved a maximum throughput of 439 Mbps and 0.11 nJ/bit/iteration energy-efficiency. Similarly, 64x parallel turbo-decoder has achieved a maximum throughput of 3.3 Gbps and 0.079 nJ/bit/iteration of energy-efficiency. These high-throughput decoders meet peak data-rates of 3GPP-LTEandLTE-Advanced standards.

From the above survey, it is clear that turbo decoders are best suited for wireless sensor networks. In turbo decoder, decoder works with number of iterations to calculate the values. Methods proposed for reducing these iterations is found to be increasing the latency. Sliding window SISO decoders causes diminishing throughput gains with increasing degree of parallelism. Thus in order to develop an energy efficient turbo decoder constant Log-MAP algorithm is used. Compared to other algorithms, constant Log-MAP algorithm is having least complexity and best performance.

## III. COMPARATIVE ANALYSIS

Table I - Performance Comparison of Viterbi And Turbo Decoder

| **Decoder** | **Performance** |
|---|---|
| Viterbi Decoder | R=1/2<br>BER= 1.36 x $10^{-5}$ |
| Turbo Decoder | R=1/3<br>BER=3.09 x $10^{-8}$, number of iteration = 2, block size = 512<br>BER=8.00 x $10^{-8}$, number of iteration = 8, block size = 512<br>BER=4.35 x $10^{-8}$, number if iteration = 8, block size = 2048 |

R= number of inputs/number of outputs (in the encoder)

BER= bit error rate

Table I shows performance comparison of Viterbi and Turbo decoder. It shows that Turbo decoder is more powerful than Viterbi decoder with ~103 times improvements in BER.

Table II Number Of Operations And Look Up Tables Required For Each Algorithm

| **Operation** | **MAX-Log MAP Algorithm** | **Log MAP Algorithm** | **SOVA** |
|---|---|---|---|
| Max operation | 5* 2M-2 | 5* 2M-2 | 3(M+1)+2M |
| Addition | 10*2M+11 | 15*2M+9 | 2*2M +8 |
| Multiplication | 8 | 8 | 8 |
| Bit comparison | 6(M+1) | Bit comparison | 6(M+1) |
| Look up tables | | 5*2M -2 | |

- Where M is an integer.
- SOVA- Soft Output Viterbi Algorithm used in Viterbi decoder
- Log-MAP , max Log-MAP, constant Log-MAP algorithms used in turbo decoder

Table II shows the comparison of arithmetic operations like addition, multiplication and number of look up tables required for different algorithms.

## IV. CONCLUSION

In this survey paper, literature review on different decoders suitable for wireless sensor networks is presented. A review on many algorithms used for decoding is done. Comparative analysis is shown for different parameters. Based on the survey it was found that turbo decoders are more appreciable for wireless sensor networks. It was observed that among many decoding algorithms constant log-MAP algorithm is more efficient and has lesser memory requirements.

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