Design and Analysis of CMOS based Ring Voltage Controlled Oscillator

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Abstract- This paper focuses on design and analysis of CMOS Ring Voltage Controlled Oscillator. This ring VCO is applicable for PLL application such as in, clock generation and recovery, frequency synthesizer. The ring VCO has frequency range from 1 MHz to 10 MHz and power consumption is 320μW. Transient response and phase noise analysis is performed and after simulation the phase noise at 1MHz is -96.05 dBc/Hz. The supply voltage VDD is 3.5V.

Keywords- Ring Oscillator, Voltage Controlled Oscillator (VCO), Current Starved Voltage Controlled Oscillator (CSVCO).

I. INTRODUCTION

In the field of VLSI design, the design of a linear and wide range voltage controlled oscillator for RF application is a challenging work for Electronics Engineers. VCO is the main component in the many RF circuits. VCO is the heart of Phase Lock Loop system. An oscillator is an autonomous system which generates a periodic output without any input. The VCO is an electronic circuit which produces the frequency signal depending on its input voltage. VCO is voltage to frequency converter. The Barkhausen criteria for oscillation can be met without resonators as in ring oscillators. If the open loop circuit exhibits sufficient gain at the zero phase frequency, oscillations occurs. The important requirements of VCO are Frequency accuracy, wide tuning range, tuning linearity, low power consumption, small size and low phase noise [1]. A voltage controlled oscillator (VCO) is one of the most important basic building blocks in phase locked loop. There are two different types of voltage controlled oscillators used in PLL, Source coupled VCO and Current starved VCO. A PLL is feedback system that compares the output phase with the input phase. [3]. VCO plays a critical role in wireless Communication systems it provide periodic signals required for timing in digital circuits. Oscillators can be divided into two categories; Firstly, the LC oscillator which is composed of the active devices, coupled with LC resonant circuit. Secondly, the loop ring oscillators which is composed of delayed cascade units with a positive feedback. The important requirements of VCO are High gain, wide tuning range, low power consumption and high signal to noise ratio.

This brief is organized as follows. In Section II different architectures of VCO described in detail. Section III shows the simulation results of VCO, and the conclusion is in Section IV.

II. ARCHITECTURES OF VCO

A VCO can be implemented through various architectures depending upon different requirements of a VCO like High gain, wide tuning range, low power consumption and high signal to noise ratio and other etc. constrains. Controlled oscillations through VCO can be generated using following architectures:

II. A. LC VCO

In this type of architecture active devices, coupled with LC resonant circuits are used. High frequency oscillations are generated using inductors and capacitors. Oscillating Sinusoidal wave is observed as output. This architecture is preferred where area and power are not constrains, as RL circuits can be bulky and more power consuming.

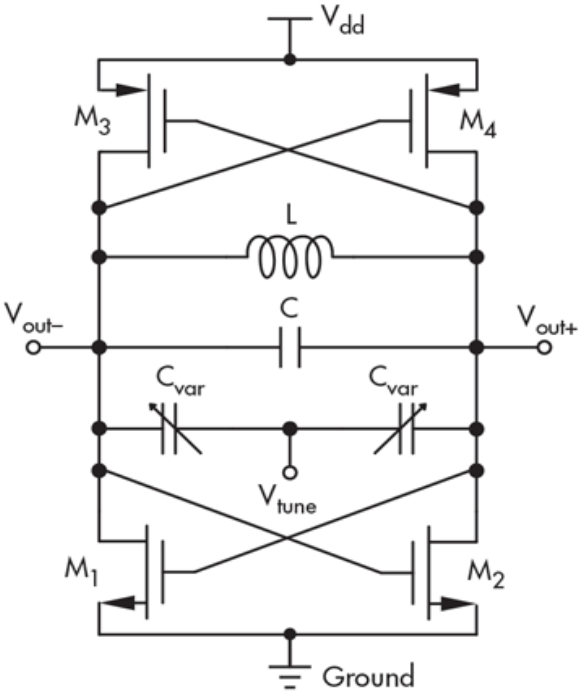

Fig. 1. LC VCO

II.B. SOURCE COUPLED VCO

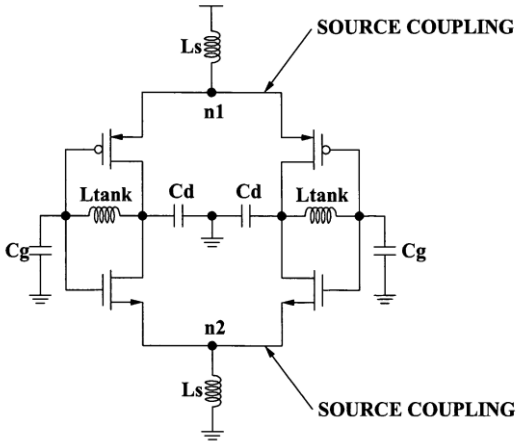

Fig. 2. Source Coupled VCO

These VCOs are made by using transistors connected back to back. This technique gives high frequency VCOs. These are also used to generate rectangular and saw tooth wave forms. These VCOs can be designed to dissipate less power than the current-starved VCO. The major disadvantage of these configurations is the need for a capacitor, something that may not be available in a single-poly pure digital process without using parasitic.

II.C. CMOS RING VCO

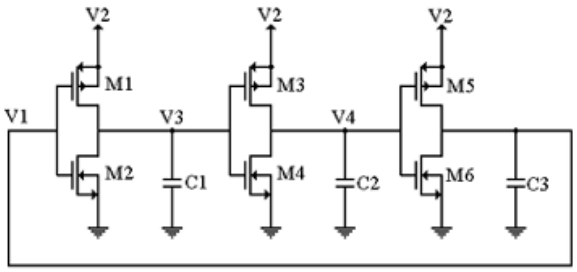

Fig. 3. CMOS Ring VCO

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of $\pi=N$, where N is the number of delay stages. The remaining phase shift is provided by a dc inversion [6]. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc

inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped. The ring oscillator works by controlling the charging and discharging of the gate capacitance of the next inverter. Decreasing the peak available charging current increases the time to charge and discharge the gate capacitance; consequently, the frequency is increcreased [7]. Ring oscillators generate high frequency up to 10 GHz.

II.D. CURRENT STARVED VCO

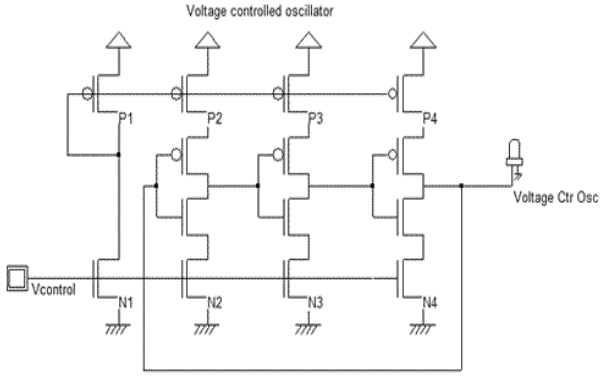

Fig. 4. Current Starved VCO

In the architecture of phase locked loop circuits VCO works as the heart of the circuits. The schematic diagram of current starved VCO is shown in Fig. 2. The circuit associated with two parts, current starving circuits and the inverter stages. The design objective of this article is to minimize phase noise and power of the CSVCO with a desired frequency of oscillation, subject to the physical compulsion. This circuit function is similar to ring oscillator, here five stage ring oscillator is used and a control voltage (Vctrl) is inputted with a supply voltage of 1 V applied in the circuits limit the current available to the inverter circuits. In other words, the inverter is starved for current. The oscillation frequency of current starved VCO for 'N' is represented as

$$f = \frac{1}{2NT} \qquad (1)$$

Where f = frequency of oscillation

N = Number of stages

$$\Gamma = t_1 + t_2$$

III. CIRCUIT OF CMOS RING VCO AND SIMULATION RESULTS

It is a cascaded feedback connection of odd number of inverters. The output of first inverter is input for second and in same fashion the output of last as input to first inverter as shown in Figure 1. The circuit forms and voltage feedback loop and thus does not have a stable operating point. The DC operating point at which the input and output of all the cascades inverters is equal to

threshold voltage Vth is unstable and any disturbance in the node voltages deviates the circuit from the unstable operating point, Vth After selecting the appropriate values for the parameters, the transient analysis of the ring oscillator is simulated as shown in Figure 2.

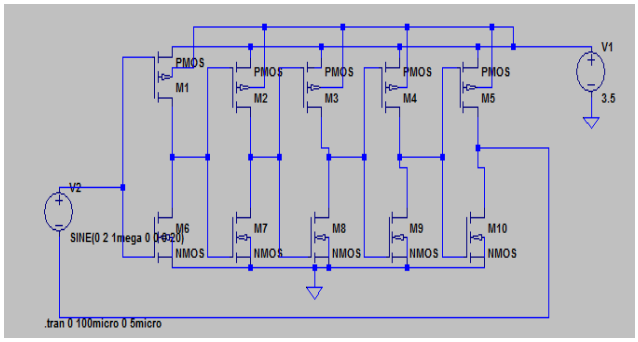

Fig.5. Circuit diagram of CMOS Ring Oscillator

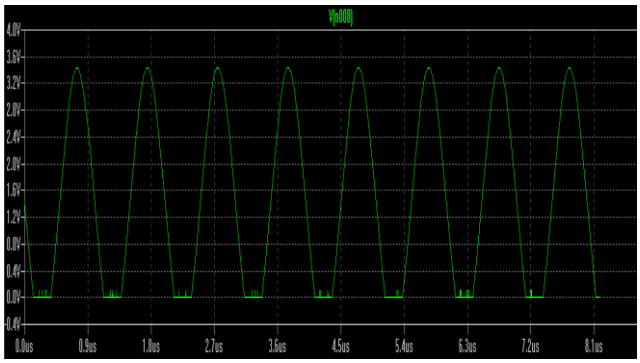

Fig.6. Transient Simulation

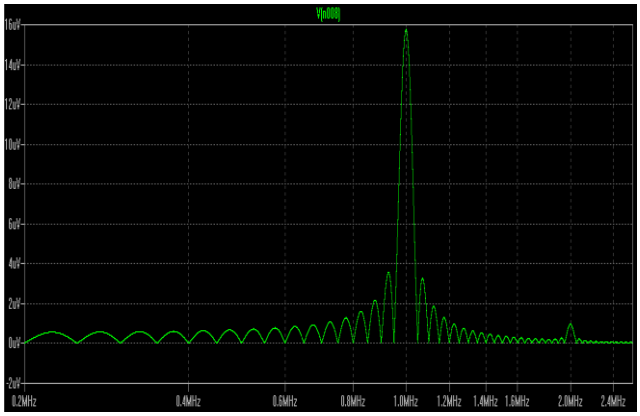

Fig. 7. Phase noise simulation

IV. CONCLUSION

The CMOS Ring VCO circuit is designed and simulated using LTspice software. The Ring VCO has frequency range from 1 MHz to 10 MHz and power consumption is 320µW. The supply voltage V_{DD} is 1.8V. The Ring VCO gives a linear voltage controlled oscillations, which is useful for PLL up to a certain high frequencies range.

REFERENCES

[1] B.Razvi, Design of ANALOG CMOS Integrated Circuits Tata Mc-GrawHill

[2] P. K. Rout, D. P. Acharya, and G. Panda, "A Multi-objective Optimization Based Fast and Robust Design Methodology for Low Power and Low Phase Noise Current Starved VCO," IEEE Trans. Semiconductor manufacturing, VOL. 27, NO. 1, Feb. 2014

[3] Pei-Kang Tsai, Tzuen-Hsi Huang, "Integration of Current-Reused VCO and Frequency Tripler for 24-GHz Low-Power Phase-Locked Loop Applications," IEEE Transactions on Circuits and Systems II: Express Briefs, , vol.59, pp.199-203, Apr. 2012.

[4] M. Kraemer, D. Dragomirescu, and R. Plana, "A High Efficiency Differential 60 GHz VCO in a 65 nm CMOS Technology for WSN Applications," IEEE Microwave and Wireless Components Letters, vol.21, pp. 314-316, June 2011

[5] M. Kumar "Design and simulation of low power PLL for wireless communication applications" IJETECS vol.1,issue 4 July 2012

[6] A.prajapati, P.P Prajapati "analysis of current starved VCO using 45nm CMOS Technology" IJAREEIE vol.3, issue, march 2014

[7] Kashyap K. Patel, Nilesh D. Patel "A Phase Frequency Detector and Charge Pump For DPLL Using 0.18µm CMOS Technology" International Journal of Emerging Technology and Advanced Engineering Volume 3,Issue1, January 2013.

[8] R.K Patil, V.G Nasre "A performance comparison of current starved VCO and source coupled VCO for PLL in 0.18um CMOS process" International journal of emerging and innovative technology vol.1, issue2, Feb. 2012.

[9] S. Verma, J. Xu, T. H. Lee, "A Multiply-by-3 Coupled Ring Oscillator for Low power Frequency Synthesis," IEEE J. Solid State Circuits, vol. 39, pp. 709-713, Apr., 2004

[10] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 µW wake-up receiver with 72 dBm sensitivity using an uncertain-IF architecture," IEEE J. Solid- State Circuits, vol. 44, no. 1, pp. 269–280, Jan. 2009.

[11] Liu, Huihua. "Design of low phase noise and fast locking PLL frequency synthesizer."International Conference on Electric Information and Control Engineering, pp. 4113-4116. 2011.