Design of Low Power Second Order CMOS Decimation Filter for ∑Δ ADC

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Abstract—Digital filter used for remove quantization noise, Casacaded Integrator Comb (CIC) architecture is a special class of filter to achieve required resolution of ADC with removing quantization error. Decimation filter is a combination of coder, integrator and digital differentiator with clock divider circuit. In this paper presents the power efficient CIC based decimation filter design and simulate using Cadence Virtuoso at 90nm technology.

Keywords—CIC, ADC, decimation filter, quantization noise.

I. INTRODUCTION

Actually signals are analog signal in real world, but analog to digital converter (ADC) helps to convert analog signal into digital domain for easier to evaluate and process. Digital to analog converter (DAC) also used for converted back digital signal into analog. There are many kinds of ADC that being widely used in the industry such as flash, successive approximation (SAR), pipeline, sigma-delta converter and others. Recently sigma-delta modulator has been widely usedinto the industry. Mainstays of Sigma-delta ADC are sigma-delta modulator and decimation filter.

The reduction in the effective sampling frequency is termed decimation. Thus decimation filter is used to reduce number of sample in discrete time signal produce from ADCs.

$$f_{s,new}=2B= f_s/2 \quad (1)$$

$$y[Ki * Ts] = \quad (2)$$

Basic block diagram of decimation filter is shown in Fig. 1, where input word passing through a digital filter and then down-sampling the result [1].

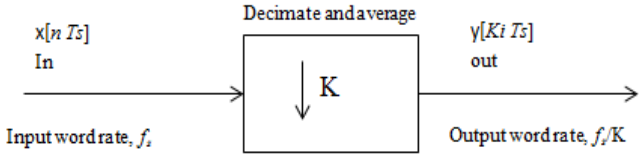


Fig. 1. Block diagram of Decimation filter

II. PREVIOUS WORK

The architecture of CIC decimation filter has an important effect on chip with respect to power and area. CIC filterchooses as the anti-aliasing filter to avoid quantization noise in PCM codes [2].The power dissipation of multistage decimation filter reduced when clock rate is same as the input sampling rate and also simplifies the clock generation [3]. Digital Finite Impulse Response (FIR) filter architecture based decimation filter realized using an effective multiplier-less structure which is minimize delay and area [4].

Decimation ratio between the two stages has significant influence on the stop-band attenuation for given oversampling ratio achieves maximum resolution, high resolution decreases the noise shaping and noise power [5]. There are many approaches to reduce power consumption of CIC decimation filter such as non-recursive architecture and poly phase implementation which eliminates the unnecessary computation [6].The operating frequency of comb filter is reduced by using polyphase decomposition in all stages, thus power consumption of digital filter also minimized with reducing operating frequency [7].CIC based decimation filter improves the gain response by using compensator and rejection of alias at pass-band interest [8]. Ternary FIR filter based decimation filter consist ternary full adder and ternary D-flip flop which is improving the filter performance and reduce the power dissipation [9]. Cosine filters has multiplier-less structure which is cascaded with CIC filter to achieve polyphase decomposition. Anti-alias rejection to be improves by using cosine filter [10].

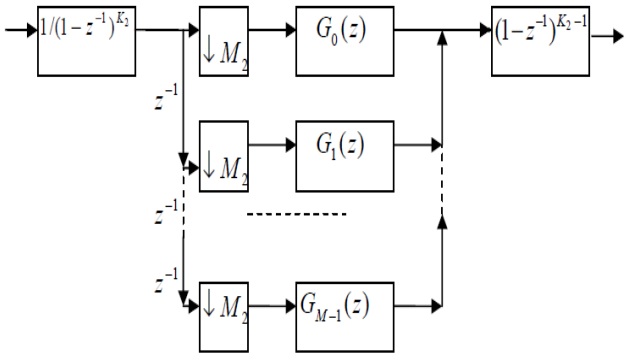


Fig. 2. Second stage CIC filter

III. CIC DECIMATION FILTER

CIC decimation filter is most frugal filter and also improve filter characteristic. CIC filter consist digital

integrator and digital differentiator, which performs digital low pass filtering and decimation at same time. Blok diagram of CIC decimation filter depicts in Fig. 3.

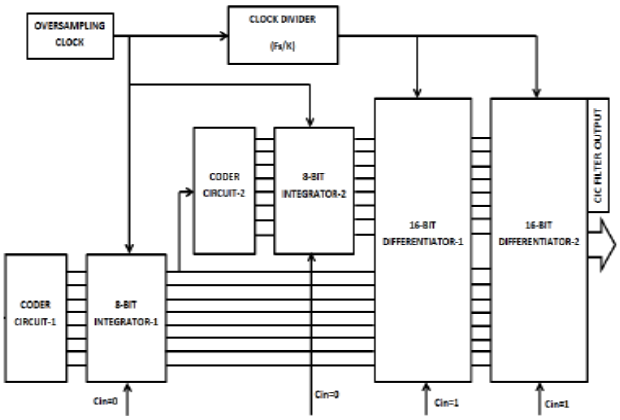
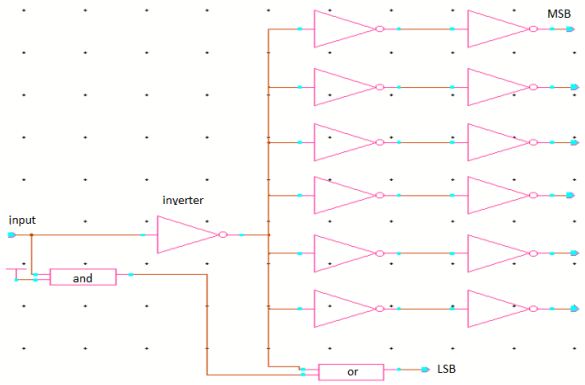


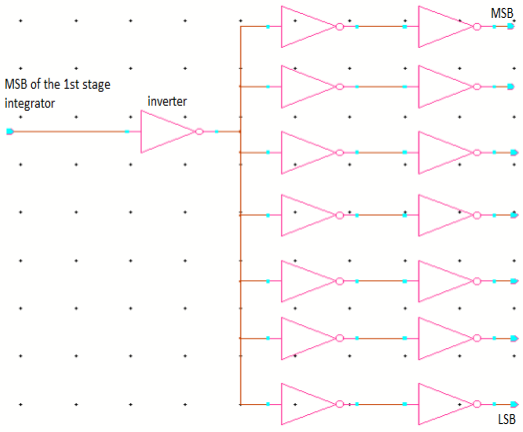
Fig. 3. 2nd order CIC decimation filter

A. *Coder Circuit*

Coder circuit is an important part in the design, used to increase the resolution of ADC or convert the single bit input signal into multi bit input signal.



(a)



(b)

Fig. 4. Schematic of (a) coder 1 (b) coder 2 circuit

Schematic of coder 1 and coder 2 circuit shown in Fig. 4, coder 1 circuit takes output of ADC as an input and converted into 7-bit input signal, coder 2 circuit takes MSB of 1st stage integrator as an input and converted into multibit input signals.

B. *Digital Integrator*

There are two 8-bit digital integrator is used in design, 8-bit integrator implement simply using 1-bit digital integrator with ripple carry adder. 1-bit digital integrator is combination of 1-bit full adder and delay circuit block diagram of 1-bit digital integrator is shown in Fig. 5.

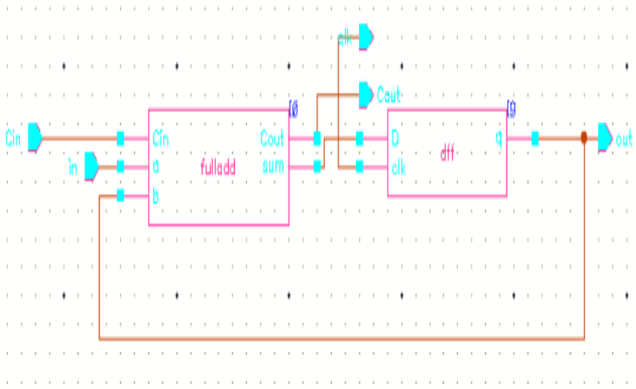


Fig. 5. 1-bit digital integrator

D- flip flop used as a delay circuit and 14-transistor full adder used which makes circuit more faster. Oversampling frequency used as a clock signal to activate the integrator circuit and produce the output. Schematic of 7-bit digital integrator interconnection of 1-bit digital integrator depicts in Fig. 6.

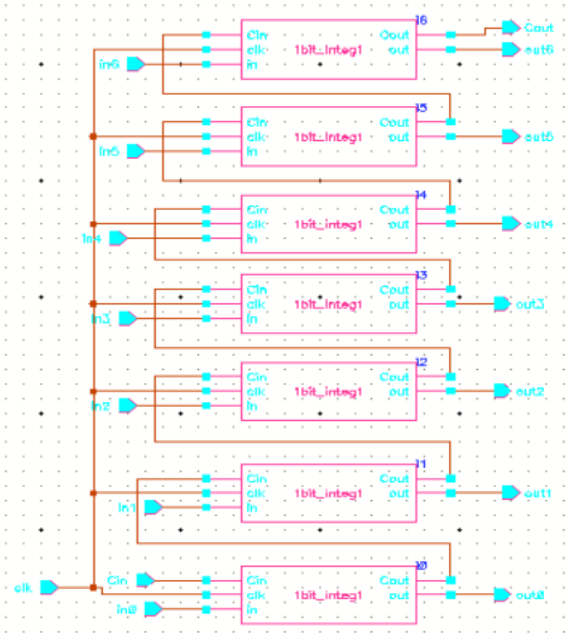


Fig. 6. 7-bit digital integrator

C. *Digital Differentiator*

Second order CIC filter consist two14-bit differentiator circuits in this design. 14-bit digital differentiator circuit

design interconnection of 1-bit digital differentiator, differentiator circuit activate by oversampling sampling frequency which is down-sampled by using clock divider circuit by 1/K and produce output. Schematic of 1-bit digital differentiator is shown in Fig. 7.

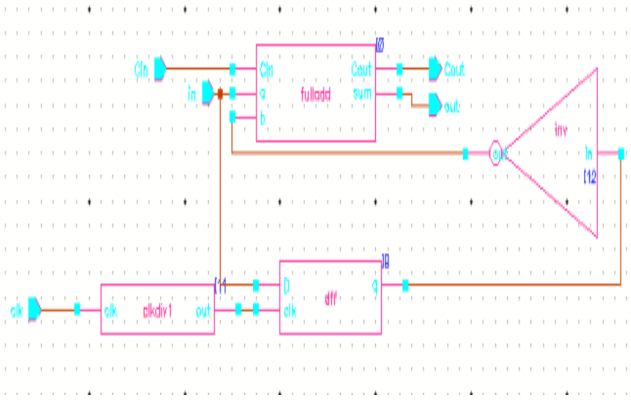


Fig. 7. 1-bit differentiator circuit

1-bit differentiator circuit is combination of full adder, inverter, clock divider circuit anb delay circuit, where tspc D-flip flop used as a delay circuit. Diifferentitator circuit is used for reducing power consumption and delay. 14-bit digital differentiator is shown in Fig. 8.

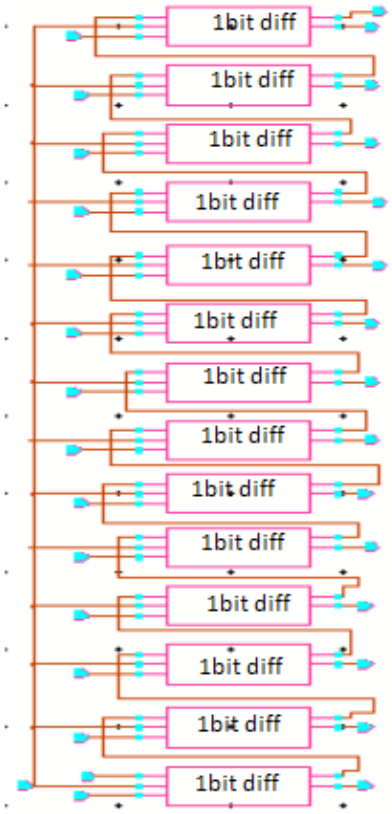


Fig. 8. 14-bit differentiator circuit

D. Clock Divider Circuit

Clock divider circuit used to down sampled oversampling frequency by 1/K, where K=64. Clock divider circuit design by using T- flip flop. Oversampling clock signal pass through a T-flip flop will be down sampled by factor 2 at every stage. Scematic of T-flip flop and clock divider circuit as shown in Fig. 9 and Fig. 10.

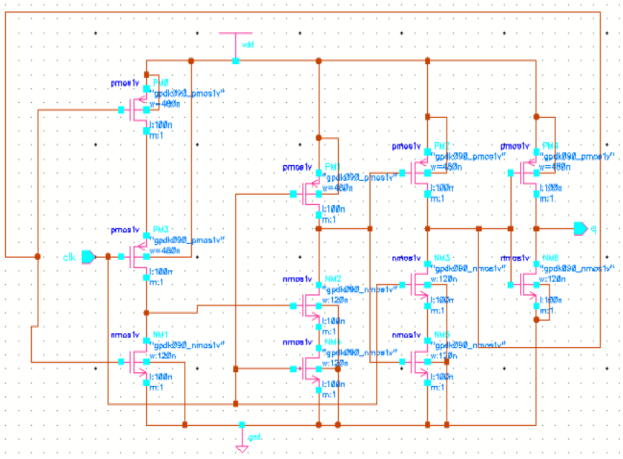


Fig. 9. Schematic of T-flip flop

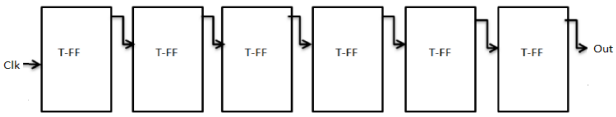


Fig. 10. Schematic of Clock divider circuit

E. Design of CIC Decimation Filter

Complete design of CIC filter is combination of coder, differentiator, integrator and clock divider circuit.

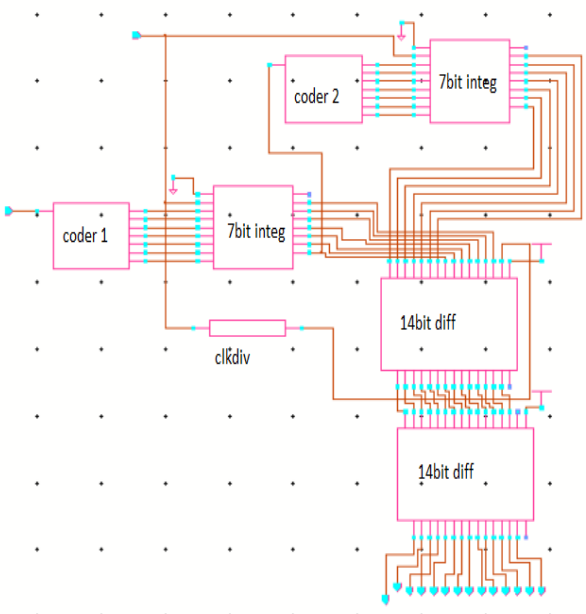


Fig. 11. 2nd order CIC Decimation filter

Coder circuit convert the single bit input signal into multibit input signal and passes to the digital integrator circuit which is work for change the phase response of the circuit. Output of an integrator circuit takes as an input signal for two stage digital differentitator circuit which is work on the concept of 2's complement method,

differentiator circuit is a summation of two inputs where second input is complement of first input and ouput produce after delay by $K*T_s$. Finally CIC decimation filter is design as a low pass filter and decimates at a same time. Schematic of CIC filter is shown in Fig. 11.

IV. Simulation And Result

All design is to be simulated using cadence spectre at 90nm technology with power supply 1.2V. Fig. 12 shows the simulation result of 1-bit digital integrator.

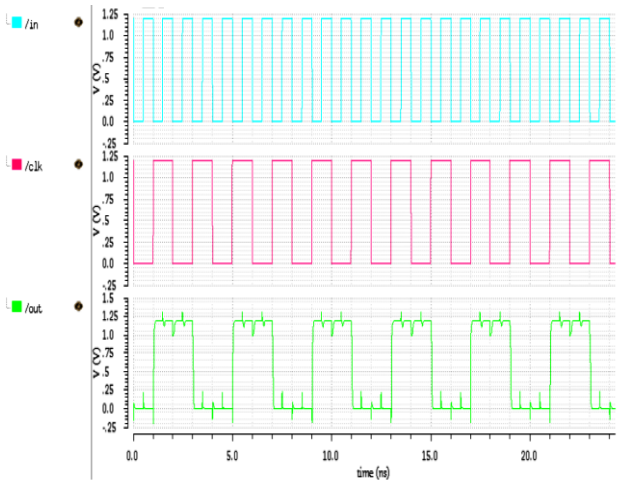


Fig. 12. Waveform of 1-bit digital integrator

Fig. 12 shows the waveform of clock divider circuit where F_s= 1GHz divided by K=64, thus Fs/K=15.625 MHz is used for activate differentiator circuit.

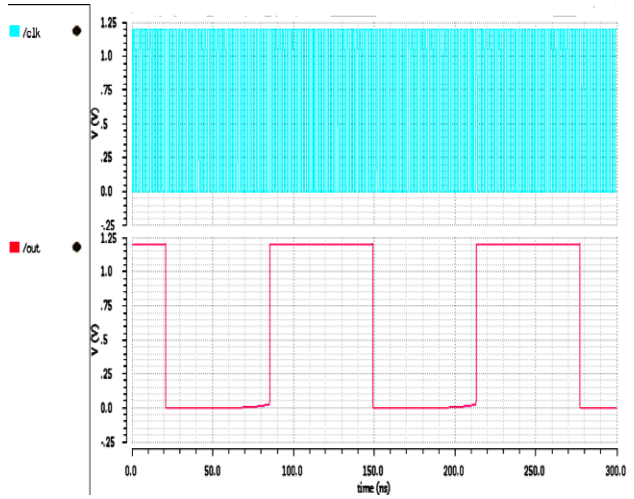


Fig. 13. Waveform of clock divider circuit K=64

When differentiator circuit activate, summing the input signal and 2's complement of input signal and produce output with delay. Basically it's a difference between two input signals. Waveform of 1-bit digital differentiator is shown in Fig. 14.

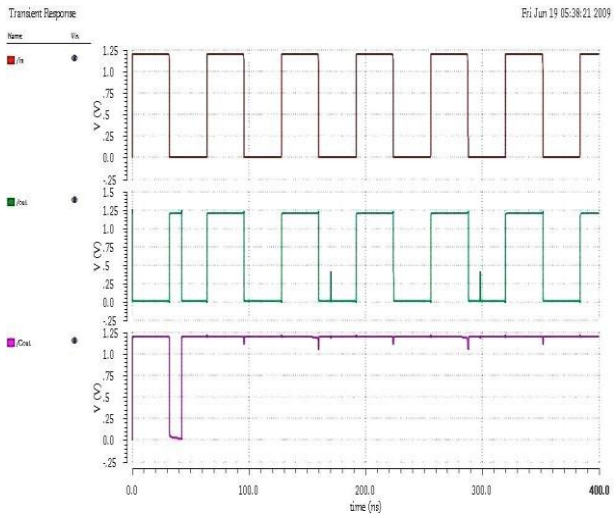


Fig. 14. Waveform of 1-bit digital differentiator

Finally decimation filter operate by oversampling frequency at 1GHz and filtered the input signal, produce the 14-bit output signal. Simulation result of decimation filter as shown in Fig. 15 and Fig. 16.

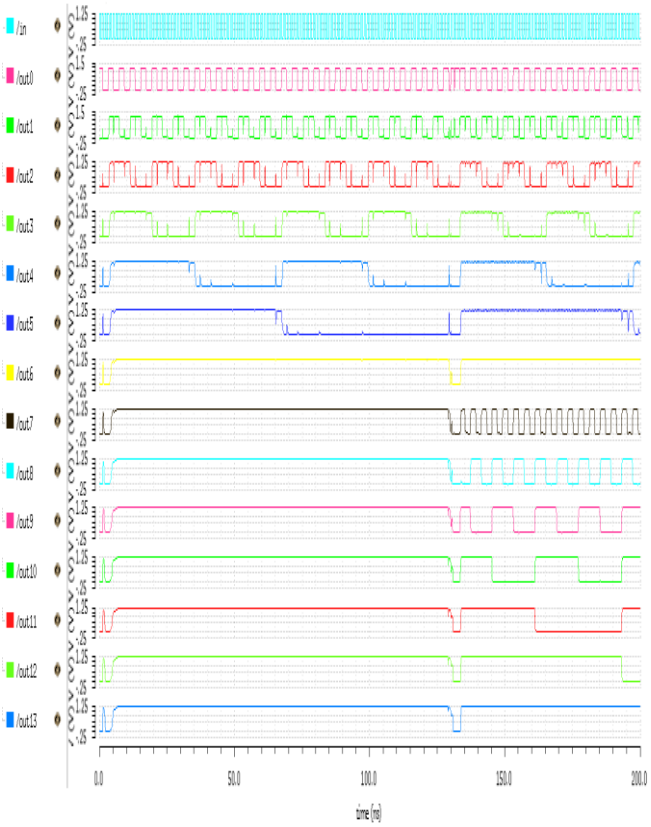


Fig. 15. Waveform of CIC decimation filter

Fig. 16. Now the CIC decimation filter reduce the quantization error of oversampling frequency and improve the anti alias rejection also reduce the power dissipation 80% as compare to previous design. TABLE I. shows the parameter of CIC decimation filter.

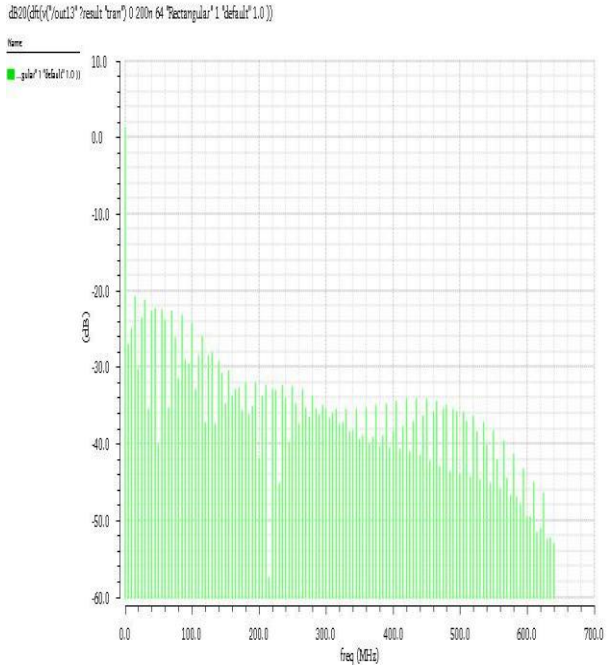


Fig. 17. DFT of CIC decimation filter

TABLE I. SUMMARY OF CIC DECIMATION FILTER

Design Specification	Parameter Value
Input badwidth	15MHz
Sampling frequency (fs)	1GHz
SNDR	36.82dB
Power Dissipation	1.51mW

Comparison of CIC decimation filter with previous work is shown in TABLE II in which power dissipation reduces80% and also improved SNDR. Fig. 12 shows the layout of CIC decimation filter.

TABLE II.COMPARISION OF PREVIOUS WORK WITH FDC VCO BASED QUANTIZER

Ref. No.	Input bandwidth	SNDR	Power Dissipation
[2]	1.024MHz	54.40dB	2.95mW
[7]	12.8MHz	31.2dB	16mW
[9]	11MHz	------	22.2mW
This Work	15MHz	36.2dB	1.51mW

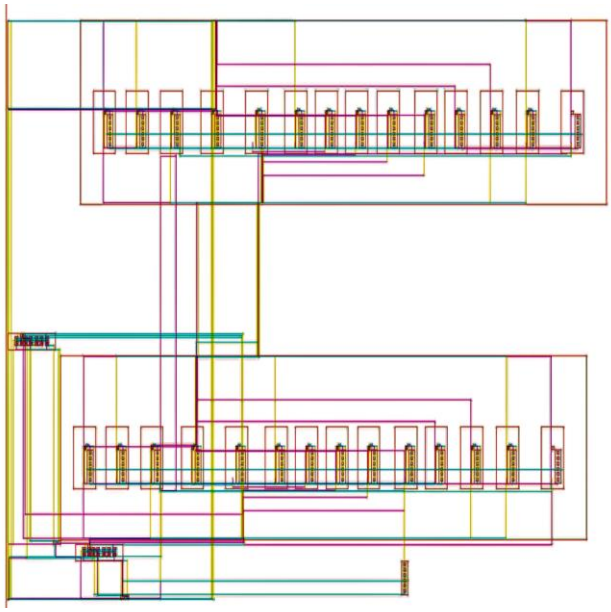


Fig. 18. Layout of CIC decimation filter

V. CONCLUSION

In this paper, decimation filter design using CIC architecture at 90nm technology. CIC filter implement by using coder circuit, differentiator, integrator and clock divider circuit. Polyphase implementation and multiplier less structure applied in CIC filter which reduces the power consumption 80% from previous work. Finally CIC decimation filter work as low pass filter and consumes less power.

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