

Study and Design of CMOS based LVDS Transmitter

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Abstract - This paper presents the design and study of LVDS (Low Voltage Differential Signaling) transmitter topology that compensates the effects of Electromagnetic Interference (EMI). A low voltage differential signaling (LVDS) is a method used for high speed transmission of binary data over copper cable. EMI is referred to as an externally produced electrical activity may generate noise. One of the most challenging task of the analog designer is to control of equipment against undesired operation due to EMI. The design of proposed LVDS transmitter to maintain a wide differential opening by achieving a superior common mode feedback circuit and also it overcomes the effects of EMI over LVDS transmitter circuit.

Key Terms- Low Voltage Differential Transmitter (LVDS), CMOS integrated circuits, electromagnetic interference (EMI), interference suppression.

I. INTRODUCTION

With continuous improvement of the integrated circuit technology, the demand for higher data throughput in electric system is increasing rapidly. As a solution, low-voltage differential signal (LVDS) transmitter has been widely investigated [1, 2]. LVDS transmission technology is a current signal transmission technology, with the logic level determinate the current direction (clockwise or counterclockwise) in the loop[3]. In LVDS transmitter, a clock generator produces high speed sampling clock signal to serialize the parallel input data. The serialized data is then driven by the LVDS driver. To lower the jitter of the output signal, the LVDS transmitter needs a low-jitter clock generator and a LVDS driver that can keep the output current stable. In addition, as high-speed data is being transmitted, the transmission line behaves as a low-pass filter. The high-frequency components of the waveform of the data sequence are filtered, which smooth the bit transition edges and lead to inter-symbol interference (ISI)[4,5,6]. Electromagnetic

interference (EMI), injected in the output nodes of integrated wireline chip to chip communication drivers via the transmission paths undesirably acting

as receiving antennas, can force these electronic circuits out of their operating region. Data transmission errors then become predominant as the injected EMI corrupts the transmitted data by causing unintended logic state

reversals due to the large amplitude excursions brought by the undesired injected signal. Additionally, as has been illustrated in previous works, the injected EMI causes severe dc shift errors inside the integrated transmitters themselves, driving the frontend blocks, both in the

transmitter and receiver, out of their operating regions [1], [2]. Low-voltage differential signalling (LVDS) is a predominant physical standard for wireline chip to chip communication [3]. As the miniaturization level of electronic systems increases,

the average distances between I/O cables and undesirable EMI sources are continuously reduced. This evolution constitutes a growing bottleneck not only for LVDS, but also for the overall integrity of most electronic devices. It was shown that as the radiated noise power applied along the LVDS transmission path is raised, the bit error rate increases

significantly: subsequently, a method for improving the EMS which uses the common-mode self-rejection of flexible printed cables was reported [4]. Although the results of [4] and [5] show that the EMS performance of LVDS communication systems can be significantly improved by redesigning the LVDS

bus, these solutions are impractical in terms of cost and development time which would be required to redesign a dedicated LVDS transmission path for each particular frequency range in industrial applications.

This paper present a low cost, effective, and power efficient LVDS driver used in the transmission paths. Section II discusses the effects of EMI when it is injected in the output of a classic LVDS transmitter, while Section III presents the LVDS transmitter circuit and the simulation results. A conclusion is presented in Section IV.

II. EMI EFFECTS IN A TYPICAL LVDS TRANSMITTER

A. LVDS TRANSMITTER.

An LVDS transmitter comprises a voltage-mode logic digital circuit, which transmits data through an output

voltage drop across the parallel equivalent of the transmitter's and receiver's terminations (R_T and R_R , respectively) as shown in Fig. 1. R_T and R_R are equal to $100\ \Omega$ and are placed at both ends of the transmission line for proper matching in accordance with the LVDS standard [3], [7]–[9]. Data are transmitted differentially and are toggled by altering

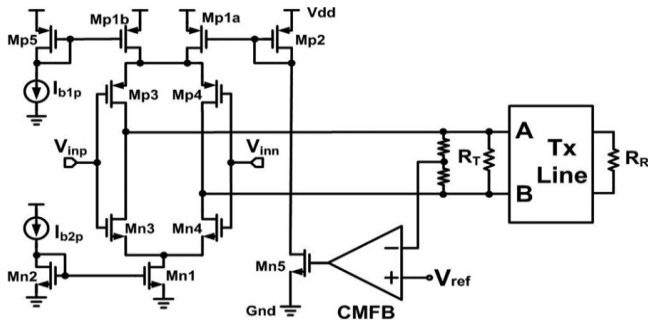


Fig. 1 LVDS Transmitter with CMFB

the current direction through switches Mp3, Mp4, Mn3, and Mn4, which are controlled by complimentary input signals V_{inp} and V_{inn} . The purpose of the common-mode feedback (CMFB) loop is to regulate and maintain the output dc level of the LVDS transmitter. Mp1a, Mp1b, and Mn1 act as current sources supplying a constant current to the transmitter.

B. EFFECT OF EMI ON LVDS TRANSMITTER

The transmission line acts as an undesirable receiving antenna that picks up EMI. For this reason, each wire of a differential transmission line is paired together in a way that an external EMI interference affects both wires simultaneously; thus, creating a common-mode disturbance which varies the transmitter's current drive. In an ideal differential transmitter, a common-mode variation has no effect on the differential signal. In a practical circuit, however, nonlinearities in the transmitter cause common-mode to differential-mode conversion. This is harmful because a common-mode variation caused by injected EMI at the transmission line degrades the differential signal to a point that it becomes totally unintelligible.

In an event of a high-frequency EMI injection, current source transistors Mp1a, Mp1b, and Mn1 are forced out of their saturation region when the common-mode EMI signal approaches the supply rails. Since the injected EMI varies the common mode voltage at a frequency higher than the CMFB bandwidth, the closed-loop system will not be able to negate the high frequency current variation. This current variation will translate into a voltage drop variation across the parallel equivalent of termination resistors R_T and R_R . A varying common mode also varies the output dc bias of the CMFB amplifier; thereby, varying the dc current through Mn5 and, hence, the total bias current provided by

Mp1a and Mp1b. This translates to a differential-mode distortion. The varying closed-loop gain of the CMFB network creates differential distortion as well. As the output common mode level varies with EMI, the closed-loop gain will vary as transistors shift out of their operating region by the significant EMI amplitude. The variation of the closed-loop gain causes the CMFB to fail dramatically when the common-mode level reaches the supply rail voltages.

A differential-mode distortion due to EMI causes the average differential amplitude to decrease closing the eye opening of the signal for increasing EM frequencies. The higher the amplitude of the injected EMI, the more the signal quality will degrade until the latter becomes unintelligible for the receiver.

III. LVDS DRIVER CIRCUIT AND SIMULATION.

Fig 2 shows an equivalent diagram of the driver. The driver tends to be a current-mode driver, driving the balance interconnect cable to a load consisting of the termination resistor. The current is steered down through the resistor and for the other, the direction of the current is reversed up through the resistor. The proper levels will not be obtained without the resistor

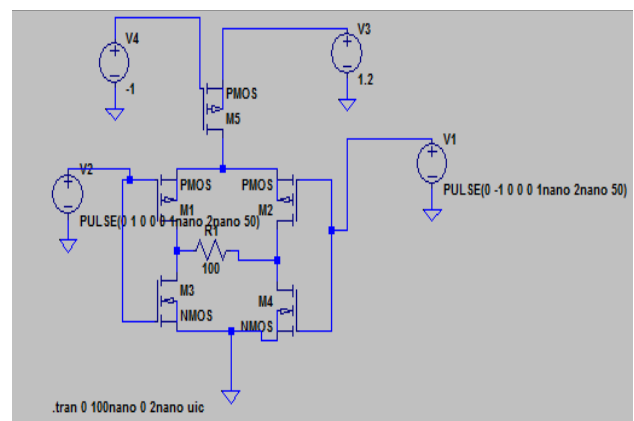


Fig. 2 LVDS Driver Circuit

in place as it completes the current loop. It is also needed to provide termination due to the fast edge rates. The current source driver minimizes switching spikes in the driver output structure. The receiver input is high impedance so that the majority of the current flows through the termination resistor and returns to the driver. This is known as odd-mode transmission. The odd-mode transmission is not only an EMI (electromagnetic interface) advantage, but also makes the signal path more tolerant to imperfections in the ground plane, thus another advantage. The LVDS interface driver, as shown in Fig. 2, has a low-voltage swing, it is connected to point-to-point and is achieved to very high data rates and is reduced by the power dissipation [1].

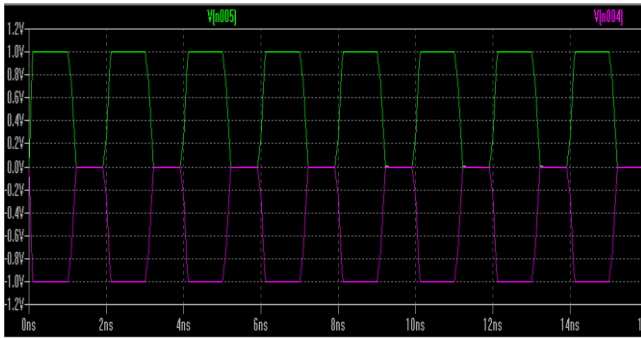


Fig. 3. Differential Signal to LVDS Driver

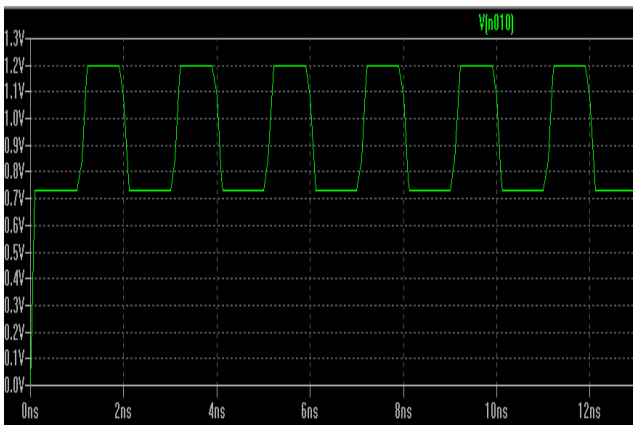


Fig 4. Output Voltage of LVDS Driver

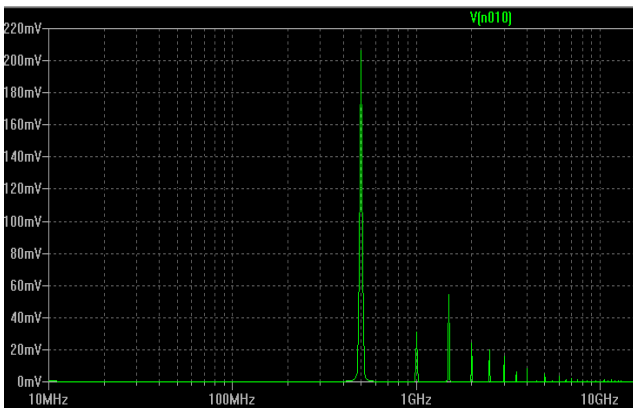


Fig 5. Simulated Phase noise

The LVDS uses differential data transmission and the transmitter is configured as a switched-polarity current generator. Due to the imperfect termination, package parasitic, component tolerances or crosstalk, there are reflected waveforms returning to the driver.

Typically, the LVDS signal is varied in magnitude from 1.1 V to 1.4 V.

The value of simulated phase noise is -15.86 dB/Hz at 536 MHz. A typical bridged-switched LVDS driver behaves as a current source with switched polarity. The bias current I_b is switched through the termination resistors according to the data input, and thus produces the correct differential output signal swing. It uses four transistor switches (M1-M4) in a bridged configuration. If switches M1 and M4 are

on ($V_{in} = \text{HIGH}$), then polarity of the output current is positive together with the differential output voltage. On the contrary, if switches M1 and M4 are off (switches M2 and M3 are on), the polarity of the output current and voltage is reversed. With a nominal 100Ω load at the receiver, both the common mode voltage and the differential swing at the output should fall within the The LVDS driver stage operates with a 3.5 mA (typical) current source that is always on. The logic ones and zeros on the bus are created by simply rerouting the current in different directions through the conductors of the differential pair. It is this always-on characteristic that eliminates switching noise and EMI. Designed for point-to-point signal transmission, the LVDS utilizes a simple termination scheme. A single 100-ohm resistor placed at the receiver input terminates the differential pair, thus eliminating reflections. Because of the high-impedance receiver input, the entire current of the driver's current source flows through the termination resistor generating a low, differential bus voltage of 250 mV nominal. This voltage swings around a 1.2 V common-mode potential, which is the typical driver output offset voltage. The LVDS standards define stringent specifications on the signal swings and signal levels.

IV. CONCLUSION

This paper describes the study of LVDS driver circuit and EMI on the LVDS. LVDS driver circuit consists of four MOS transistors i.e. (2 NMOS and 2 PMOS) combinedly called the CMOS. Differential input signal is given to LVDS driver and output is terminated to 100 ohm resistance. Performance of the LVDS driver is improved by adding common mode feedback which reduce the effect of induced EMI signal.

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