Performance Estimation of 9T SRAM Design Using FinFET

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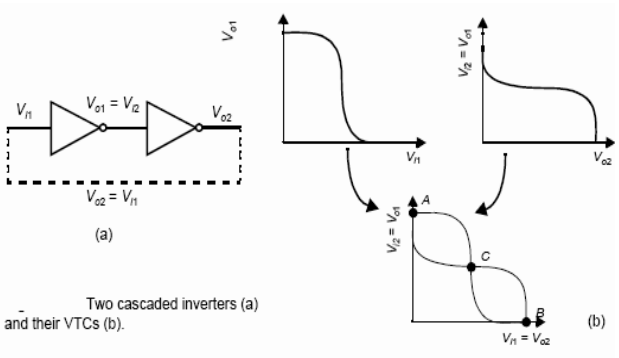
Abstract- In order to verify the robustness of an integrated circuit design, semiconductor manufacturers will fabricate corner lots, which are groups of wafers that have had process parameters adjusted according to these extremes, and will then test the devices made from these special wafers at varying increments of environmental conditions, such as voltage, clock frequency, and temperature, applied in combination in a process called characterization. FinFETs are 3D structures that rise above the substrate and resemble a fin, hence the name. The "fins" frame the source and drain, successfully giving more volume than a planar transistor for a similar region. The gate wraps around the fin, giving better control of the channel and permitting next to no current to spill through the body when the device is in the 'off' state. This, in turn, enables the use of lower threshold voltages and results in better performance and reduction in Short Channel Effects (SCEs). In this research we have utilize the property of FinFET technology for SRAM circuit design to lower power consumption. Proposed circuit design shows highest saving of dynamic power up to 76.57% in 4T, highest leakage power saving upto 53.21% in 6T at 250C and 45.13% at 1100C. Simulation result has been performed through HSPICE simulator by using Berkley Productive Technology model at 32nm.

Keyword:- SRAM, FinFET, Shorter Channel Effect, Multigate Device.

I. INTRODUCTION

SRAM cell consists of two cross coupled inverters. **S**tatic memory cells [1] basically consist of two cascaded connected inverters as seen in Fig. 1. The output of the second inverter (V_{o2}) is connected to the input of the first inverter (V_{i1}) consider the voltage transfer characteristics (VT) of the first inverter (V_{o1}) vs. (V_{i1})) and that of the second considering(V_{i2}=V_{o1} as shown in Fig. 1 and Fig. 2 respectively. It may be seen that operation points A, B are stable as loop gain is less than 1. Point A shows that the output of inverter1 is high and the output of the inverter2 is low. Point B shows that the output of inverter1 is low and the output of inverter 2 is high. This shows that the outputs of two inverters are complementary in any stable condition. This property is made use of to realize static random access memory SRAM.

Point C is a meta stable operating point as the loop gain at point C is much larger than 1. When a little deviation is applied to the input of the first inverter when the operating point is C, it gets amplified up by the gain of the primary inverter and is connected to the contribution of the second inverter and again enhanced by the gain of the second inverter. The values of V_{o1} and V_{o2} (V_{i2}) increases and the bias point moves away from C until it reaches either A or B.



Two cascaded inverters (a) and their VTCs (b).

Fig. 1 Back to back connected in- (c).

SRAM Architecture

The actual SRAM architecture based on CMOS inverters consists of two cascaded inverters A and B and two access transistors PG1 and PG2. The access transistors are connected between inverters and bit lines BL and BLB and their gates are connected to word line WL. The access transistors are turned on through the word line to enable writing and reading operation and turned off during hold condition.

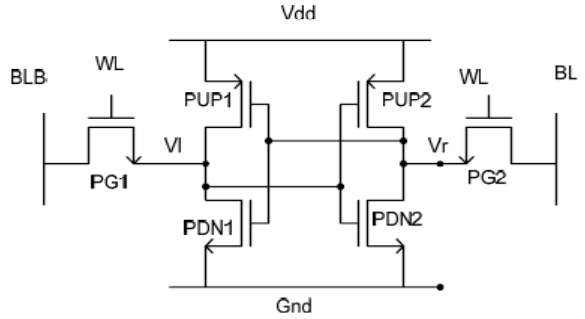


Fig. 2 Meta stability in SRAM shown in the transfer characteristics

Same ports are used for read and write operation. To operate the cell reliably, the sizes of the transistors should be properly designed. Since sense amplifiers (which are basically differential amplifiers) are used to read the data

quickly, the conventional *6T SRAM* is balanced and double ended. We know that system need memory devices to store information in bit format either 0 or 1, so in one case the there are two lines one is bit line and second one is bit bar here bit bar can also be treated as data bar and first one was the data line here the main emphasis is laid on the smaller size of memory cell and effective sensitivity.

To operate SRAM using lower operating voltage means increasing the cell stability and long life of the memories. Persistent shrinking of channel length builds the speed of devices and in substantial scale circuits. This relentless scaling down of transistor with each new era of mass CMOS innovation has yielded constant change in the execution of advanced circuits. Due to this scaling of CMOS device, significant challenges like Short Channel Effects (SCEs) occurs due to fundamental material and process technology limits.

Conventional 6T SRAM Cell

In traditional 6T-SRAM as shown in fig. 3 it has one word line and two bitlines which are required during a read and write operations. The cell must be both stable during a read event and writeable during a write event ignoring redundancy; such functionality must be preserved for each cell under worst-case variation. At the cell level, transistor strength ratios must be chosen such that cell static noise margin and write margin are both maintained, which presents conflicting constraints on the cell transistor strengths.

For cell stability during a read, it is desirable to strengthen the storage inverters and weaken the pass-gates. The opposite is desired for cell write ability a weak storage inverter and strong pass-gates. This delicate balance of transistor strength ratios can be severely impacted by device variation, which dramatically degrades stability and write margins, especially in scaled technologies. Low supply voltages further exacerbate the problem as threshold voltage variation consumes a larger fraction of these voltage margins. Variability can thus limit the minimum operating voltage of SRAM.

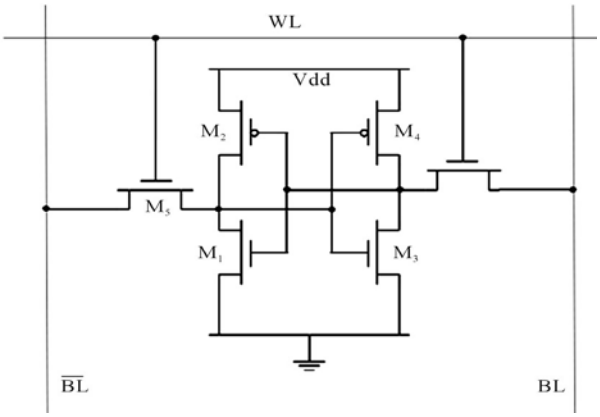


Fig. 3. Conventional 6T SRAM cell

II. SYSTEM MODEL

As mentioned earlier, the “traditional” FinFET structure evolved from an earlier device known as a fully depleted lean channel transistor (DELTA, Fig 4 a), that was originally introduced in 1989 [3]. The concept of multiple-gate FETs was already familiar, but the novelty of the DELTA resulted in development of similar devices.

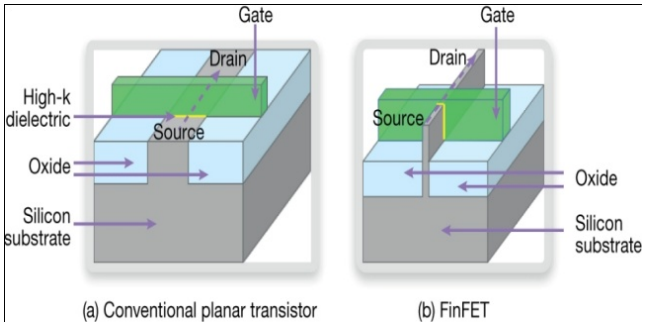


Fig. 4 (a) Conventional Planer Transistor (b) FinFET transistor, adapted from.

The DELTA and FinFET transistor both function on same principle. The body of the device (fin) is a relatively thin structure that connects the large source/drain pads. With a gate dielectric formed on the side of the fin, a conformal gate material is deposited to cover both sides of the fin, creating a tied double-gate transistor. The current conduction is thus on the side of the fin that connects source and drain, and the device channel width is often approximated as twice the fin height. The device current drive is easily increased by adding more parallel fins to the structure, as allowed by the source/drain dimensions. Although familiar for over a decade, these devices have garnered a lot of attention as of late. There have been several groups working on FinFET devices in recent years, with most research coming from University of California at Berkeley (UCB), IBM, and Intel.

Due to the unconventional nature of the device (sidewall channel conduction), transistor metrics can be interpreted several ways. It is important to note that for FinFETs, channel width is often defined as fin height. When compared to classical MOSFETs, the channel width that should be compared is actually twice the fin height. These concepts should be kept in mind when evaluating device performance from literature. The approaches taken in fin creation employ a variety of techniques: from electron-beam lithography [4] to conventional deep ultraviolet photolithography, and combinations of ultraviolet photolithography and spacer-based lithography. Research has often focused on the development of ultra-thin body structures to ensure full depletion, with some efforts concerned with reduction of etch damage in the channel region.

III. LITERATURE REVIEW

$FinFETs$: From Devices to Architectures, 7 September 2014 [1] Since Moore‘s law driven scaling of planar MOSFETs faces imposing difficulties in the nanometer regime, $FinFETs$ and $Trigate$ FETs have emerged as their successors. Owing to the presence of various (two/three) gates, $FinFETs/Trigate$ FETs can handle short-channel impacts (SCEs) superior to routine planar MOSFETs at profoundly scaled innovation hubs and in this manner empower proceeded with transistor scaling. In this research work, to audit inquire about on $FinFETs$ from the bottommost gadget level to the highest design level. Overview diverse sorts of $FinFETs$, different conceivable FinFET asymmetries and their effect, and novel logiclevel and engineering level tradeoffs offered by FinFETs. Likewise survey examination and improvement devices that are accessible for describing $FinFET$ devices, circuits, and architectures.

Saurabh Khandelwal et al, 2015 [1] implemented 6T SRAM cell using independent-gate DG $FinFET$ in view of the fact that scaling of gadgets in mass CMOS innovation prompts to short-direct impacts and increment in spillage. Static random access memory (SRAM) is relied upon to possess 90% of the range of SoC. Since spillage turns into the main consideration in SRAM cell, it is executed utilizing $FinFET$. Further, twofold gate FinFET devices improved as a decision for profound submicron innovations. With this thought in examination work, 6T SRAM cell is completed using self-ruling gate DG $FinFET$ in which both the inverse sides of doors are controlled freely which gives better flexibility to the SRAM cell. The device is executed utilizing diverse spillage lessening strategies, for example, gated-strategy and multithreshold voltage system to diminish spillage. In this way, control use in the SRAM cell is decreased and gives better execution. Free gate $FinFET$ SRAM cell utilizing different spillage lessening systems has been mimicked utilizing Cadence virtuoso device as a part of 45 nm technology.

Saurabh Khandelwal et al, 2013 [2] discovered a possibility for low power interconnect combination at the 45nm node and past, utilizing Fin-type Field-Effect Transistors ($FinFETs$) which are a promising substitute for mass CMOS at the considered gate lengths. They consider a component for enhancing $FinFETs$ productivity, called variable-supply voltage plans. It is outstanding that leakage savings utilizing transistor stacks is not viable in double-gate advances, for example, $FinFETs$, because of the nonappearance of body impact. Notwithstanding, transistor stacking alongside factor supply voltage operation of $FinFETs$ can offer bigger spillage funds contrasted with that of mass devices. In this research work, They’ve illustrated the design and implementation of $FinFET$ based 4x4 SRAM cell array by means of one bit 7T SRAM. FinFET based 7T SRAM has been designed and analysis have been carried out for leakage current, dynamic power and delay. Furthermore, 2:4 decoder has been designed and results obtained through proposed model have been verified. For the validation of their design approach, output of $FinFET$ SRAM array have been compared with standard CMOS SRAM and significant improvements are obtained in proposed model.

Saurabh Khandelwal et al, 2015 [3] proposed new leakage power reduction techniques namely series LSVL (lower self controlled voltage level) and after using it, leakage power reduces 20% for every increment of series transistor in lower ground connection. Leakage is found to contribute more measure of aggregate power utilization in power-streamlined $FinFET$ logic circuits. Their research work primarily manage the different rationale configuration styles to acquire the spillage control reserve funds through the sensible utilization of $FinFET$ rationale styles utilizing NOR based plan at 45 nm innovation. $FinFET$ circuits are unrivaled in execution and create less static power when contrasted with 32nm circuits. Finally, implementation of the schematics in CMOS NOR MODE, SG MODE, IG MODE, IG/LP MODE, LP MODE of NOR based FINFET is simulated by cadence virtuoso tools version 6.1 to obtain Leakage Power and Power Dissipation. By applying this they obtain 88% Leakage power savings through the judicious use of $FinFET$ logic styles having NOR based design at 45 nm technologies.

Vasundara Patel K. S. et al,2014 [4] explored technology that is relatively new and has not been explored in $FinFE$T technology. In their research work, a solitary cell Schmitt Trigger Based Static RAM utilizing $FinFET$ innovation is proposed and broke down. The most widely used semiconductor memory types are the Dynamic Random Access Memory (DRAM) and Static Random Access memory (SRAM). Competition among memory manufacturers drives the need to decrease power consumption and reduce the probability of read failure . The precision of the outcome is approved by method for HSPICE reenactments with 32nm $FinFET$ technology and the outcomes are then compared with $6T\ SRAM$ using the same technology.

Vandna Sikarwar et al, 2013 [5] designed a 6T SRAM cell using tied gate DG $FinFET$ as scaling of conventional CMOS circuit tends to have short channel effects due to which, effect such as drain barrier bringing down, hot electron impact, punch through and so on happens and thus leakage increments in the transistor. To minimize short channel impacts, twofold gate $FinFET$ is utilized. $FinFET$ might be the most encouraging device in the LSI (expansive scale coordination) circuits since it understands

the self-adjusted twofold gate structure effectively. Subthreshold spillage current and gate spillage current of inward transistors in the proposed cell are watched and contrasted and the ordinary structure of 6T SRAM cell. DG *FinFET* SRAM cell is connected with self controllable voltage level strategy and after that spillage current is watched. Reenactment is performed with rhythm virtuoso apparatus in 45 nm innovation. The aggregate spillage of DG *FinFET* SRAM cell is decreased by 34% in the wake of putting forth a concentrated effort controllable voltage level system.

IV. PROPOSED WORK

The Proposed circuit is shown in Fig. 5.1. Here in this the two extra PMOS transistor M_8 and M_9 has been used in the pull down network. As a result of the stacking of these two PMOS transistor in Pull Down system a voltage drop happens in crosswise over it. There is a NMOS transistor in parallel of PMOS stack in draw down system which is once in a while called assessment transistor. Therefore when the pull down network system is in standby mode this PMOS stack minimize the leakage current which directly diminishes the leakage power consumption of the circuit. The overall power consumption of the circuit is also reduces by using this technique. The adjusted plan utilizes a heap of PMOS transistor has been included the SRAM cell the schematic and setup of this approach work in a way so it can diminish the leakage to ground and in a roundabout way lessens the power scattering novel low-leakage-control configuration is depicted.

9T SRAM Cell-Working

The 9T SRAM cell is shown in fig. 5 This cell has 9T and it is like the conventional SRAM cell which has cross coupled inverters like the conventional cell. It is connected in PNN fashion that is one PMOS as Pull-up transistor and 2 NMOS one is for stacking purpose and the other Pull-down transistor. It has one discharging NMOS transistor ND. The RD signal is always connected to ground reference during the read operation. The data storage in the 9T cell is performed by the cross-couple inverters [7]. Two NMOS access transistors (PG) NA1 and NA2 connect to the virtual storage nodes (V1 & V2) to the write bitline pair when the write wordline (WDL) is on. N1 and N2 transistors are placed in between the pull-up PMOS transistors P1 and P2 and the pull-down NMOS transistors N3 and N4 of the cross-coupled inverters. RDL is read signal which controls the read port. N3 and N4 are the pull down transistors. During read the RDL signal is grounded so that there will be less power consumption. There is only one word line for reading and writing. During write "1" keep BL as high and also WDL and RDL high. Similarly during write "0" we can keep BL as "0". During read keep WDL and RDL as "0".

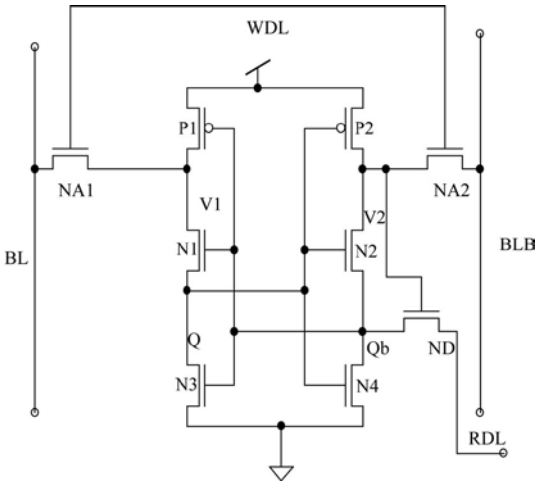


Fig. 5 9T SRAM

V. RESULTS AND DISCUSSION

The circuit is simulated using HSPICE simulator at 32 nm at *FinFET* technology with supply voltage of 1V output capacitance is of 1pF at temperature 25^0C and 110^0C with operating frequency of 10MHz. As leakage current reduces shorter channel effect (SCE) reduces, according to the simulation results saving of dynamic power dissipation in proposed circuit with existing circuit is 76.57% at 4T, 51.59% at 6T, 46.31% at 7T, 51.21% at 8T, 38.14% at 9T and 82.21% at 10T. Similarly saving of the leakage power is 15.52% and 18.35% at 4T, 53.21% and 38.75% at 6T, 16.74% and 17.58% at 7T, 20.65% and 23.13% at 8T, 47.53% and 45.71% at 9T, 44.40% and 34.36% at 10T with temperature of 25^0C and 110^0C respectively.

Table.1 Results of Proposed 9T SRAM Cell

SRAMS	Average Power Consumption(μW)	Delay (pS)		Leakage Power (nW)	
		Maximum	Minimum	25^0C	110^0C
4T	0.7896	19.323	5.657	20.1	502.2
6T	0.3822	6.0423	2.161	36.12	682.5
7T	0.3446	2.3644	2.358	20.3	507.2
8T	0.3792	3.429	0.149	21.3	543.8
9T	0.2991	2.469	0.088	39.8	770.0
10T	1.040	3.192	0.426	30.40	636.9
Proposed	0.185	3.305	1.647	16.90	418.0

Circuit					

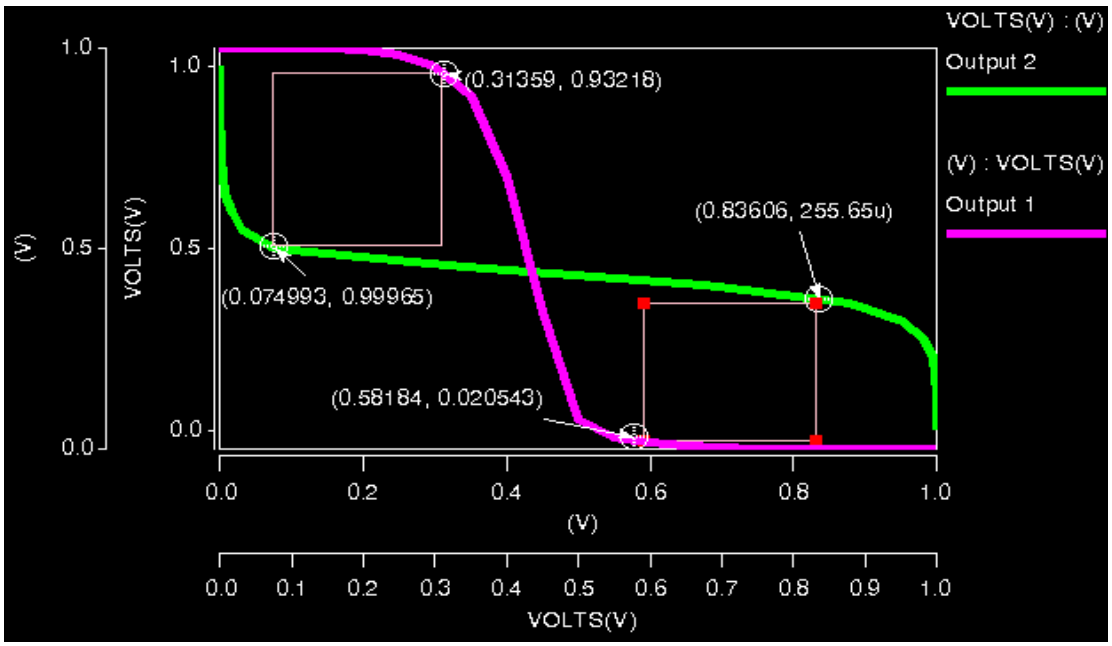


Fig. 6.1 SNM Butterworth Curve of Proposed 9T SRAM Cell.

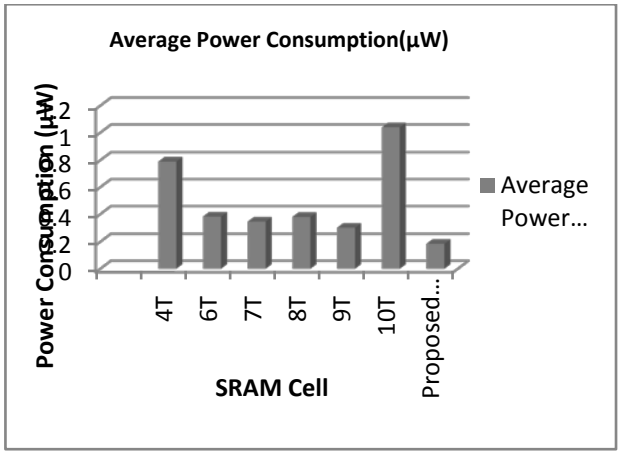


Fig. 6.2 Average power consumption of existing and proposed SRAM cell.

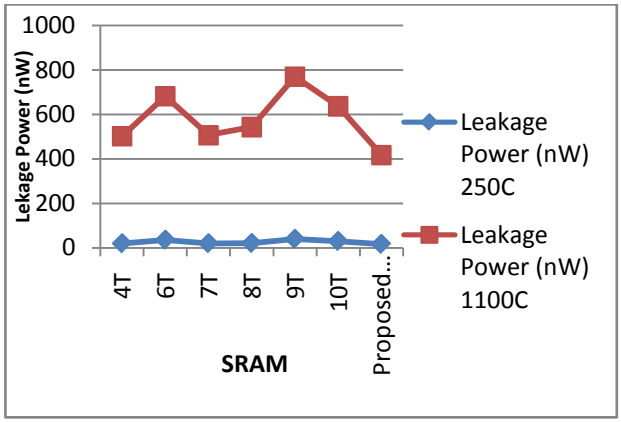


Fig. 6.3 Leakage power consumption of existing and proposed SRAM cell at 25^0C & 110^0C.

VI. CONCLUSION

As the dimension of CMOS devices is scaled down to several tens of nanometers in gate- length, $FinFET$ with multiple gates presents an effective solution to controlling the short channel effect. The Schottky barrier source/drain technology has been discussed as the most promising solution to reducing the parasitic series source/drain resistance for $nanowire - Fins$ surrounded by multiple gates. In this research work, a new 9T SRAM cell structure for low leakage and high stability and improve write stability. The proposed circuit is based on 6T SRAM cell, which consist of footer transistor to reduce the static power. The efficiency of the existing cell $4T, 5T, 6T, 7T, 8T, 9T, 10T$ and proposed is calculated and its characteristics were compared. The simulation results shows that proposed circuit shows saving of delay, average power, static noise margin (SNM), Leakage current, Frequency. This method is useful because it got the same butterfly diagram as 8-T SRAM. The numerical values of the proposed circuit from table 1 are Average Power consumption (0.185µW), Delay (pS) Maximum (3.305), Minimum(1.647) & Leakage Power(nW) (16.90) at 25^0C , (418.0) at 110^0C.

REFERENCES

[1] P. Sharma, S. Khandelwal and S. Akashe, "Design & Optimization of FinFET Based Schmitt Trigger Using Leakage Reduction Techniques," 2015 Fifth International Conference on Advanced Computing & Communication Technologies, Haryana, 2015, pp. 70-74.

[2] Saurabh Khandelwal," Leakage Current And Dynamic Power Analysis Of Finfet Based 7t Sram At 45nm

Technology" The International Arab Conference on Information Technology (ACIT'2013)

[3] V. Gupta, S. Khandelwal, B. Raj and R. D. Gupta, "Leakage current reduction in finfet based 6T SRAM cell for minimizing power dissipation in nanoscale memories," 2015 5th Nirma University International Conference on Engineering (NUiCONE), Ahmedabad, 2015, pp. 1-5.

[4] S. Sandesh, Niranjan S, S. B. Bhargav, Sneha B and Vasundara Patel K S, "A novel architecture implementation in RF Amplifier using CMOS 180nm technology," 2015 IEEE International Advance Computing Conference (IACC), Banglore, 2015, pp. 1185-1190.

[5] V. Sikarwar, S. Khandelwal and S. Akashe, "Optimization of Leakage Current in SRAM Cell Using Shorted Gate DG FinFET," 2013 Third International Conference on Advanced Computing and Communication Technologies (ACCT), Rohtak, 2013, pp. 166-170.

[6] S. Singh, N. Arora, N. Gupta and M. Suthar, "Leakage reduction in differential 10T SRAM cell using Gated VDD control technique," 2012 International Conference on Computing, Electronics and Electrical Technologies (ICCEET), Kumaracoil, 2012, pp. 610-614.

[7] E. Grossar et al., "Read stability and write-ability analysis of SRAM cells for nanometer technologies," IEEE J. Solid-State Circuits, vol.41, no. 11, pp. 2577–2588, Nov. 2006.

[8] B.H. Calhoun and A.P. Chandrakasan, "A 256-kb 65-nm Subthreshold SRAM Design for Ultra-Low-Voltage Operation", in *Solid-State Circuits, IEEE Journal of, Volume 42*, Issue 3, pp. 680 - 688, March 2007.

[9] Mayank Shastri, Shyam Akashe, "Read Write Stability With Leakage Minimization Of 4t Sram Cell For Nano Cmos Technology" in Proc. of IEEE, pp. 355-359, 2011.

[10] Anie Jain, Shyam Akashe, "Optimization of low power 7T SRAM cell in 45nm Technology" in Proc. of Advanced Computing & Communication Technologies IEEE, pp 324-327, 2012.

[11] K. Dhanumjaya, M. Sudha, M.N.Giri Prasad, Dr.K.Padmaraju, "Cell Stability Analysis of Conventional 6t Dynamic 8T Sram Cell In 45nm Technology" VLSICS, vol.3, no.2, pp. 41-51, April 2012.

[12] Hiroki Noguchi et al., "Which is the best dual port SRAM in 45nm process technology8T,10T single end and 10T differential" Renesas Technology corporation,2008.

[13] Zhiyu Liu, Volkan Kursun, " Characterization of a novel Nine Transistor SRAM cell,IEEE Transactions on Very Large Scale Integration Systems,voI. 46, Issue 4,April 2008.pp-488-492.

[14] Neil H.E.Weste,David Harris and Ayan Banerjee, "CMOS VLSI Design, a circuits and systems perspective" ,ISBN: 0321149017/9780321149015 Third edition, Pearson Education, 2005.