Asynchronous Router for Low Area Utilization on FPGA

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Abstract - Network-on-Chip handles the communication between the numbers of cores on a chip. The demand of processing element is rapidly increasing but its area parameter remains constrained and to improve the efficiency of router area reduction is an important factor. In this paper we design asynchronous router for low area utilization on SPARTAN 3E FPGA and compared with previous work. To communicate between router XY routing algorithm and wormhole switching technique is used. The proposed router utilizes 141 slices and NoC operate at 226.09MHz frequency.

Keywords: Network-on-Chip(NoC) , area, crossbar, router, buffer.

I. INTRODUCTION

A system on chip (SoC) contains bus architecture it creates communication problem when number of core are increase. NoC handles this problem of communication in a efficient way and it is a new proposal to SoC design. NoC interconnect various IP cores using on chip network. NoC provides new methodology to on-chip communication and improve efficiency and scalability over bus systems. NoC is data packet based communication network. It has many resources and all resources are connected through router. Because of its parallel communication mechanism NoC has higher performance and wider bandwidth. Now a day's many complex SoC designs contains asynchronous clocking mechanism.

The rest of this paper is organized as follow: section II presented router input port and output port. Section III presents the results and section IV presents conclusion.

A. NOC Architecture

The architecture of a 3x3 NoC connected in 2D mesh style is shown in Figure 1. Routing nodes, IP Core, Network Interfaces, and Physical links are the component of NoC. The router consists of bidirectional interfaces. Four are connected to the neighbouring routers with the help of physical links and the fifth one is connected to the local port through the Network Interfaces. The NoC architecture supports different network topologies depends on application requirements.

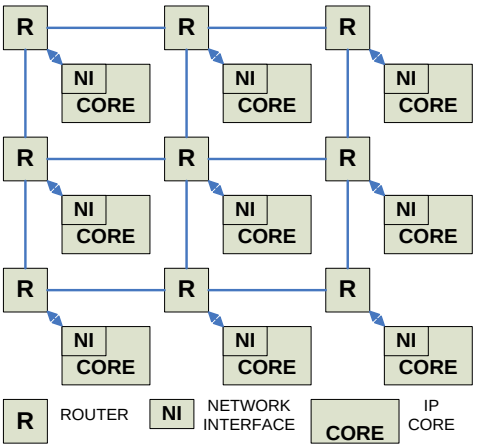

Figure 1. Noc example with elements

B. Asynchronous Communication Mechanism

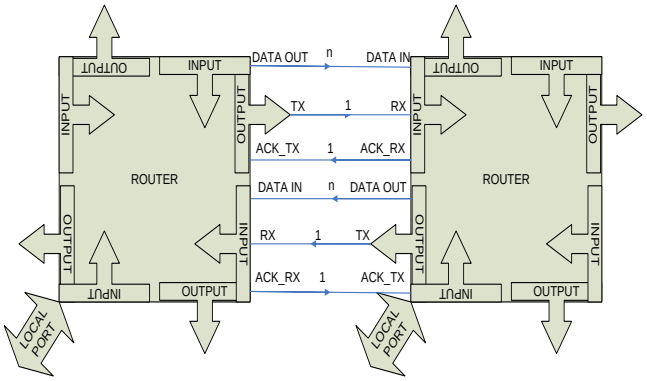

Figure 2. Handshake protocol between two NoC routers

To communicate between routers, handshaking communication protocol is used when data is received at the input of the router it transmits its confirmation to the sender router. So in summation to the flits sending and receiving channels, transmit (TX), acknowledge (ACK-TX), receiver (RX) and acknowledge (ACK-RX) signals required. Whenever the data is available in the output port TX equals to one and waits for ACK-TX to be equalled to one. Likewise RX input is one, reads the data and equals the ACK-RX output to one. The link between two neighbour routers is shown in Figure2.

II. PROPOSED ROUTER

The proposed Asynchronous router is a combination of 5 input and output ports and has five directions like east, west, north, south and local and every port connects other

ports. The design implements 2D-Mesh Topology using XY routing algorithm and wormhole switching techniques having flit size 32 bits. The block diagram of the proposed router is shown in Figure 3. The switching directions are encoded using three bits as listed in Table I. The communication between input and output port is carried by crossbar switch.

The routing algorithm which is used by various designs is XY algorithm. This algorithm guaranteed dead-lock free routing. This algorithm is deterministic algorithm in which packet takes routing in one dimension and it continues till this packet attains the desired coordinate in that dimension. First routing takes place in X direction and then in Y direction with respect to coordinates.

In the proposed work, a wormhole switching technique is used as it buffers low amount of data and hence, the router directly forward the received flit to the next port without waiting for the new flits. Moreover, the router stores only one flit at time and thus resulted in low area requirement. This is achieved by using a FIFO buffer for each input and output port.

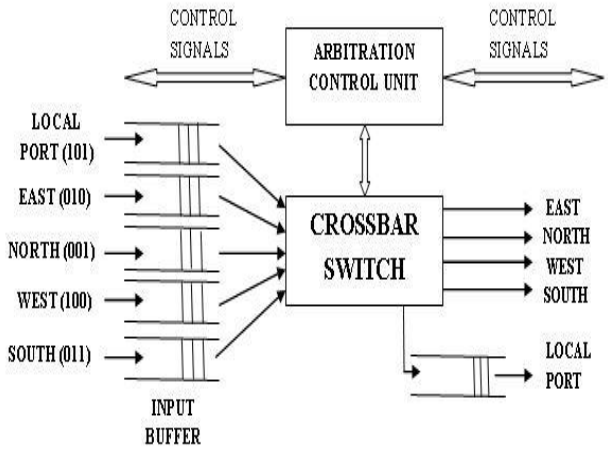

Figure 3. The Asynchronous NOC Router

C. Input Port :

The input port route the packet to the output port. The switching direction is controlled by multiplexers, the header (rh), intermediate (ri), and end requests (re). The first arriving flit is the header flit which has information about the switching direction. Three MSBs of the header flits store switching directions

These three switching bits first latched and then used for control input to the multiplexers. The switching direction must be same for all flits belongs to the same packet. So, latch is controlled in such a way that when header request signal (rh) is high it is transparent.

The data signal should be treated differently with respect to flit type. If it is header flit then data rotate three bits and if it is end or intermediate flit the data must be passed directly. To maintain data validity scheme the multiplexer is controlled by OR gate and C-element, with the rh and ack_in as input.

The delay is provided to all request channels. Delay should be provided to head request signal until the requested de-multiplexer control signal is stable otherwise glitch may appear.

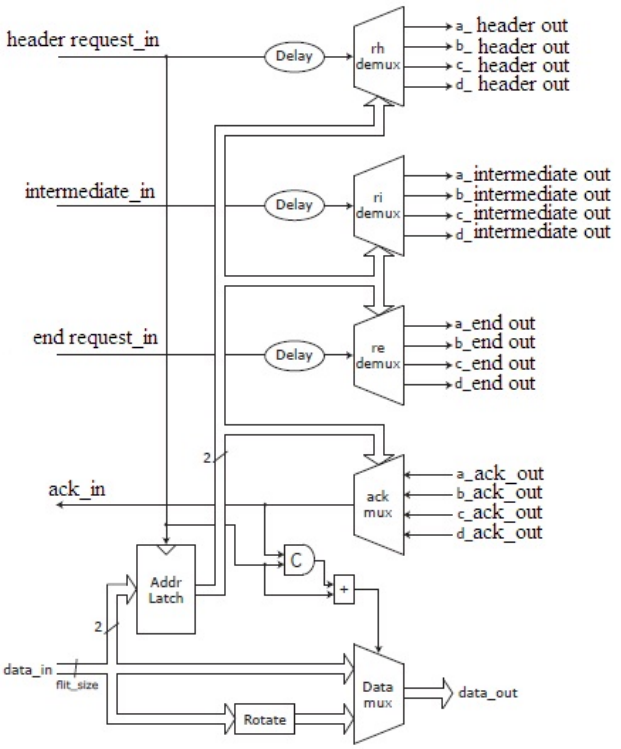

Figure 4. Input Port

D. Output Port :

The output port contains four input and one output channel. At a time only one input channel is granting access to output channel and once it gained access it must keep until complete packet have been transmitted. Receiving of end flit indicate packet completion. At the end merging is done with the help of merge component in which it merge input channel to get output on the output channel.

Access control circuits and mutex component handles the arbitration. Each input channel has its own control circuit. As soon as control circuit receives a header request it request to mutex for output port access. If mutex grants control circuit request then header flit is passed to the output port through that control circuit. Mutex is not release its control before receiving end flit and other inputs will wait for the mutex access.

Table I. Routing Directions with Encoding Bits.

Direction	North	East	South	West	Local
Direction encoding	001	010	011	100	101

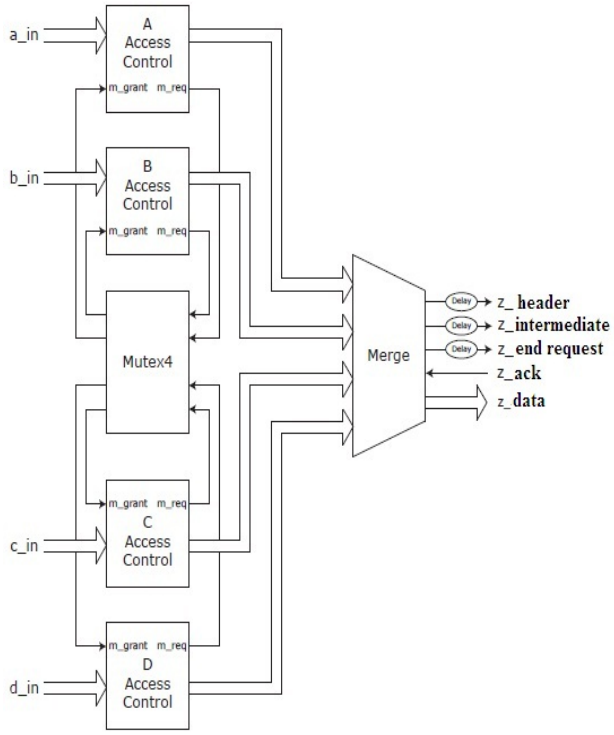

Figure 4. Output Port

III. RESULTS

The proposed asynchronous router design is developed by using 2D-Mesh Topology and uses XY routing algorithm and wormhole switching techniques on VHDL platform.

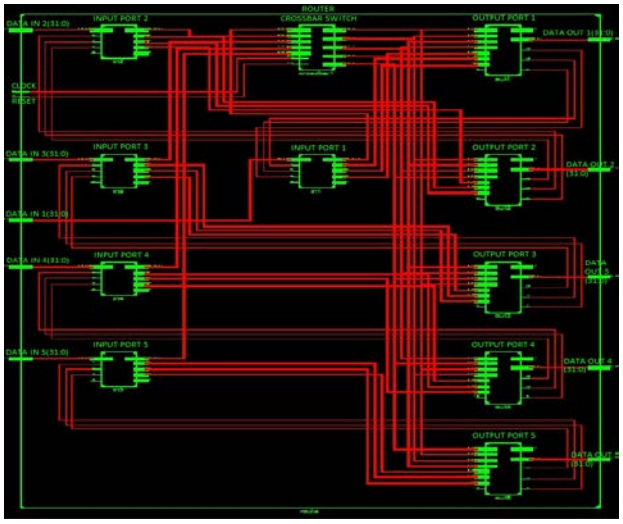

Figure 6. Router 5x5 RTL schematic

The design is implemented on Xilinx 13.1 for the Spartan 3E XC3S500E FPGA. The proposed router operates at a frequency of 226.09MHz and data arrival time 5.84ns in FPGA and utilizes 141 slices.

A. RTL Schematic

To test routing test bench is taken in which alternately entering some packets and their behaviour studied in output port. The tests were conducted by entering four 32 bits packets at the input port and different direction (3 bits) taken in header flit.

All the possibilities are studied by simulation test. The RTL schematic of proposed router is shown in figure 6.

B. Hardware Utilization

The report shows that the proposed router improves the efficiency of Network on Chip. The proposed router compared with previous published work as tabulated in table II and it is seen that proposed router uses 141 slices which is less than other.

Table II.comparison of the resource utilization

Router Design	Platform	Area on FPGA (slices)
Proposed Work	Spartan 3E	141
[4]	Spartan 3E	266
[8]	Spartan 3E	412

IV. CONCLUSION

In this paper we proposed a low area asynchronous NOC router and by using statistical data we proved that proposed design uses less area compared to published work [4]. The proposed router uses XY routing algorithm and wormhole switching techniques using 2D mesh topology. When number of packets is more that time wormhole switching technique provide low latency and XY routing gave conformation for deadlock.

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