Design of Two Stage Operational Amplifier using Miller compensation in 100 nm CMOS Technology

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Abstract- The paper represents a design procedure of basic two stage CMOS operational amplifier using Miller compensation technique. The LtSpice simulation tool is used to present system result at low capacitive load with different characteristics. The Miller capacitor creates an undesirable right-half-plane (RHP) zero due a non inverting feedforward signal path is induced in the input of the second stage towards its output, which can be eliminated by using voltage buffer. My work shows the two stage amplifier with Miller compensation technique, simulated using LtSpice simulation tool for 100 nm CMOS technology process. When a 2-pF capacitive load is drive, the amplifier achieves voltage gain approximate 20 % more with exactly double gain bandwidth (GBW) which shows phase margin of 123.24°, and gain margin is 78.4dB, with dissipating power value of 350 µW at 2 V, supply voltage.

Keywords- CMOS, Compensation, Gain bandwidth, LtSpice, Miller Compensation, Output swing, Poles, RHP, Slew Rate, Two Stage Op-amp, Voltage Gain, Zero.

I. INTRODUCTION

The trend towards low voltage low power silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry[2]. Op-amps are built with different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks[1]. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits. Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc . Generally an Operational Amplifier is a 3-terminal device[5]. It consists mainly of an Inverting input denoted by a negative sign, ("-") and the other a Non-inverting input denoted by a positive sign ("+") in the symbol for op-amp. Both these inputs are very high impedance[3]. The output signal of an Operational Amplifier is the magnified difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier. An operational amplifier is a DC-coupled differential input voltage amplifier with an rather high gain[10]. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. For most general applications of an op-amp a negative feedback is used to control the large voltage gain[9]. The negative feedback also largely determines the magnitude of its output ("closed- loop") voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration [12]. An ideal Opamp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero).to put it simply the op- amp is one type of differential amplifier. This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp[4]. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system[10].

A basic op-amp consists of 4 main blocks:

a. Current Mirror

b. Differential Amplifier

c. Level shift, differential to single ended gain stage d. Output buffer

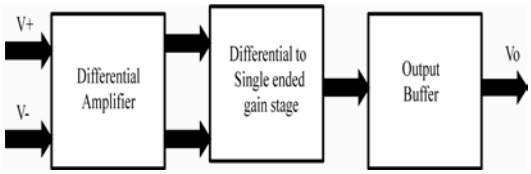

Fig.1 General Structure of op-amp

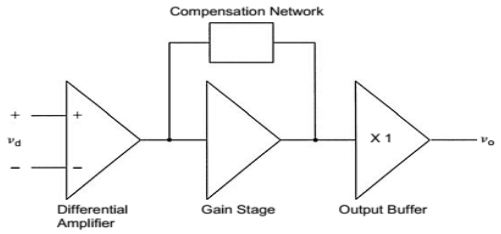

Fig. 2 Functional Block Diagram of two stage op-amp

In above figures, the first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The second stage performs Level shifting, added gain and differential to single ended converter. The third block is the output buffer[8]. The output buffer may sometimes be omitted to form a high output resistance un-buffered op-amp often referred to as Operational trans conductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers)[1].

CMOS Operational Amplifier is one of the most versatile and important building blocks in analog circuit design. Based upon the value of their output resistance they are being classified into two categories:

1. Unbuffered Operational Amplifier: These are Operational Transconductance Amplifiers (OTA), which have high output resistance.

2. Buffered Operational Amplifier: These are Voltage Operational Amplifiers, which have low output resistance. Operational amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer – function is practically independent of the gain of the op-amp. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement negative feedback concept[2].

CMOS op-amps are very similar in architecture to their bipolar counterparts.

The Two Stage op-amp shown in fig 3 is widely used because of its structure and robustness. Our aim is to create the physical design and fabricate a low power Op-amp .An ideal op-amp having a single ended out is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. In a real op-amp however these characters cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications[15]. With the introduction of each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down.

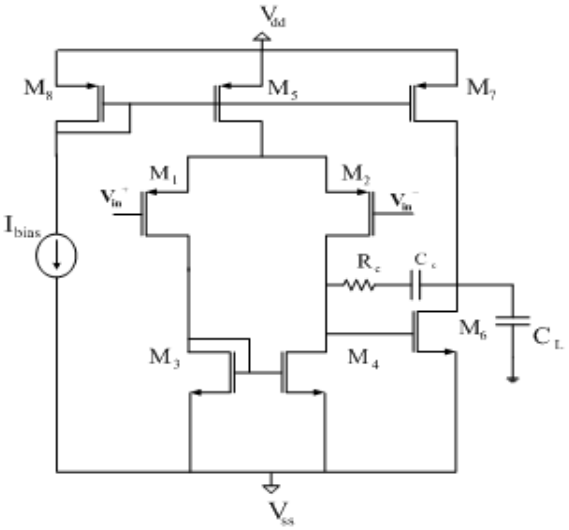

Fig. 3 A Typical Two Stage Amplifier

II. DESIGNING OF TWO STAGE CMOS OPAMP

The designed op-amp has been simulated to find the different characteristics of the designed op-amp. The total design performed in LtSpice . Different test benches have been created and extracted design has been then simulated with the parasitic values and compared with the schematic. Later in the chapter we also have compared the obtained parameters of the device through simulation to the specifications for the device.

Design Issues

Typical specs	Design factors
• DC Gain (Av)	Frequency Response
• Unity Gain Bandwidth	Phase Margin
• Power Dissipation	Load Capacitance

Steps in designing a CMOS OP AMP:

- Choosing or creating the basic structure of the op amp.
- Decide on a suitable configuration determination of the type of compensation needed for meeting the specification Selection of the dc currents and transistor sizes.
- Physical implementation of the design.
- Fabrication
- Measurement

The design process involves the two major steps, the first is the conception of design ,and second one is optimization of design . The conception of the design has been accomplished by proposing an architecture to meet the given specifications. This step is normally done by using hand calculations in order to maintain the intuitive view point necessary for choices that must be made. Second step is to take the "first-cut" design and verify and optimize it. This is normally done by using Computer simulation and can include such influences as environmental or process variations.

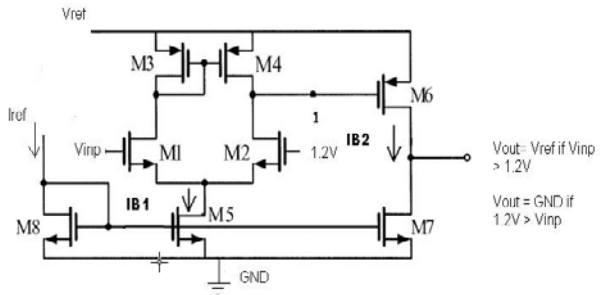

Fig.4 Unbuffered two stage CMOS OPAMP

Table.1 Specifications for a Typical Unbuffered CMOS Op-Amp

Specifications	Value
Supply voltage	±2.5 V ±10%
Supply Current	100 µA
Gain	=>70 dB
Gain Bandwidth	=>5MHz
Settling Time	<= 1 µsec
CMRR	=>60 dB
PSRR	=>60 dB

Compensation of Op-amps:

Objective of compensation is to achieve stable operation when negative feedback is applied around the op amp.

Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.

   • Miller capacitor only • Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.

   • Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero[5].

2. Self compensating - Load capacitor compensates the op amp (later).

3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

III. PROPOSED SCHEMATIC OF OP-AMP AND SIMULATION RESULTS

Table 2. Channel Width For MOS Transistor Designed For 100 nm Technology Op-amp.

MOS Transistor	Aspect Ratio (W/L)	Channel width (nm)
M1	3	300
M2	3	300
M3	3	300
M4	3	300
M5	3	300
M6	2.35	235
M7	2.35	235
M8	2.35	235

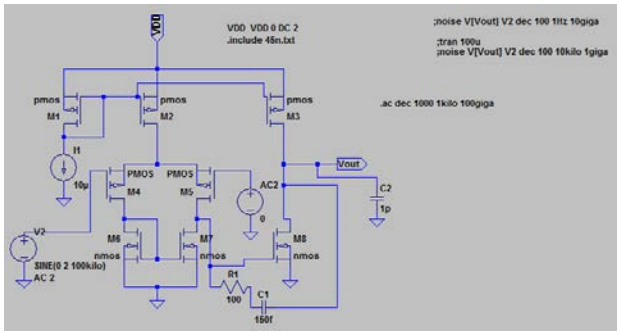

Fig.5 Proposed circuit with two stage op-amp with compensation

From above fig we can found that the gain bandwidth is 34.67 MHz (the unity gain frequency, 0dB) The Corresponding phase margin for a 1pF load we can find out as 123.23°, and gain margin is 74.4dB.

Table 3. Comparison of two stage opamp

Ref.	[2]	This Work
Technology	50nm	100nm
Supply Voltage	2	2
Load Capacitance	100fF	1pf
Gain margin(dB)	62.8	78.4
Phase Margin (Degree)	77.667	123.24
Power dissipation	500µW	350 µW

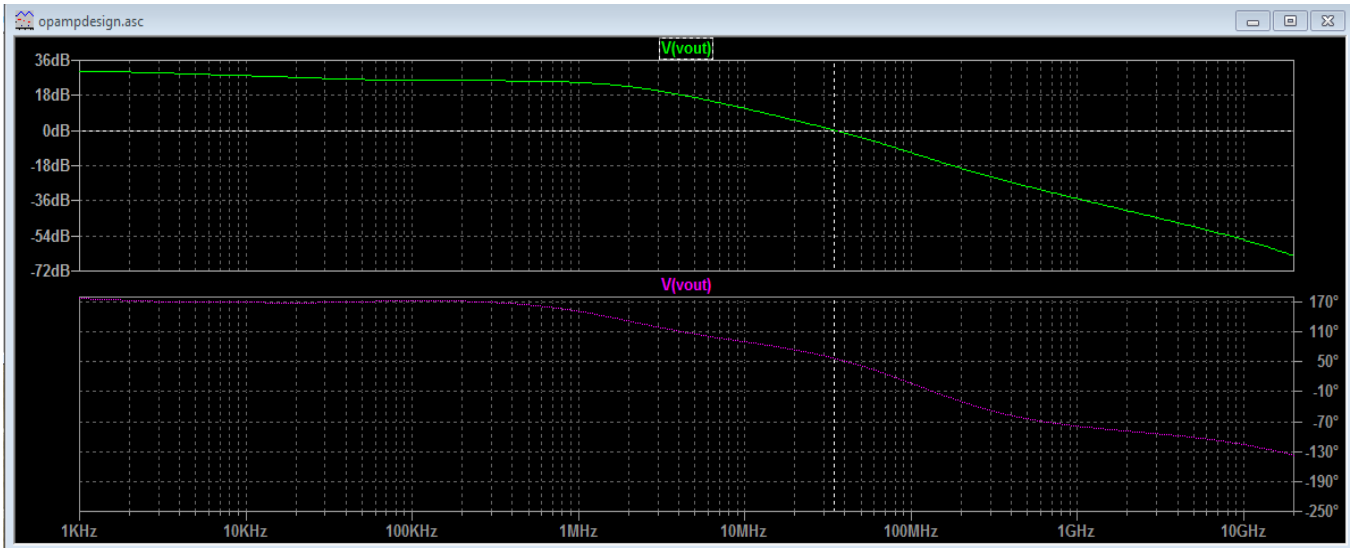

Fig.6 Frequency response simulation result

IV. CONCLUSION

The objective of this work was to implement the full custom design of low voltage and low power operational amplifier**.** In this paper a well-defined method for the design of a two-stage CMOS operational amplifier has been presented. The design has been made through the scaling of device parameters, as it is known that, by maintaining the scaling factor to a minimum value can reduce the current, power consumption and area as well. Now an OPAMP has been described in its negative feedback Configuration, as it can provide a moderate gain as compare to the open loop, but the problem is this case is the stability, which can be reduced by using the compensation techniques. In this thesis Miller Compensation technique is implemented, where this simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor across the high-gain stage.

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