Design of an Operational Amplifier for Sensor Interface

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Abstract: The aim of this paper is to design a high-gain, high PSRR, low power op-amp for use as a universal pre-amplifier in a generic sensor interface. Sensors are omni-presents these days, employed to measure a plethora of variables in a multitude of applications. So this paper is based on cascading two high-gain differential stages to form a composite front-end gain stages for enhancing gain as well as CMRR with the consumption of low power. Proposed amplifier which is presented here operates with 2.5V power supply at 0.25 micron (i.e ,250 nm) technology, whose input is depending on bias current. To reduce overall power consumption of the system voltage has been scaled down. The main aim is to increase gain, reduce power dissipation, increased CMRR, and low offset. This two stage CMOS op-amp provides a gain of 64 dB and a -3db bandwidth of 22 kHz and UGB of 12 MHz for a load considered of 2 pF compensation capacitor and 10 pF load capacitor. It has a high CMRR of 80 dB and an output slew rate of 22 V/ µs. The power consumption for the op-amp is 0.775mW as per required for sensor interface.

Key words: Op-amp (operational amplifier), Unity Gain Bandwidth (UGB), Gain, Phase margin, Input Common-Mode Range (ICMR), Power Supply Rejection Ratio (PSRR), Slew Rate (SR).

I. INTRODUCTION

We are witnessing the dominance of microelectronics (VLSI) in every sphere of Electronics forming the backbone of modern electronics industries in mobile communications, computers, state of processors etc. As the ever increasing advancement in the field of technology the demand for automation is also increased exponentially. Sensors are the main device used in the area of automation and sensors are ubiquitous these days, employed in a many applications like health-care monitoring, weather and environment monitoring, agriculture sensing, automobiles, structure monitoring of building and many more. In addition to the sensor, a typical measurement system consists of electronics to perform data processing and signal conditioning which impose demanding requirements on the electronics interface between the sensor and the processing system. Because the sensor produce low level signals, therefore pre-amplification of the signals is necessary for further conditioning and processing. Operational Amplifiers thus plays an important role in sensor interface for instance, the autonulling bridge for gas sensors and chemical sensors or the well-known Wheatstone bridge for pressure sensor etc, often require amplifiers having intrinsically high CMRR, low offset, and low noise for floating differential sensing function.

There are several approaches to deal with the design challenges. First the amplifiers in sensors can be designed using auto-zeroing technique [1], but the drawback in that it may be valid for a certain temperature range or constrained conditions due to the added sensitivity of the circuit. Alternatively, the correlated double sampling technique [2], chopper stabilization technique [3]-[4] or baseline subtraction techniques [5] so as to increase CMRR and/or to reduce both the low frequency flicker noise and the offset in CMOS sensor circuit.

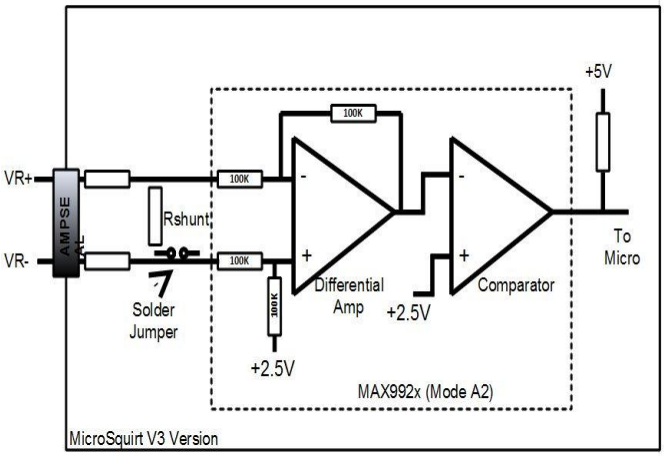

Figure 1: Block diagram of the new sensor interface circuit

However, the key disadvantages of these techniques can be observed as (i) the clock circuit coupling is unavoidable interference into sensitive analog circuitries adding design concern of power supply rejection ratio (PSRR). (ii) the generation of residual nonlinear switching errors arising from mismatch or inadequate compensation of switches and (iii) the use of high-order continuous-time filter for rejection of unwanted spectral components. All these techniques increasing the silicon overhead indirectly. As a result, turning to increase the cost of overall architecture. Therefore, for low cost solution as one of the focuses, the circuit architecture and device matching are considered as two critical issues because they shows the instrumentation-based performance in terms of gain, CMRR and offset

parameters. Therefore, this paper presents the design of a compact and economical operational amplifier for use as a universal pre-amplifier in a generic sensor interface. Here is a block diagram of the new sensor interface circuit shown in figure-1, which shows that how the operational amplifiers can be used as pre-amplifying circuit for sensor interface.

II. PROPOSED AMPLIFIER

Designing high-performance analog circuit is become very challenging task with the persistence trend towards reduced supply voltages. The main bottleneck in analog circuit is the designing of operational-amplifier. At large supple voltages, there is a trade-off among speed, power and gain. The main characteristics under consideration are high gain, high slew rate, low offset voltage, high output swing. Performance of any circuit depends upon these characteristics. At reduced supply voltages, output swing becomes an important parameter. Due to the consistent efforts the op-amp architecture have evolved from a simple Telescopic architecture to the high performance cascading architecture involving less power consumption, low noise, high gain etc. The objective of our work is to design the procedure for an operational amplifier made by cascading two high gain differential stages and evaluate the performance parameter as required for the sensor interface.

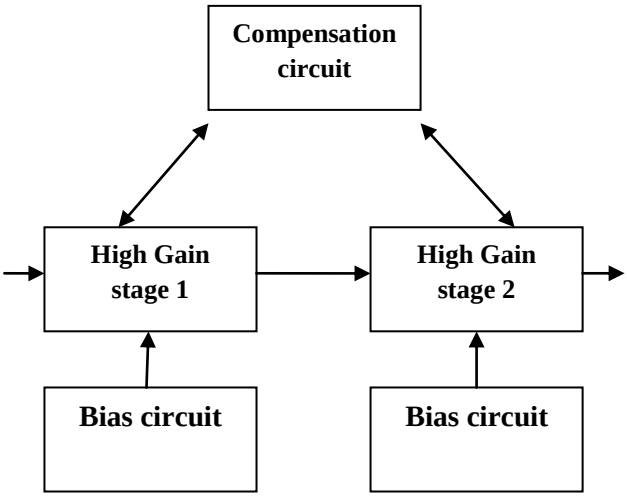

Figure 2: Two stage CMOS op-amp

Typically, an op-amp requires sufficiently high gain so that the closed loop transfer function is practically independent of the gain [6]. Fig. 2 shows the general two-stage CMOS op-amp block diagram. The circuit consists of two differential inputs followed by a common source at the second stage. The differential inputs provide the initial gain, while the second stage increases the gain by an order of magnitude and maximizes the output swing. The compensation is one is one method to increase the phase margin [7] and is required for stable closed-loop performance [8]. There are a few approaches to frequency compensation techniques to eliminate the effect of a right-half plane of zero, which can cause stability issues. These approaches includes pole-splitting, a self-compensation capacitor and the inclusion of a transconductance stage to cancel the feed forward signal [9]. The compensation capacitor that is connected between the input and output nodes of the second stage cause the pole associated with them to split apart. This generates a non-dominant or dominant pole feed forward path that produces the right half plane.

For a cascaded two stage op-amp, the simplest compensation technique is to connect a capacitor across the high gain stage. This results in the pole splitting phenomena which improves the closed-loop stability significantly. However, due to the feed-forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created. In theory, such a zero can be nullified if the compensation capacitor is connected in conjunction with either a nullifying resistor or a common-gate buffer (fig. 3)

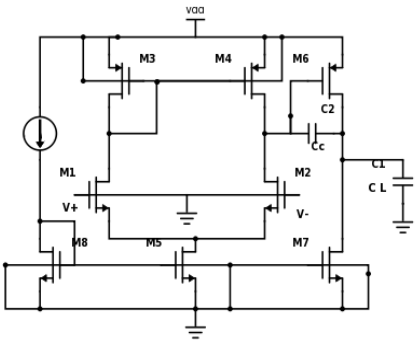

Figure 3: Schematic Diagram of Proposed Operational Amplifier

The design procedures of the former type ofop-amp have been proposed. However since the previous procedure employs pole-zero cancellation, they are sensitive to process and temperature variation. Although the implementation of the op-amp with buffer compensation has been reported and the design strategy has been proposed, the complete design procedure for the op-amp of this type has been presented. In this paper, we attempt to fill the gap by proposing the design procedure for the CMOS op-amp with Miller compensation in conjunction with the current buffer. It should be pointed out that unlike the strategy proposed previously, which result in the op-amp with a pair of complex conjugate poles and one finite zeros, the proposed design procedure is based on the strategy which would theoretically result in the op-amp with only one real non-dominant pole. The simplified schematic diagram of proposed operational amplifier is shown in figure 3.

III. PARAMETERS TO BE MEASURED:

3.1 Gain (dB) :

Operational amplifiers basic function is to amplify the input signal and the higher is its open loop gain, the better as in many applications they are used with a feedback loop, so ideal op-amps are characterized by a gain of infinity. For practical op-amps, the voltage gain is finite. Typical values for low frequencies and small signals are A = 102 – 105, corresponding to 20-100 dB gain. This is the open loop differential gain measured as a function of frequency [10].

3.2 Common Mode Rejection Ratio (CMRR):

The common mode rejection ratio (CMRR) of an operational amplifier is the ratio between the differential gain and the common mode gain. Where A_D is [10]

$$A_D = \frac{V_O}{V_A - V_B}$$

The CMRR is defined as AD/AC or (in logarithmic units)

CMRR= $20 \log_{10}(A_D/A_C)$, In decibels

Typical CMRR values for CMOS amplifiers are in the range 60 to 80 dB. The CMRR is a parameter that measures that how much the op-amp can suppress noise, and hence a large CMRR is an important requirement.

3.3 Power Supply Rejection Ratio (PSRR):

We apply a small signal in series with the positive or the negative power supply we obtain a corresponding signal at the output with a given amplification .The ratio between the differential gain and the power supply gain leads to two PSRRs. These are two merit factors showing the ability of the op-amp to reject spur signals coming from the power supply [10].

Having a good PSRR is an important merit. Unfortunately, especially at high frequencies, the PSRR achieved is quite poor .A typical value of PSRR is 60dB at low frequencies that decreases to 20-40dB at high frequencies**.**

PSRR=20 log (Vout/Vin) , in decibels

3.4 Offset Voltage (Vos):

The output of an amplifier is supposed to be independent from common mode inputs applied at the input terminals and is supposed to be zero when the voltage difference between the inverting and non-inverting inputs is said to be zero or can say when both inputs are equal [10].

For an ideal op-amp, if $V_a = V_b$ (which is easily obtained by short circuiting both the input terminals) then $V_o = 0$. In real devices, this is not exactly the scenario, and a voltage $V_{0,\ off} \neq 0$ will occur at the output for shorted input voltages. Since $V_{0,\ off}$ is directly proportional to the gain of the amplifier, the effect can be more conveniently described in terms of the input offset voltage $V_{in,off}$, defined as the differential input voltage needed to restore $V_o = 0$ in the real devices. For MOS op-amps mostly $V_{in,off}$ is about 5- 15mV.

3.5 Input Common Mode Range (ICMR) :

This is basically the voltage range that we can use at input terminal without producing a significant degradation and reduction in op-amp performance. Since the typical input stage of an op-amp is a differential pair, the voltage required for the proper operation of the current source and the input transistors limit the input swing. A large input common mode range is very important when the op-amp is used in the unity gain configuration. In this case the input must follow the output. The op-amp must possess good ICMR for desirable performance [10].

3.6 Output Voltage Swing :

It is the maximum swing at the output terminal without producing a significant degradation of op-amp performance [10].

Typically it ranges between 60% to 80% of (V_{DD}-V_{SS}). Within the output swing range the response of the op-amp should conform to given specifications and in particular the harmonic distortion should remain below the required level.

3.7Unity Gain Bandwidth:

Because of stray capacitances and finite carrier motilities, the gain A_{DC} decreases at high frequencies. It is usual to describe this effect in terms of the unity gain bandwidth, that is the frequency f_T at which $|A_{DC}(f_T)| = 1$. For MOS op-amps, f_T is usually in the range of 1-10 MHz. The frequency at which the gain becomes *0dB* is called unity gain frequency f_T . Therefore, f_T is also known as the gain-bandwidth product, GBW [10].

3.8 Slew Rate (SR) :

Slew rate of an Op-amp is defined as the maximum rate of change of output for the small change in input [10].

$$SR = \left[\frac{dVo}{dt}\right]_{\max}$$

This is the maximum achievable time derivative of the output voltage. It is measured using the op-amp in the open loop or the unity gain configuration. A large input step voltage fully imbalances the input differential stage and brings the op-amp output response into the slewing conditions .The positive slew rate can be different from the negative slew rate, depending on the specific design. Typical values ranges between 40 and 80V/ µs.

3.9 Phase Margin (PM):

This is the phase shift of the small –signal differential gain measured at the unity gain frequency. In order to ensure stability when using the unity gain configuration it is necessary to achieve a phase margin better than 60 degree. A lower phase margin (like 45 degree) will cause ringing in the output response. However, for integrated implementation it is not strictly necessary to ensure absolute stability [10].

3.10 Power Consumption:

This is the power consumed under standby conditions. The power used in the presence of a large signal can significantly exceed the one required in the quiescent conditions. Moreover, the consumed power depends on the speed specifications. Typically, higher bandwidth leads to higher power consumption. Low power operation is a very important quality factor: batteries that should supply the system for hours or days power more and more electronic systems. Thus, a key design task to achieve low power consumption for required speed [10].

IV. DESIGN METHODOLOGY:

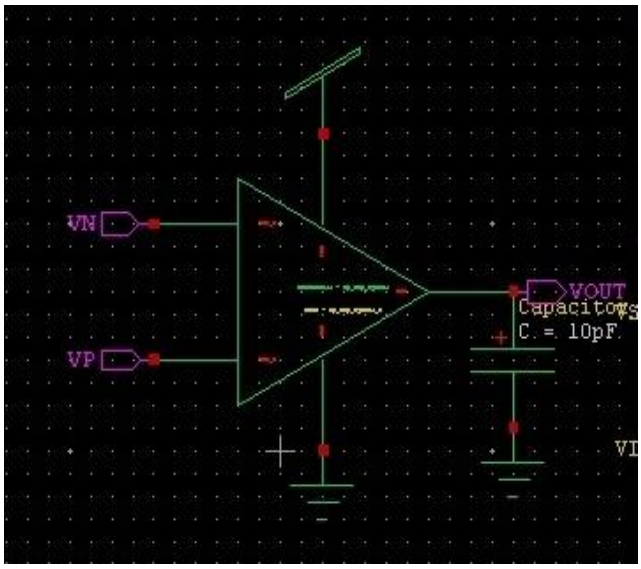

Figure 4 : Symbolic representation of FCOA

4.1 Design Specifications:

TABLE 1: DESIGN SPECIFICATIONS

PARAMETERS	VALUE
DC GAIN	80dB
GBW	20 MHz
PHASE MARGIN	$\geq 60^\circ$
SLEW RATE	$\geq 20\ V/\mu s$
C_L	10pF
V_{DD}	2.5 V
V_{SS}	0 V
ICMR(+)	2.1 V
ICMR(-)	0.9V
POWER DISS.	<5 mW
CMRR	100 dB
OUTPUT SWING	**0** V to 2.5V

4.2 Design Consideration:

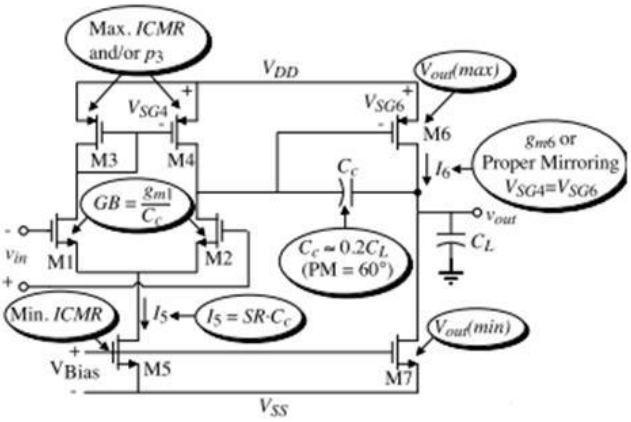

Figure 5: Two stage amplifier

Steps Involved:

1. The design procedure begins by choosing a device length to be used through the circuit.
2. The minimum value for the compensation capacitor C_c should be 0.22 times more than C_L to get phase margin 60 degree.
3. Based on the slew rate requirements the value of tail current I_5 is determined.
4. The aspect ratio of M_3 can be determined by positive input common mode ratio range by using the equation-3.
5. Aspect ratio of M_1 can be determined through transconductance g_m by using equation-5.
6. To calculate the saturation voltage of transistor M_5 negative input common mode ratio range is used by equation-7.
7. For reasonable phase margin, the value of g_{m6} is approximately 10 times the input stage transconductance g_{m1}. To achieve proper mirroring of

the first stage current mirror load of M_3 and M_4 requires $V_{GS4} = V_{GS6}$. By V_{GS6} we can get the aspect ratio of M_6.

8. The device size of M_7 can be determined from the I_6 current flowing through M_6 and balanced equation.

4.3 Design Equation:

In this section we will outline the design methodology adopted to design the two-stage amplifier with the regulated current source load. The discussion will draw on the analysis of the design goals here:

1. Very high gain
2. Low noise
3. GBW configurable for high-speed
4. PSRR as high as possible
5. CMRR as high as possible

Here we outline one of the possible design sequences for designing the required amplifier. A number of alternative sequences can be adopted depending upon the design goals and constraints on performance specifications. Here, we will list the steps to design an amplifier for a required gain A_{total} within a given power budget (implying a constraint on the bias current I_0, since bias voltage is fixed), and a given bandwidth GBW_{total} with a fixed load capacitance C_L. The main design steps of an op-amp are as follows:

Step-1: Choose I_5 to be as a value which will be decided by slew rate and power dissipation.

Step-2: From the desired phase margin, choose the minimum value for Cc, i.e. for a 60° phase margin use the following relationship. This assumes that z ≥10 GB

$$C_C \geq 0.22 C_L \tag{1}$$

Step-3: We Determine the minimum value for the "tail current" (I_5) from

$$I_5 = C_c \times SR \tag{2}$$

Step-4: The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ is

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2I_3}{\mu_n C_{OX}\left(V_{DD} - ICMR + (-V_{t3(MAX)}) + V_{tMIN}\right)^2} \tag{3}$$

Step-5: Requirements for the Trans-conductance of the input transistors can be determined from knowledge of C_c and GBW. The Trans-conductance g_{m1} can be calculated using the following equation:

$$g_{m1} = GBP \times C_C \times 2\pi \tag{4}$$

Step-6: The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below:

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_m^2}{\mu_n C_{OX} I_{D5}} \tag{5}$$

Step-7: Using the negative ICMR equation, calculate the saturation voltage of M5 (VDS5) by the following relationship:

$$V_{Dsat} \geq ICMR(-) - \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{t1_{\max}} \tag{6}$$

Step-8: With V_{Dsat} determined $(W/L)_5$ can be calculated by the following equation:

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{D5}}{\mu_n C_{OX}\left(V_{DSAT}\right)^2} \tag{7}$$

At this stage the design of first stage op amp is complete.

Step-9: Next the trans-conductance g_{m4} and g_{m6} can be determined by the following relationship:

$$g_{m6} \geq 10 g_{m1}$$
$$g_{m4} = \sqrt{\mu_p c_{ox}.(\mathrm{W/L})_4.2I_D} \tag{8}$$

Step-10: Then to design of M_6 we can write $V_{SG4} = V_{SG6}$:

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{g_{m4}}\left(\frac{W}{L}\right)_4 \tag{9}$$

Step-11: Calculate $I_{7:}$

$$I_{D7} = SR(C_C + C_L) \tag{10}$$

Step-12: Design S_7 i.e $(W/L)_7$ to achieve the desired current ratios between I5 and I7:

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5}\left(\frac{W}{L}\right)_5 \tag{11}$$

4.4 Prototype Design:

The design has been done using the 0.25 µm 2.5V standard CMOS process by following the design methodology developed above. Let's start the calculation according to our designing equation:

STEP 1: From the desired phase margin, choose the minimum value for Cc, i.e. for a 60° phase margin use the following relationship.

$$C_C \geq 0.22 C_L \tag{12}$$
$$C_C \geq 0.22 * 10\,pf$$
$$C_C \approx 2\,pf$$

STEP 2: We Determine the minimum value for the "tail current" (I_5) from

$$I_{D5} = C_C \times SR \quad (13)$$
$$I_5 = 20V / \mu\text{sec} * 2pf$$
$$I_5 = I_0 = 40\mu A$$

STEP 3: Requirements for the Trans-conductance of the input transistors can be determined from knowledge of C_c and GBW. The Trans-conductance g_{m1} can be calculated using the following equation:

$$g_{m1} = GBP \times C_C \times 2\pi \quad (14)$$
$$g_{m1} = 20MHz \times 2pf \times 2\pi$$
$$g_{m1} = 252$$

STEP 4: The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below:

$$(\frac{W}{L})_{1,2} = \frac{g_m^2}{\mu_n C_{OX} I_{D5}} \quad (15)$$
$$(\frac{W}{L})_{1,2} = \frac{252^2}{2 \times 20 \times 220}$$
$$(\frac{W}{L})_{1,2} \approx 8$$

STEP 5: The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ is

$$(\frac{W}{L})_{3,4} = \frac{2I_3}{\mu_n C_{OX}(V_{DD} - ICMR + (-V_{t3(MAX)}) + V_{tMIN})^2} \quad (16)$$
$$(\frac{W}{L})_{3,4} = \frac{2 \times 20}{70(2.5 - 2.2 - 0.5 + 0.4)^2}$$
$$(\frac{W}{L})_{3,4} \approx 15$$

STEP 6: Using the negative ICMR equation, calculate the saturation voltage of M5 (VDS5) by the following relationship:

$$V_{Dsat} \geq ICMR(-) - \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{t1_{\max}} \quad (17)$$
$$V_{Dsat} \geq 0.9 - \sqrt{\frac{2 \times 20}{220 \times 5}} - 0.589$$
$$V_{Dsat} \geq 0.12v$$

STEP 7: With V_{Dsat} determined $(W/L)_5$ can be calculated by the following equation:

$$(\frac{W}{L})_5 = \frac{2I_{D5}}{\mu_n C_{OX}(V_{DSAT})^2} \quad (18)$$
$$(\frac{W}{L})_5 = \frac{2 \times 20}{220 \times (0.12)^2}$$
$$(\frac{W}{L})_{5,8} \approx 12$$

STEP 8: Next the trans-conductance g_{m6} and g_{m4} can be determined by the following relationship:

$$g_{m6} = 2.2 \times g_{m1} \quad (19)$$
$$g_{m4} = \sqrt{\mu_p c_{ox}.(W/L)_4.2I_D}$$
$$g_{m4} \approx 205$$

STEP 9: Then to design of M6 we can write VSG4 = VSG6:

$$(\frac{W}{L})_6 = \frac{g_{m6}}{g_{m4}}(\frac{W}{L})_4 \quad (20)$$
$$(\frac{W}{L})_6 = \frac{2520}{205} \times 15$$
$$(\frac{W}{L})_6 = 184$$

STEP 10: Design S_7 i.e $(W/L)_7$ to achieve the desired current ratios between I_5 and I_7:

$$(\frac{W}{L})_7 = \frac{I_7}{I_5}(\frac{W}{L})_5 \quad (21)$$
$$(\frac{W}{L})_7 = \frac{245}{40} \times 12$$
$$(\frac{W}{L})_7 \approx 74$$

Schematic configuration of two stage OPAMP with 250nm technology is shown in figure and aspect ratio's of 250 nm technology op-amp their channel width for cmos transistor are tabulated below.

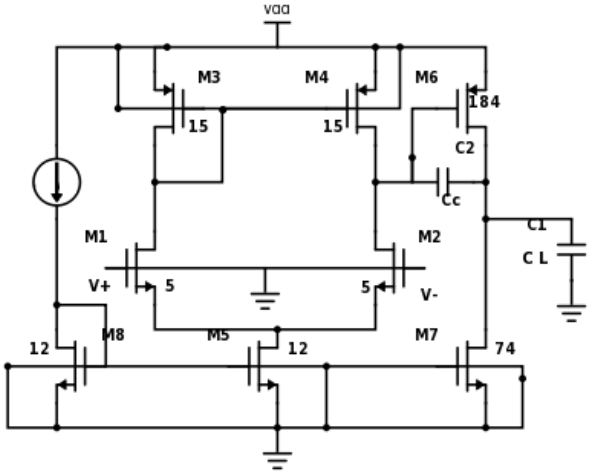

Figure 6: Designing of two stage op-amp

The summary of the aspect ratio will be mentioned in the tabulated format below:

Table 2: W/L Ratios Of Different Mosfet's

Aspect ratio Transistor	$S_i = (W_i/L_i)$	Ratio
M1	2.5µm/0.5µm	5
M2	2.5µm/0.5µm	5
M3	7.5µm/0.5µm	15
M4	7.5µm/0.5µm	15
M,5	6.0µm/0.5µm	12
M6	92µm/0.5µm	184
M7	37µm/0.5µm	74
M8	6.0µm/0.5µm	12

V. SIMULATION RESULTS

In the design of Operational Amplifier, to determine the various characteristics, a number of analyses are performed. Some of the analyses are presented here. The analyses are performed on simple two-stage Op-Amp designed in 0.25µm CMOS technology.

A schematic diagram of two-stage Op-Amp schematic diagram is shown in fig 7.

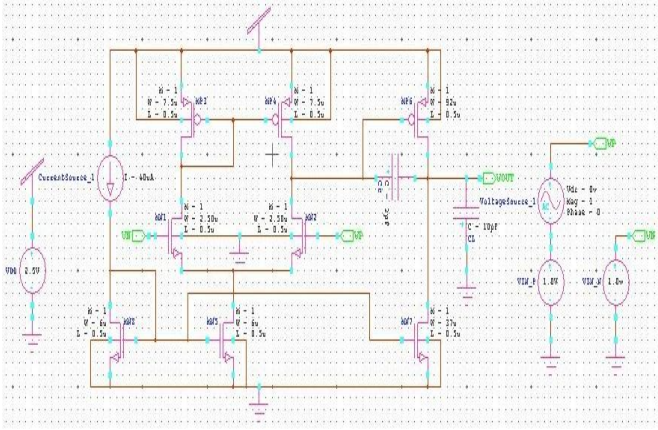

Figure 7 Schematic diagram with aspect ratios

Table 2 shows the transistor sizes used for two-stage Op-Amp. Here the minimum length is 0.5µm which is greater than 0.25µm due to allowance of fabrication process.

5.1 DC analysis

DC analysis is used to determine the quiescent point of the device operation. In two-stage Op-Amp, all the transistors must work in saturation. To determine that all transistors are operating in saturation or not for the entire input common mode range, DC analysis is performed. The DC analysis of Op-Amp also gives the information about the characteristic of Op-Amp i.e. trans-conductance, threshold voltage, current gain value etc. Fig 8 shows the set-up for DC analysis of Two- Stage Op-Amp. The minimum common mode range input supply of 1V is applied to both the input terminals.

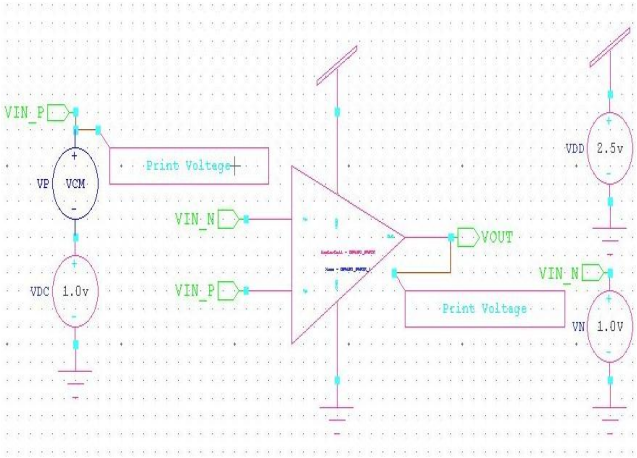

Figure.8: Set-up for DC analysis of Two-Stage Op-Amp

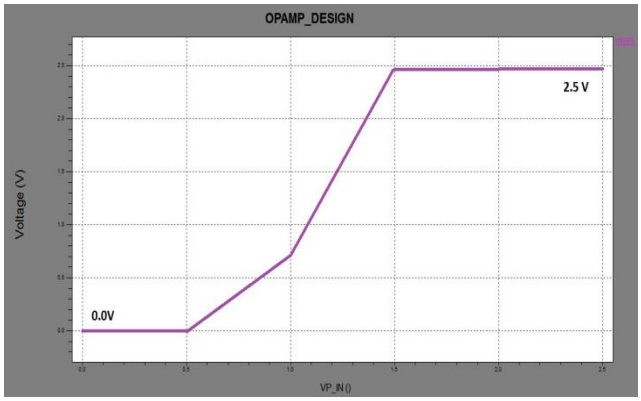

Figure 9: ICMR Measurement

5.2 AC analysis

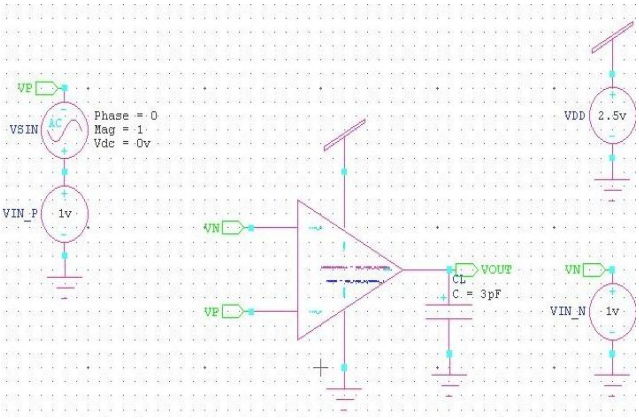

Figure 10: Set-up for AC analysis of Two-Stage Op-Amp

Ac analysis is used to determine the open-loop gain, gain-bandwidth, 3-db cutoff frequency, common mode rejection ratio, power supply rejection ratio and phase margin of two-stage Op-Amp. The AC analysis gives the frequency response of the two-stage Op-Amp. Ac analysis is performed by connecting an AC source to the one of the input terminal of with the minimum dc value required to keep the transistors in the saturation region.

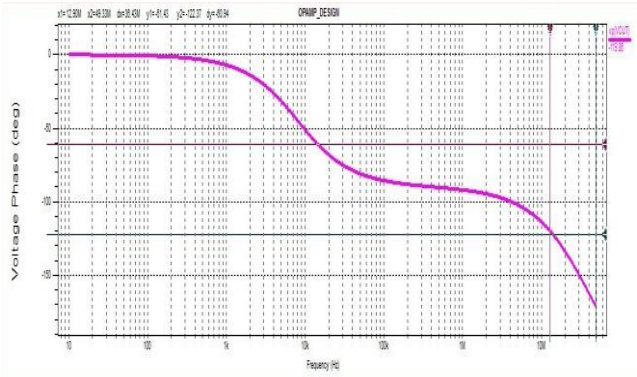

Figure 11: Phase-Frequency plot for Two-Stage Op-Amp

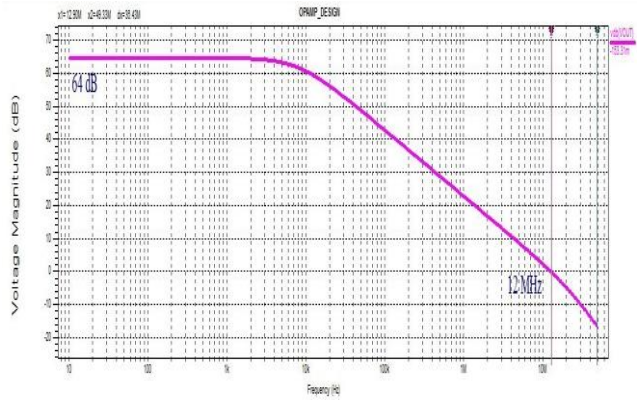

Figure 12: Gain –frequency plot for Two-Stage Op-Amp

5.3 Transient analysis

Transient analysis gives the timing details of the device. In the case of two-stage Op-Amp, transient analysis is used to determine settling time, slew rate, output voltage swing. The transient analysis shows how fast the system or device respond to the applied input. The transient response is performed by applying sinusoidal input and pulse input.

[A] Sinusoidal input:

Transient analysis of Op-Amp using sinusoidal input is used to determine the output voltage swing.

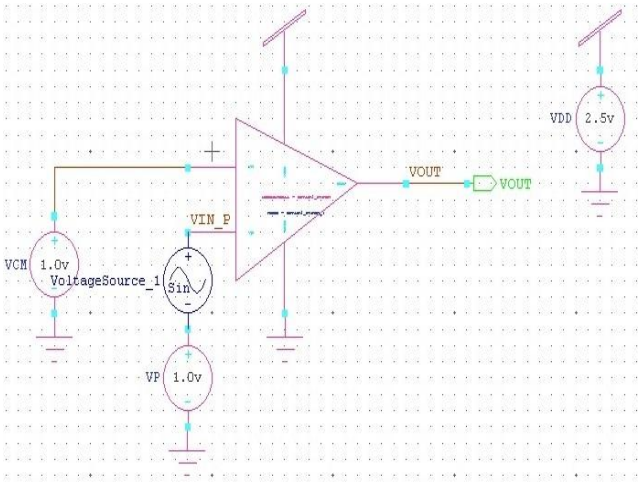

Figure 13: Set-up for Transient analysis with sinusoidal input

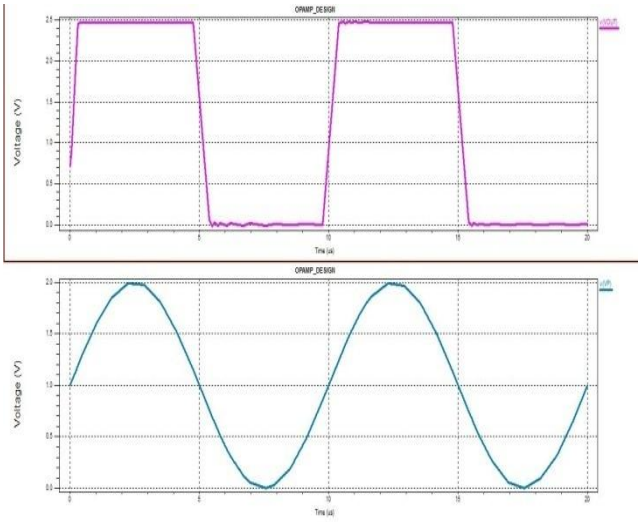

Figure 13: Transient Analysis Output for sinusoidal input

[B] Pulse input

Transient analysis of Op-Amp using Pulse input is used to determine the speed of Op-Amp. The slew rate (SR) and setting time of Op-Amp is obtained from the transient analysis using pulse input.

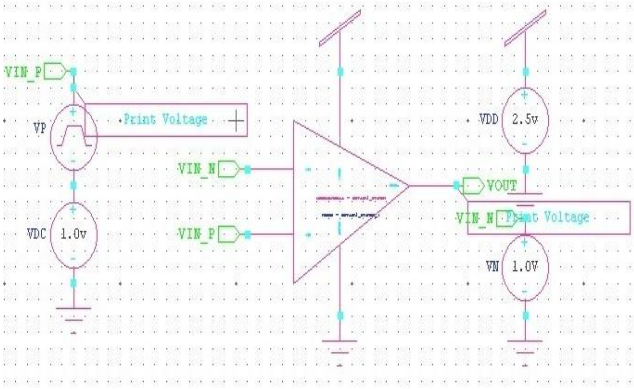

Figure 15: Set-up for Transient analysis with pulse input

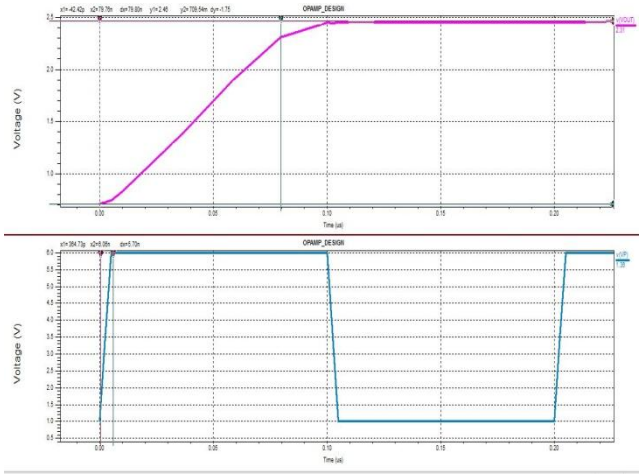

Figure 16: Transient analysis output with pulse input

Table 3: Summary of Results

S. No.	Parameter	Value
1.	Technology	0.25µm CMOS
2.	Supply Voltage	2.5V
3.	Current	328µA
4.	C_L	10pF
5.	C_C	2pF
6.	Open-loop gain	64.05 dB
7.	Gain-bandwidth	13 MHz
8.	3-dB cutoff frequency	20 kHz
9.	Phase Margin	64^o
10.	Slew Rate	22 V/µs
11.	Settling time	0.18µs
12.	Power consumption	0.75 µW
13.	CMRR	80dB

VI. CONCLUSION

This thesis presents the design of a very high-gain, low-power, low-noise op-amp intended for use in a generic sensor interface. The classical single stage amplifier was chosen as the starting point of the design because of its simplicity and robustness and a well defined design methodology. It was already conspicuous at the beginning of the project that it will be difficult, if not impossible, to achieve the >25 dB targeted value of gain with just the classical single-stage op-amp structure. Cascading another stage, this is a typical method of increasing the gain. As one of the main significance of the project, a step-by-step design methodology for the design of the complete two-stage op-amp utilizing the regulated current source for gain-boosting in the first stage was developed. Using the developed methodology an op-amp with 64 dB gain, 12 MHz GBW, was designed in a 0.25 µm 2.5 V CMOS process. Most of the performance parameters of the circuit are either better than or comparable to the state-of-art. The complete circuit consumes 80 µW power provided from a 2.5V supply. The op-amp thus designed is intended to be used as a pre-amplifier in a sensor interface. Consequently it will always be used in a feedback loop whose gain will be determined externally. Hence, the fact that the transient response of the op-amp in unity gain feedback shows a very small ripple is inconsequential.

VII. FUTURE SCOPE

The scope is open for the further detailed study of the circuit to ensure its stability as a buffer too. Alternative design approaches for designing this circuit constraining other parameters like noise (and not just gain) needs to be developed. Finally, it would be interesting to study the limits on the performance this circuit architecture can achieve with more advanced process technologies like 0.18µm. An analytical approach for the design of the regulated current source was developed to formulate the gain boost provided by it as well as the condition for ensuring stable operation.

The same circuit can operate in low-power mode with up to ten times less power consumption than the high-power mode. Operating in low-power mode, it consumes 69 µW of power and consequently has almost 10 time slower GBW.

VIII. REFERENCES

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