Design of Folded-Cascode Operational Amplifier for High Frequency Application

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Abstract : This paper deals with the detailed study of Folded-Cascode Op-Amp and its characterizing parameters is presented. Parameter measurements of a Folded-cascode Op-Amp are presented along with measurement set-ups in the tool and simulate results has been shown. The design procedure for a Single Stage Folded-Cascode Op-Amp is developed using design equations. A Folded-Cascode Op-Amp is designed in 0.25µm CMOS technology. The designed Op-Amp operates at 2.5V power supply i.e. V_{DD} is 2.5V. The designed Op-Amp achieves 30 dB of DC gain, 60^{o} phase margin, Gain Bandwidth of 60 MHz, 35V/µs of Slew rate with good Input Common Mode Range (ICMR). The design provides good swing and good Common Mode Rejection Ratio (CMRR) of 36 dB and Settling time of 105 ns. Without additional components, the high frequency response of the classical folded cascode operational amplifier is improved so as to be used in High Frequency application such as RF amplifier and video circuits.

Keywords : Op-Amp (Operational Amplifier), Folded-Cascode Operational Amplifier (FCOA), Unity Gain Bandwidth (UGB), Gain, Phase Margin, Input Common Mode Range (ICMR), Power Supply Rejection Ratio (PSRR), Slew Rate (SR), Common Mode Rejection Ratio (CMRR), RF(Radio Frequency), HF(High Frequency).

I. INTRODUCTION

We are experiencing the dominance of microelectronics (VLSI) in every sphere of electronics and communications forming the backbone of modern electronics industry in mobile communications, computers, state-of-art processors etc. All efforts eventually converge on decreasing the power consumption entailed by ever

shrinking size of the circuits enabling the portable gadgets. The most important characteristics of consideration are high PSRR, high CMRR, high slew rate and low offset voltage. The performance of any op-amp circuit depends upon these characteristics. At reduced supply voltages, the output swing becomes an important parameter of consideration.

Operational amplifier is an integral part of analog and mixed signal system. The design of high performance operational amplifier has always been one of the hotspots of analog integrated circuit design as its performance directly affects the overall performance of circuits and system. With each innovation in generation of CMOS technology, the overall decrease in supply voltage and transistor length continuously makes the design of op-amp more complex [1].

Cascode amplifiers can have quite large gains and reduce significantly the miller effect, which gives them an improved frequency response compared with that of other amplifiers [2]. Speed and accuracy are the two most important properties of analog circuits, however both the aspects leads to contradictory demands because its difficult to attain both at a time. In a wide variety of CMOS analog circuits, such as switched-capacitor filters, sample and hold amplifiers and pipeline A/D converters the speed and accuracy are determined by the settling behavior of the op-amp. Fast settling requires a high unity gain frequency and a single pole settling behavior of the operational amplifier where as accurate settling behavior requires a high dc gain [5].

The proposed design of Folded-Cascode Op-Amp is designated for high frequency application such as ***RF amplifier*** and video circuits. A radio frequency amplifier, or RF amplifier, is a tuned amplifier that amplifies high-frequency signals used in radio communications. The frequency at which maximum gain occurs in an RF amplifier is made variable by changing the inductance or capacitance of the tuned circuit. An RF amplifier can tune over the desired range of input frequencies. The shunt capacitance permits high gain at radio frequencies because it adversely affects the gain of a resistance-capacitance coupled amplifier. Power gain of RF amplifiers is always limited at high radio frequencies i.e. around 20-30dB.

***Applications for RF Amplifiers*:**

Amplifier applications include electromagnetic compatibility (EMC) testing, defense components, communications testing and medical diagnostics. RF power amplifiers can be used in driving to another high power source and microwave heating. They can also be used driving a transmitting antenna, where the transmitter–receivers are used for voice and data communications as well as for weather sensing. Microwave or RF heating is used in industrial applications as well as in microwave ovens. Also, particle accelerators use RF sources.

1.1 Operational Amplifier :

Basically an Op-Amp has two input terminals i.e. Inverting terminal and Non-inverting terminal and a output

terminal and power supply. An inverting terminal is one, in which the applied input produces out of phase output. Non-inverting terminal produces in-phase output for given input.

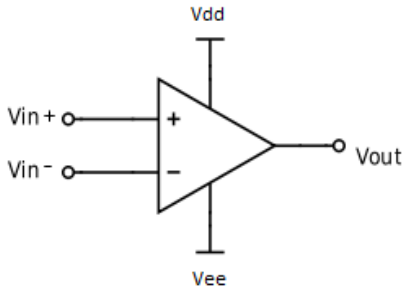

Fig. 1: Basic Op-Amp Symbol

The basic symbol for an Op-Amp is shown in fig.1 where Vin+ and Vin- are non-inverting and inverting terminals, respectively. And Vo is the output terminal, Vdd and Vee represents the positive and negative power supplies respectively.

1.2 Operational amplifier Topologies:

A few popular topologies are discussed below:

1. Two-stage Op-Amp
2. Telescopic Op-Amp
3. Folded-Cascode Op-Amp

1.2.1 Two-stage Op-Amp :

Two-stage Op-Amp mainly consists of a cascading of Voltage to Current and Current to voltage stages. The first stage consists of a differential amplifier converting the differential input voltage to differential currents i.e. voltage to current. These differential currents are applied to a current mirror load that recovers into the differential voltage. The second stage consists of common source (CS) stage MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink which converts the current to voltage at the output terminal. The second stage is also nothing more than the current sink inverter.

The major disadvantage is high power consumption due to two stages in its design and low PSRR.

1.2.2 Telescopic Op-amp :

Although Telescopic operational amplifier has smaller output swing, which means reduced dynamic range, this is offset somewhat by the lower noise factor. The above reason implies that the Telescopic op-amp is a better candidate for low power, low noise applications. There are two architectures of telescopic Op-amp i.e. with tail and without tail.

Disadvantage of a Telescopic op-amp is severely limited output swing. It is smaller than that of Folded Cascode. It has comparatively low dc gain, low PSRR, low CMRR, low bandwidth.

1.2.3 Folded-Cascode Op-Amp :

Folded cascode operational amplifier, as compared to the ordinary operational amplifier is a good gain, a single-pole operational amplifier with large output swing, because compared to a two stage operational amplifier or multi stage operational amplifier, the biggest advantage of single pole amplifiers is that the phase margin is very high and stable. Secondly, its small signal gain can be very large. Folded cascode fulfills above requirement quite well [14].

The voltage gain of the Op-Amp is given by

$$A_v = G_M . Ro$$

Where, A_v is voltage gain and Ro is output impedance

$$Ro= (gm_7 r_{07} (r_{01}||r_{09})) || (gm_5 r_{05} r_{03}).$$

Thus, voltage swing of folded cascode amplifier is slightly greater than that of telescopic configuration.

1.3 Comparison Of Various Topologies :

TABLE 1 : COMPARISON OF PERFORMANCE OF VARIOUS TOPOLOGIES

Topologies	Gain	Output swing	Power dissipation	Noise
Two stage	High	Highest	Medium	Low
Folded-cascode	Medium	Medium	Medium	Medium
Telescopic	Medium	Medium	Low	Low

II. PROPOSED ARCHITECTURE OF FCOA

The FCOA uses cascading at the output stage combined with differential amplifier, that results in achieving good ICMR. The name “folded cascode” comes from folding down n-channel cascode active loads of a differential pair and changing the MOSFET to p-channel. This operational amplifier has good PSRR as compared to two stage operational amplifier and telescopic operational amplifier [2].

Folded cascode op-amp possess a very important property i.e. it allows the input common-mode level close or nearer to supply voltage. With PMOS input, the input common-mode level can be lower to 0V while one with NMOS input it can reach to supply voltage V_{DD}. As compared to ordinary op-amp, folded cascode provides high gain with large output swing and is a single-pole op-amp. The major advantage of single-pole op-amp is that it provides great stability and large phase margin [10]. Here we are dealing with NMOS input FCOA.

The major ***disadvantage*** of PMOS input is the large area and hence more power consumption. The bandwidth of folded cascode op-amp with pmos input is comparatively lower than NMOS input FCOA. The proposed structure in fig.3 contains **differential input**, **single-ended output** folded cascode operational amplifier configuration. The main part of folded cascode op-amp is the differential pair which acts as an input stage. Hence proper matching of the differential pair is quite important. Generally an op-amp consists of a differential pair in the first stage and a common source in the second stage so as to increase the overall gain of op-amp. But this requires an additional capacitance for the frequency compensation.

Moreover, additional capacitance introduces a second pole in the amplifier system. The proposed design shown here, is set to achieve overall gain in the first stage. Also this op-amp helps in the rejection of different noise components present in the input signal and in the supply voltage. The biasing voltages V_{NB1}, V_{NB2}, V_{PB1}, V_{PB2} is provided so as to operate the transistors in saturation region is the foremost requirement of this design.

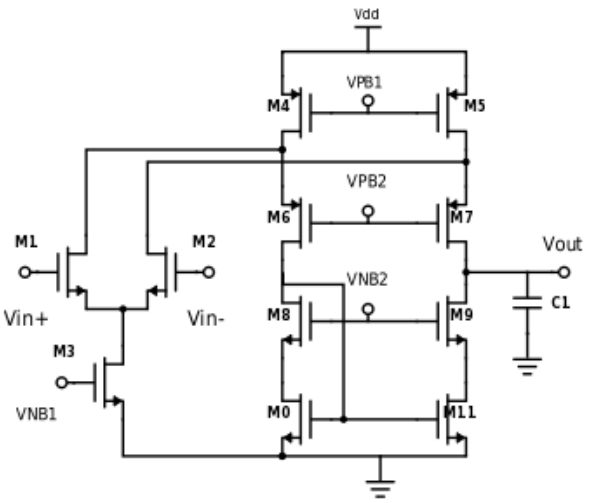

Fig 2 : Single-ended folded cascode op-amp with NMOS input

The proposed folded cascode op- amp is designed using differential NMOS input because these types of input gives more output gain and more stability in comparison to PMOS input configuration. The gain bandwidth of NMOS input is much more higher than PMOS input configuration. The 3pF of capacitor load also used in this circuit design thus to stabilize the phase of the op-amp circuit. In fig 3, M1 and M4 form one cascode structure and M2 and M5 form another. The biasing should be adjusted accordingly to bring all transistors in saturation region of operation. The current mirror converts the differential signal into single-ended output by sending variations in the drain current to the output.

The resulting op-amp is differential input folded cascode op-amp. Our requirement of higher bandwidth, low power, high swing and higher g_m is fulfilled in FCOA with nmos input.

The nmos input FCOA provides higher bandwidth than pmos FCOA. As we know that,

$$\text{GBW}= \frac{g_m}{2\pi.C_L}$$

So, the higher transconductance will provide higher gain bandwidth. And hence the gain of any operational amplifier depends on the transconductance of the amplifier. Thus, higher is the transconductance , better will be the gain of the amplifier.

2.1 Architecture of proposed design in Tool :

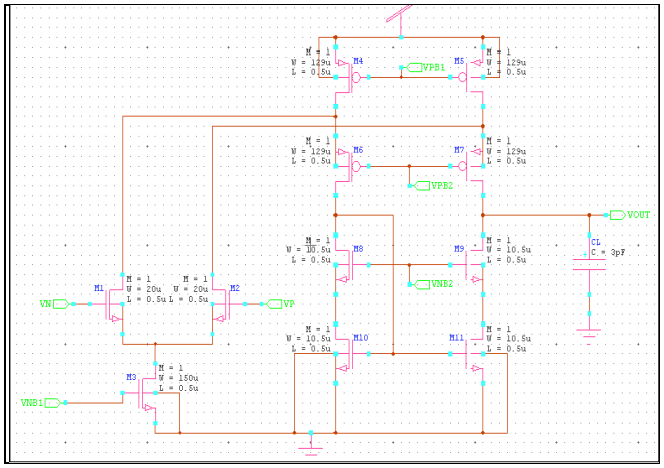

Fig 3 **:** Schematic of proposed folded-cascode design in tool

III. PARAMETERS TO BE MEASURED

3.1 Gain (dB) :

Operational amplifiers basic function is to amplify the input signal and the higher is its open loop gain, the better as in many applications they are used with a feedback loop, so ideal op-amps are characterized by a gain of infinity. For practical op-amps, the voltage gain is finite. Typical values for low frequencies and small signals are A = 102 – 105, corresponding to 20-100 dB gain. This is the open loop differential gain measured as a function of frequency.

3.2 Common Mode Rejection Ratio (CMRR):

The common mode rejection ratio (CMRR) of an operational amplifier is the ratio between the differential gain and the common mode gain. Where A_D is

$$A_D = \frac{V_O}{V_A - V_B}$$

The CMRR is defined as AD/AC or (in logarithmic units)

$$\text{CMRR}= 20 \log_{10}(A_D/A_C)\text{ , In decibels}$$

Typical CMRR values for CMOS amplifiers are in the range 60 to 80 dB. The CMRR is a parameter that measures that how much the op-amp can suppress noise, and hence a large CMRR is an important requirement.

3.3 Power Supply Rejection Ratio (PSRR):

We apply a small signal in series with the positive or the negative power supply we obtain a corresponding signal at the output with a given amplification .The ratio between the differential gain and the power supply gain leads to two PSRRs. These are two merit factors showing the ability of the op-amp to reject spur signals coming from the power supply.

Having a good PSRR is an important merit. Unfortunately, especially at high frequencies, the PSRR achieved is quite poor .A typical value of PSRR is 60dB at low frequencies that decreases to 20-40dB at high frequencies**.**

PSRR=20 log (Vout/Vin) , in decibels

3.4 Offset Voltage (Vos):

The output of an amplifier is supposed to be independent from common mode inputs applied at the input terminals and is supposed to be zero when the voltage difference between the inverting and non-inverting inputs is said to be zero or can say when both inputs are equal.

For an ideal op-amp, if $V_a = V_b$ (which is easily obtained by short circuiting both the input terminals) then $V_o = 0$. In real devices, this is not exactly the scenario, and a voltage $V_{0,\ off} \neq 0$ will occur at the output for shorted input voltages. Since $V_{0,\ off}$ is directly proportional to the gain of the amplifier, the effect can be more conveniently described in terms of the input offset voltage $V_{in,off}$, defined as the differential input voltage needed to restore $V_o = 0$ in the real devices. For MOS op-amps mostly $V_{in,off}$ is about 5- 15mV[13].

3.5 Input Common Mode Range (ICMR) :

This is basically the voltage range that we can use at input terminal without producing a significant degradation and reduction in op-amp performance. Since the typical input stage of an op-amp is a differential pair, the voltage required for the proper operation of the current source and the input transistors limit the input swing. A large input common mode range is very important when the op-amp is used in the unity gain configuration. In this case the input must follow the output. The op-amp must possess good ICMR for desirable performance[13].

3.6 Output Voltage Swing :

It is the maximum swing at the output terminal without producing a significant degradation of op-amp performance.

Typically it ranges between 60% to 80% of (V_{DD}-V_{SS}). Within the output swing range the response of the op-amp should conform to given specifications and in particular the harmonic distortion should remain below the required level.

3.7 Unity Gain Bandwidth:

Because of stray capacitances and finite carrier mobilities , the gain A_{DC} decreases at high frequencies. It is usual to describe this effect in terms of the unity gain bandwidth, that is the frequency f_T at which $|A_{DC}(f_T)| = 1$. For MOS op-amps, f_T is usually in the range of 1-10 MHz. The frequency at which the gain becomes $0dB$ is called unity gain frequency f_T . Therefore, f_T is also known as the gain-bandwidth product, GBW.

3.8 Slew Rate (SR) :

Slew rate of an Op-amp is defined as the maximum rate of change of output for the small change in input.

$$SR = \left[\frac{dVo}{dt}\right]_{\max}$$

This is the maximum achievable time derivative of the output voltage. It is measured using the op-amp in the open loop or the unity gain configuration. A large input step voltage fully imbalances the input differential stage and brings the op-amp output response into the slewing conditions .The positive slew rate can be different from the negative slew rate, depending on the specific design. Typical values ranges between 40 and 80V/ µs.

3.9 Phase Margin (PM):

This is the phase shift of the small –signal differential gain measured at the unity gain frequency. In order to ensure stability when using the unity gain configuration it is necessary to achieve a phase margin better than 60 degree. A lower phase margin (like 45 degree or less) will cause ringing in the output response. However, for integrated implementation it is not strictly necessary to ensure absolute stability.

3.10 Power Consumption :

This is the power consumed under standby conditions. The power used in the presence of a large signal can significantly exceed the one required in the quiescent conditions. Moreover, the consumed power depends on the speed specifications. Typically, higher bandwidth leads to higher power consumption. Low power operation is a very important quality factor: batteries that should supply the system for hours or days power more and more electronic systems. Thus, a key design task to achieve low power consumption for required speed.

IV. DESIGN METHODOLOGY

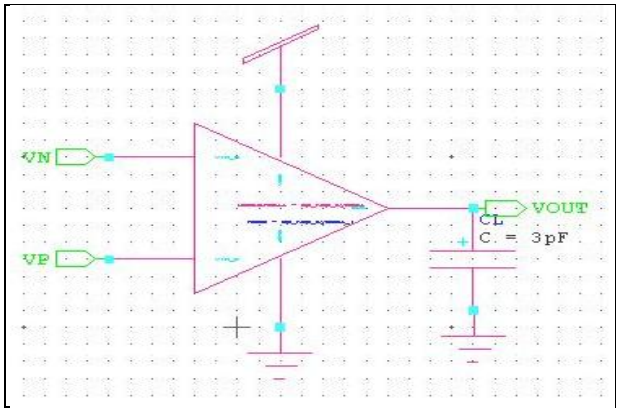

Fig 4 : Symbolic representation of FCOA

4.1 Design Specifications:

TABLE 2 : DESIGN SPECIFICATIONS

PARAMETERS	VALUE
DC GAIN	40dB
GBW	30 MHz
PHASE MARGIN	$\geq 60°$
SLEW RATE	$\geq 20\ V/\mu s$
C_L	3pF
V_{DD}	2.5 V
V_{SS}	0 V
ICMR(+)	2.1 V
ICMR(-)	0.9V
POWER DISS.	<5 mW
CMRR	50 dB
OUTPUT SWING	-2.3 V to 2.1V

TABLE 3 : ASPECT RATIO

TRANSISTOR NAME	W/L RATIO (µ/ µ)
M1, M2	20/0.5
M3	150/0.5
M4, M5	129/0.5
M6, M7	129/0.5
M8, M9	10.5/0.5
M10,M11	10.5/0.5

TABLE 4 : VALUES TO BE USED IN DESIGN STEPS

PARAMETERS	VALUE
$V_{OUT(min)}$	2.3 V
$V_{OUT(max)}$	0.4 V
K_P'	70µ
K_N'	220µ
$V_{IN\ (min)}$	0.9V
$V_{IN\ (max)}$	2.1 V
V_{T1} (NMOS)	0.43 V
V_{T1} (PMOS)	-0.43 V

4.2 Design equations :

1. The first step of the design gives the estimation of the bias current. Assuming the Slew Rate, we have

$$I_3 = SR.C_L \quad (1)$$

2. Bias currents in output cascode, thus avoiding zero currents in cascode .

(I$_4$ and I$_5$, should be designed so that I_6 and I_7 never become zero)

$$I_4 = I_5 = 1.2I_3\ to 1.5I_3 \quad (2)$$

3. Design for S9 and S7 using the maximum output voltage , Vout(max) , Since, I$_5$ is equal to I_7

$$V_{SD5}(sat) = V_{SD7}(sat) = 0.5\left[V_{DD} - V_{out}(\max)\right] \quad (3)$$

$$S_5 = \frac{2I_5}{K_P' V_{SD5}^2}, S_7 = \frac{2I_7}{K_P' V_{SD7}^2}, \left(S_4 = S_5, S_6 = S_7\right) \quad (4)$$

4. Design for S3, S4, S5 and S6 using the minimum output voltage, Vout (min):

Since, I$_4$ and I$_5$ is equal to I$_9$ and I$_{11}$

$$V_{SD9}(sat) = V_{SD11}(sat) = 0.5\left[V_{out}(\min) - V_{ss}\right] \quad (5)$$

$$S_{11} = \frac{2I_{11}}{K_N' V_{SD11}^2}, S_9 = \frac{2I_9}{K_N' V_{SD9}^2}, \left(S_{10} = S_{11}, S_8 = S_9\right) \quad (6)$$

5. Design S1 and S2 to achieve desired gain bandwidth product,

$$S_1 = S_2 = \frac{g_{m1}^2}{K_N' I_3} = \frac{GB^2.C_L^2}{K_N' I_3} \quad (7)$$

6. Using minimum input common mode :

$$S_3 = \frac{2I_3}{K_N'\left(V_{in(\min)} - V_{SS} - \sqrt{\left(I_3 / K_N' S_1\right)} - V_{T1}\right)^2} \quad (8)$$

7. Using maximum input common mode :

S4 and S5 must meet or should exceed the values in step3

$$S_4 = S_5 = \frac{2I_4}{K_P' \left(V_{DD} - V_{in(\min)} + V_{T1}\right)^2} \quad (9)$$

8. Power dissipation (P_{diss}) is given by :

$$P_{diss} = (V_{DD}-V_{SS})\,(I_3+I_{10}+I_{11}) \quad (10)$$

V. SIMULATION RESULT

In the designing of this proposed Folded-Cascode Operational Amplifier, to determine the various characteristics, a number of analysis had been carried out and are presented here. Some of them are explained here. The analyses are performed on single-stage FCOA designed in 0.25µm CMOS technology.

5.1 DC Analysis :

DC analysis is used to determine the quiescent point of the device operation. In folded cascode Op-Amp, all the transistors must work in saturation. To determine that all transistors are operating in saturation or not for the entire input common mode range, DC analysis is performed. The DC analysis of Op-Amp also gives the information about the characteristic of Op-Amp i.e. trans-conductance, threshold voltage, current gain value etc. Fig.6 shows the set-up for DC analysis of Folded-Cascode Op-Amp. The minimum common mode range input supply of 1V is applied to both the input terminals.

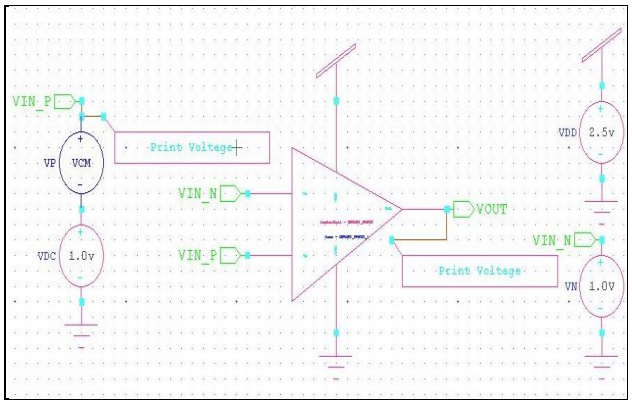

Fig 5 : Set-up for DC analysis of FCOA

5.1.1 *ICMR Measurement*

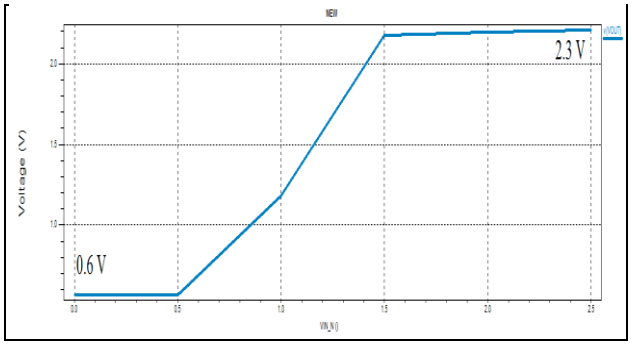

Fig 6 : Plot for ICMR measurement

5.2 AC Analysis :

AC analysis is used to determine the open-loop gain, gain-bandwidth(GBW), common mode rejection ratio(CMRR), power supply rejection ratio(PSRR) and phase margin of folded-cascode Op-Amp. The AC analysis gives the frequency response of the designed Op-Amp. Ac analysis is carried out by connecting an AC source to the one of the input terminal with the minimum DC value required to keep the transistors in the saturation region of operation. Fig.8 shows the set-up for DC analysis of Folded-Cascode Op-Amp[12].

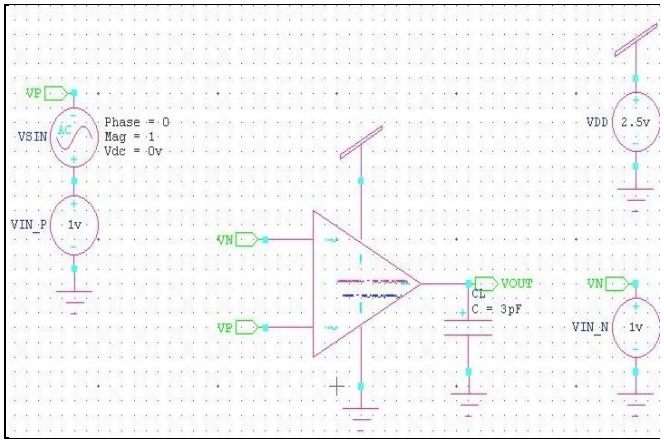

Fig 7 : Set-up for AC analysis of FCOA

5.2.1 DC Gain

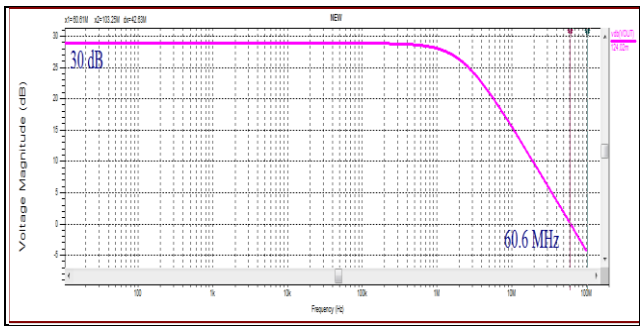

Fig 8: Gain-Frequency plot for FCOA

5.2.2 Phase Margin

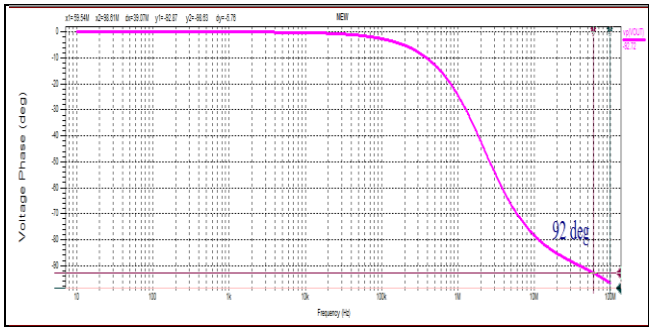

Fig 9 : Phase-Frequency plot for FCOA

5.3 Transient Analysis:

Transient analysis gives the timing details of the device. In the case of folded-cascode Op-Amp, transient analysis is used to determine settling time, slew rate, output voltage

swing. The transient analysis mainly shows how fast the system or device responds to the applied input. The transient response is performed by applying sinusoidal input and pulse input in the input terminal.

5.3.1 Sinusoidal Input:

Transient analysis of Op-Amp using sinusoidal input is used to determine the **output voltage swing.**

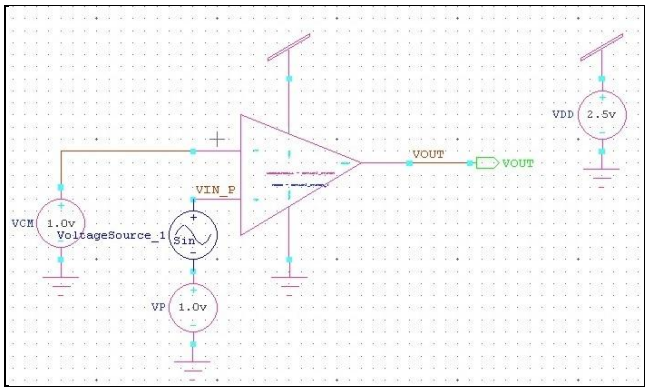

Fig 10 :Set-up for Transient analysis for sinusoidal input

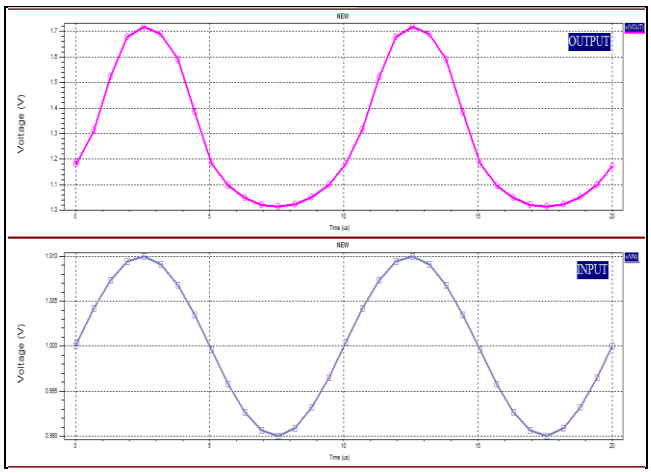

Fig 11 :Transient Analysis output for sinusoidal input

5.3.2 Pulse Input:

Transient analysis of Op-Amp using Pulse input is used to determine the speed of Op-Amp. The **slew rate** (SR) and setting time of Op-Amp is obtained from the transient analysis using pulse input.

The simulation result of pulse input transient analysis also gives *Settling Time* of **105 ns**.

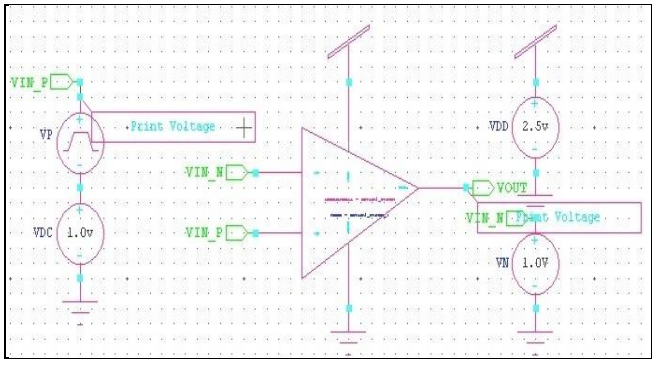

Fig 12 :Set-up for Transient analysis for pulse input

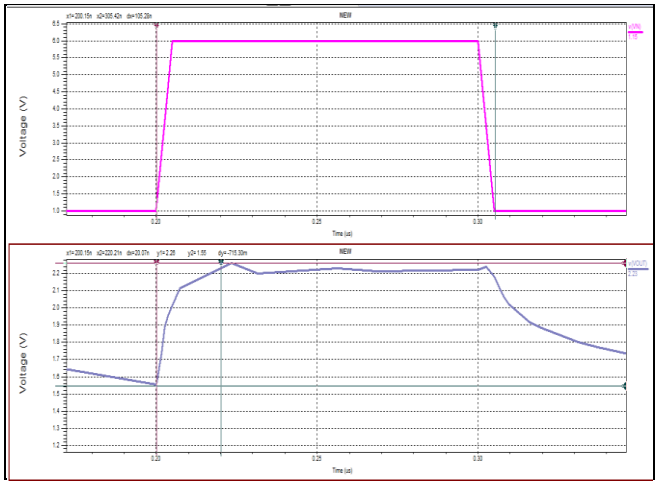

Fig 13 :Transient Analysis output for pulse input

TABLE 5 : SUMMARY RESULT

PARAMETERS	SPECIFICATIONS	SIMULATED OUTPUT
DC Gain	40dB	30dB
GBW	>30 MHz	>60MHz
Phase Margin	$\geq 60°$	$\geq 60°$
Slew Rate	$\geq 20\ V/\mu s$	$35\ V/\mu s$
ICMR(+)	2.1 V	2.3 V
ICMR(-)	0.9V	0.6 V
Power Diss.	≤5 mW	5.03 mW
CMRR	50dB	36dB
Output Swing	-2.3 V to 2.1V	0.6V to 2.08V

VI. CONCLUSION

We have successfully simulated circuits for measuring ac gain and have calculated the phase margin. We have also measured CMRR, output-swing and Slew-rate. The development of a design equation based procedure provides a quick and effective mechanism for directly estimating the MOS circuit parameters of the op-amp. The performance requirements Op-amp designed with these calculated circuit values were able to satisfy these requirements to a good extent as evidenced by the T-spice simulations.

The transistors size of the architecture has been tuned so as to operate all the transistors in saturation along with adjusting the biasing to get the output .The results of SPICE simulation results are shown to agree very well with the use of our design equations.

VII. FUTURE SCOPE

The op-amp proposed in this paper is implemented in Tanner in 0.25µm CMOS technology which produces a gain of 30dB in a single stage without the need of frequency compensation. High CMRR of 36 dB is obtained after simulation.

To increase input and output swing further the current mirror used here can be replaced with high **swing cascode current mirror**. Stability of this amplifier can be increased using a common mode feedback circuit. For high gain applications **gain boosting technique** can be used. Furthermore, the **slew rate can be enhanced** using PMOS inputs in differential pair in place of NMOS inputs.

Using PMOS inputs in differential pair, the flicker noise can be reduced to more acceptable level.

TABLE 6 : COMPARISON OF THE PROPOSED FOLDED CASCODE OP-AMP WITH PRIOR DESIGNS

Parameters	**[15]**	**[14] ,[2]**	**[20]**	**This Work**
Technology	1.25 µm	0.18 µm	0.13 µm	0.25 µm
Supply voltage(V)	±2.5	1.2	1.2	2.5
Gain(dB)	55	50.9	49	30
PM(degree)	-	77.2	-	> 60
UGB(MHz)	8	490	58	>60
Slew Rate(V/µs)	8.55	-	2.71	35
Power(mW)	-	0.661	0.22	5.03
Output swing(V)	-2.3V to +2.0V	-	±0.7 V	0.6V to 2.08V
CMRR	-	-	52.7dB	36dB
Settling Time	-	-	-	105 ns

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